Reconfigurable Computing Lab Summer Coop Projects 2018

Debug, test and performance features for heterogeneous multicore architectures on FPGAs -- Dr. Lesley Shannon

Background: Soft-processors are an important part of the FPGA ecosystem. Their potential for offering high levels of configurability enables their use in systems ranging from simple micro controllers to complex many core systems. Additionally, soft-processor systems on FPGAs offer the flexibility to researchers to perform system level computer architecture. In industry, the largest time component for any project is the verification of a design. A processor system provides particular challenges due to large amounts of non-deterministic behaviour in systems along with complex software-hardware interactions.

Objective: This project will have a student extend debug and verification support for our existing Taiga soft-processor along with exploration into micro-architectural improvements. They will develop new automated test infrastructure for the processors functional units and a framework to be used for the addition of new units. They will also have the opportunity to investigate performance enhancing features, a possible example of which could be investigating new branch predictor implementations. This project provides an opportunity to learn about micro-architectural design considerations for FPGA-based soft-processors as well as methods of debugging and verifying HDL designs.

Skills needed:
- Programming competency in either VHDL or Verilog HDL (will learn SystemVerilog during coop);
- Scripting language knowledge (preferably Python and tcl)
- Competency with FPGAs and their CAD tools (either Xilinx or Altera, preferably Xilinx);
- Completed ensc350 (ensc452 would be an asset)
- Designed a MicroBlaze/NIOS/ARM based SoC on an FPGA would be very helpful, but is not required.

Please visit my website for further information on my research interests and course offerings: http://www.ensc.sfu.ca/~lshannon/.