Reconfigurable Computing Lab Summer Coop Projects 2016

1. Floating Point Unit design for a Variable Length Pipeline Processor -- Dr. Lesley Shannon

**Background:** Multicore systems are a key component of our computing framework. They are used in almost every aspect of computing - from servers, databases, and cloud computing resources to embedded and portable computing platforms. They allow one (or more users) to perform a variety of computations. As computing tasks and platforms become complex, the challenge of selecting appropriate architectures and scheduling algorithms to provide the desired data throughput while being energy efficient has become increasingly complex. In a world where data centres consume at least as much energy as the airline industry, investigating the architectural tradeoffs such as how to effectively integrate heterogeneous components into an energy efficient platform is an important area of modern research.

**Objective:** Our team is currently developing a multicore system based on a Variable Length Processor (RISC V) Architecture. This research project will have a student develop support for the processor’s floating point unit. Floating Point (FP) instructions use a separate register file, but the load/store instructions and conversion operations between FP and integer would need be provided by another team member. The student would be responsible for the arithmetic pipeline and some of the decode functionality. Specifically, the student would be responsible for implementing arithmetic support for ADD/SUB, MUL/DIV, compare and SQRT operators for 32 and 64 bit FP operations. The objective is to make the final multicore system open source to be used by the research community, making this potentially a high impact contribution to research in heterogeneous systems worldwide.

**Skills needed:**
- Strong programming competency in either VHDL, Verilog, or SystemVerilog HDL;
- Solid intuition for translating algorithms to architectures
- Strong Critical thinking skills required
- Keen understanding of hardware design and fundamental processor architecture.
- Competency with FPGAs and their CAD tools (either Xilinx or Altera- however Xilinx is preferable);
- High-level language programming skills (preferably C or C++);
- Completed ensc350 by time of start of coop (required)
- Designed a MicroBlaze/NIOS/ARM based SoC on an FPGA would be very helpful, but is not required.
- Experience with the Linux kernel and/or device driver design would also be an asset, but not required.

Please visit my website for further information on my research interests and course offerings: [http://www.ensc.sfu.ca/~lshannon/](http://www.ensc.sfu.ca/~lshannon/).