

A. Henkel, S.L. Delage, M.-A. diForte-Poisson, E. Chartier and H. Blanck (Laboratoire Centrale de Recherches, Thomson-CSF, Domaine Corbeville, 91404 Orsay/Cédex, France)

H.L. Hartnagel (Institut für Hochfrequenztechnik, Technische Hochschule Darmstadt, 64283 Darmstadt, Germany)

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Improved breakdown voltages in submicrometre planar GaAs MESFETs with a thin (Ga,In)P surface layer

C.R. Bolognesi, M.W. Dvorak, G. Soerensen and S.P. Watkins

Indexing term: MESFET

A thin 100Å (Ga,In)P surface layer in the extrinsic gate-to-drain space of the transistor improves the power-handling capabilities of MOCVD-grown planar GaAs MESFETs. The authors demonstrate 0.8µm devices with drain and gate-drain breakdown voltages of 21 and 23-24V, respectively. Although achieved in non-optimised structures, the results are comparable to some obtained with more complicated passivation approaches.

The breakdown mechanisms in GaAs MESFETs have been of much interest over the last 20 years. Several techniques such as the use of gate recessing [1], surface state chemical passivation by chemical dips in (NH₄)₂S_x [2], the development of low-temperature grown GaAs non-stoichiometric surface layers with enhanced bulk breakdown fields [3, 4], and overlapping gate structures [4 - 6] have been shown to lead to significant improvements in MESFET power handling capabilities. Recent work [7] has also shown that Ga_{0.5}In_{0.5}P [(Ga,In)P] channel MESFETs can display very high breakdown voltages because of the high breakdown field values in (Ga,In)P. To our knowledge, no study has been carried out on the effect of a (Ga,In)P passivation layer deposited at the surface of otherwise conventional GaAs MESFETs.

In this Letter, we demonstrate that an MOCVD-grown 100Å (Ga,In)P surface passivation layer enhances both the ON- and OFF-state breakdown voltages of planar geometry GaAs MESFETs. Non-recessed MESFETs can be prone to early breakdown phenomena, and this simple configuration was chosen to emphasise the role of the gate-drain surface space in the breakdown behaviour of MESFETs. The present passivation approach is simple, effective, and does not increase process complexity. In fact, the (Ga,In)P cap structure permits excellent *I_{DSS}* control because of the good etch selectivity between GaAs and (Ga,In)P.

Our MESFET structures were grown on (100)-oriented GaAs substrates in a Thomas-Swan vertical MOCVD reactor at a pressure of 50 torr at a temperature of 600°C using a hydrogen carrier flow of 2.3 SLM. Trimethylgallium (TMG), tertiarybutylarsine (TBA), and tertiarybutylphosphine (TBP) were the alkyl precursors used. Doping was performed using 500ppm hydrogen sulphide diluted with high-purity hydrogen. Undoped layers of GaAs, grown with the above conditions using TMG and TBA, show residual *p*-type background concentrations of ~10¹⁵cm⁻³. A

3000Å *p*-undoped GaAs buffer layer was first grown to reduce hot electron injection in the buffer layer and minimise short-channel effects due to substrate currents. The buffer was followed by a 2000Å GaAs channel doped at 10¹⁷cm⁻³ with sulphur. This is the baseline structure for the present study. A nominally identical structure differing only by the addition of a 100Å (Ga,In)P sulphur-doped cap was also grown for comparison.

Hall effect measurements on the as-grown samples revealed a sheet density of *N_s* = 1.55 × 10¹²cm⁻², and a mobility of μ = 3900cm²/Vs for the GaAs baseline sample, and *N_s* = 1.88 × 10¹²cm⁻² and μ = 4150 cm²/Vs for the (Ga,In)P -capped sample. The selective removal of the (Ga,In)P cap layer with an HCl etch results in *N_s* = 1.40 × 10¹²cm⁻² and μ = 4050cm²/Vs. Devices from both samples were processed simultaneously: Ge/Au/Ni/Au Ohmic contacts were formed by first selectively removing the cap layer (if present) by wet etching, and by annealing at 400°C. Ti/Au (100nm/300nm) gates were defined by conventional hard contact optical lithography and lift-off after selectively exposing the GaAs surface under the gate finger with an HCl-based wet etch relying on the excellent etch selectivity between (Ga,In)P and GaAs. The gate finger is positioned at the centre of the 4µm source-drain space. Fig. 1 shows a schematic cross-section of the finished (Ga,In)P -capped devices.

In the following, we define the ON-state drain breakdown voltage as the drain bias at which the device undergoes irreversible damage with a zero gate bias. The OFF-state breakdown is defined as the drain voltage at which *I_D* = *I_{DSS}*/10 under a pinched channel condition.

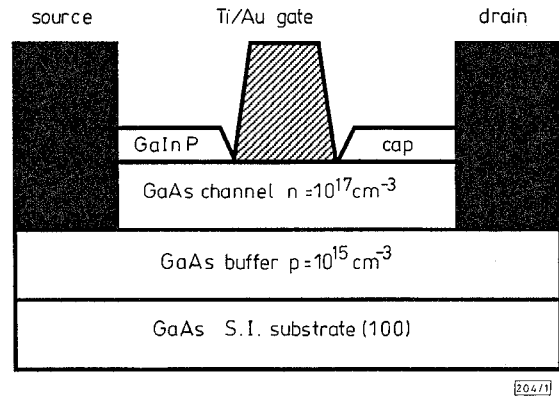


Fig. 1 Schematic representation of device structure studied here

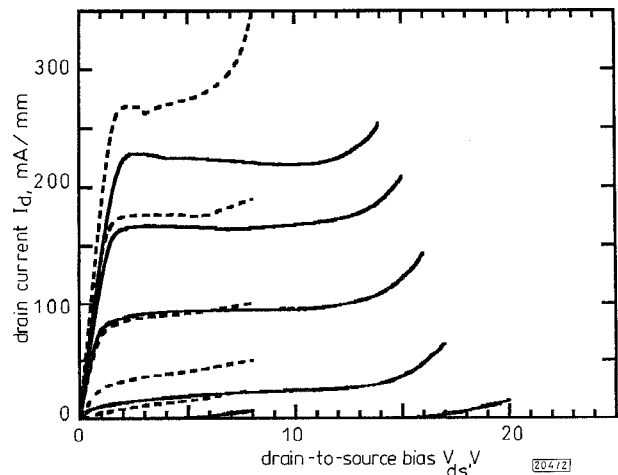


Fig. 2 Typical room temperature drain characteristics for baseline GaAs MESFETs and for (Ga,In)P-capped MESFETs

Gate length: 0.8µm
 Gate voltage is stepped from *V_{GS}* = 0 in increments of -1V
 - - - - baseline GaAs MESFETs
 ——— (Ga,In)P-capped MESFETs

Fig. 2 shows typical drain characteristics for 0.8µm gate devices centred in a 4µm source-to-drain space. Both the GaAs baseline and the (Ga,In)P-capped MESFETs exhibit good pinch-off characteristics. The (Ga,In)P-capped samples are characterised by ON-state breakdown voltages of 14V, and OFF-state breakdown volt-

ages of 21–22V. In comparison, the baseline all-GaAs MESFET structure showed ON and OFF-state breakdown voltages of 8–9V, and 13–14V respectively. The (Ga,In)P-capped MESFETs are characterised by gate-to-drain breakdown voltages $BV_{DG} = 23$ –24V defined at a 1mA/mm gate leakage current during common-source transistor operation. It is remarkable that such a significant improvement in breakdown voltage can be achieved by inserting a 100Å thick layer at the sample surface: this fact indicates that the very sample surface plays a dominant role in determining the breakdown behavior of GaAs MESFETs. The same conclusion could also be reached from the sulphide passivation experiments of [2].

It is difficult to perform a direct and meaningful comparison between devices implemented in different laboratories with different processes and geometries. However, the present results are comparable to some achieved by others for submicrometre devices with low-T GaAs passivation and overlapping gates [5], despite the fact that our 100Å (Ga,In)P cap is significantly thinner than the 500–1000Å LT-GaAs thicknesses commonly used [3–5]. The use of (Ga,In)P passivation layers allows GaAs MESFET structures to remain aluminium-free since no AlAs layers are required to restrict point defect diffusion from LT-GaAs layers: this could turn out to be a reliability advantage but experimental verification will be required to validate these expectations. From a manufacturability standpoint, the (Ga,In)P-GaAs MESFET system enjoys an excellent etch selectivity, another desirable feature for a production technology. The optimisation of the (Ga,In)P cap thickness and doping density will most likely lead to further increases in breakdown voltages.

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C.R. Bolognesi and M.W. Dvorak (*Compound Semiconductor Device Laboratory, School of Engineering Science and Physics Department, Simon Fraser University, Burnaby, British Columbia, V5A 1S6, Canada*)

G. Soerensen and S.P. Watkins (*Department of Physics, Simon Fraser University, Burnaby, British Columbia, V5A 1S6, Canada*)

E-mail: colombo@sfu.ca

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Microwave performance of 0.25µm doped channel GaN/AlGaIn heterostructure field effect transistor at elevated temperatures

Q. Chen, R. Gaska, M. Asif Khan, M.S. Shur, A. Ping, I. Adesida, J. Burm, W.J. Schaff and L.F. Eastman

Indexing terms: Field effect transistors, Microwave transistors

The authors report the DC and microwave performance of a 0.25µm gate doped channel Al_{0.14}Ga_{0.86}N/GaN HFETs exhibiting a cutoff frequency of 37.5GHz and a maximum frequency of oscillations of 80.4GHz. The calculations of the Fermi level position and comparison with the expected conduction band discontinuity confirm that the channel in these transistors is doped. DC and microwave characteristics of these devices do not change much with temperature up to at least 200 and 90°C, respectively.

We recently reported doped channel AlGaIn-GaN heterostructure field effect transistors (DC-HFETs) with 1 µm gate length [1, 2] and deep submicrometre gates [3, 4], which demonstrated excellent potential for operation at microwave frequencies. Our calculations of low field [5] and high field [6] properties showed that these devices should also exhibit superior performance at elevated temperatures.

In this Letter, we report the DC and microwave performances of 0.25µm gate doped channel Al_{0.14}Ga_{0.86}N/GaN HFETs and show that microwave characteristics of these devices do not change much with temperature up to at least 90°C.

The material growth and device fabrication have been described before (see for example [1]). The Hall mobility and electron sheet carrier concentration, $n_{s,Hall}$ were 1044cm²/V-s and 1.4×10^{13} cm⁻², respectively. The device width, W , was 50µm. The drain-to-source separation was 2 µm. The offset gate design was used to improve the high voltage characteristics with a gate-to-source spacing of ~0.6µm.

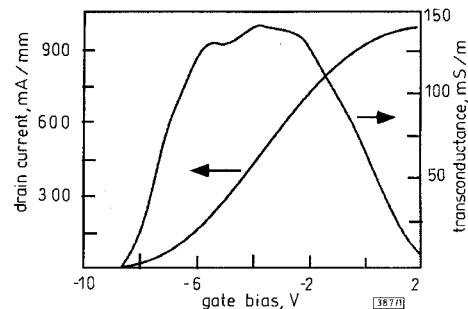


Fig. 1 Measured dependencies of drain-to-source current and device transconductance in saturation region

The devices used in this investigation had a large threshold voltage (close to ≈ 8.5 V). The measured dependencies of the drain-to-source current and device transconductance in the saturation region (at the drain bias of 8V) are shown in Fig. 1a. The maximum measured transconductance (at the gate bias of ~ 3.7 V) was $g_m = 142$ mS/mm comparable to the record values reported by other groups [7–9]. We crudely estimate our source series resistance to be $R_s = 2.5\Omega$ -mm and the maximum intrinsic transconductance $g_{m0} = g_m/(1-g_m R_s) = 220$ mS/mm.

Fig. 2 shows the measured current-voltage characteristics. The maximum drain-to-source current observed at a gate bias of 2V and drain bias of 10V was 1.02A/mm, which is, to our knowledge, the largest current observed for GaN/AlGaIn FETs. It is interesting to notice the absence of the negative differential resistance usually observed in GaN/AlGaIn HFETs at high current densities [2]. This may be explained by a reduced power dissipation in these relatively narrow gate devices (50µm). The gate leakage current remains small even at a gate bias of 2V. As seen from Fig. 3, the devices exhibited excellent pinch-off characteristics. This is in agreement with positive transconductance measured at such a bias (see Fig. 1). An important role played by the source series resistance is clearly seen from a small modulation of the channel-conductance at large gate-voltage swings.