# CONTACT

asa582@sfu.ca

in ahmadsb101

## **AHMAD SEDIGH BAROUGHI**

# **EDUCATION**

M.Sc. - Electrical Engineering

University of Tabriz, Tabriz, Iran

Supervisor: Jafar Sobhi

**Thesis**: Design and Implementation of an 8-bit RISC-based micro-controller core with 60-MHz clock frequency and low power consumption

B.Sc. - Electrical Enginering
Shahid Beheshti University, Tehran, Iran

2015

2018

## RESEARCH INTERESTS

FPGA Design
 Accelerated Computing
 Multicore Systems
 Computer Architecture
 Intelligent System Design

## **PUBLICATIONS**

#### **Carry Disregard Approximate Multipliers**

**IEEE Early Access** 

IEEE Transactions on Circuits and Systems I: Regular Papers

Nima Amirafshar, Ahmad Sedigh Baroughi, Hadi Shahriar Shahhoseini, and Nima TaheriNejad

# High Performance Application-oriented Memory Management on Multi-core Systems

**IEEE Indexed** 

2020 6th Iranian Conference on Signal Processing and Intelligent Systems (ICSPIS)

Ahmad Sedigh Baroughi, and Madjid Naderi Award: Outstanding Paper

# AxE: An Approximate-Exact Multi-Processor System-on-Chip Platform

**IEEE Indexed** 

2022 25th Euromicro Conference on Digital System Design

Ahmad Sedigh Baroughi, Stefan Huemer, Hadi Shahriar Shahhoseini, and Nima TaheriNejad

#### An Approximate Carry Disregard Multiplier with Improved Mean Relative Error Distance and Probability of Correctness

**IEEE Indexed** 

2022 25th Euromicro Conference on Digital System Design

Nima Amirafshar, Ahmad Sedigh Baroughi, Hadi Shahriar Shahhoseini, and Nima TaheriNejad

# CERTIFICATES

Outstanding Paper in: 6th Conference on Signal Processing and Intelligent Systems (ICSPIS 2020)

Developing FPGA-accelerated cloud applications with SDAccel: Theory

# **WORKSHOPS**

#### Task Scheduling on Mixed-Precision MPSoC

Oct 2021

6th Workshop on Approximate Computing

International Conference on Computer Aided Designs (ICCAD)

# **WORK EXPERIENCE**

**FPGA Designer** 

Feb. 2021 to Mar. 2023

Hooshman Accelerator Group

Main duties: Designing digital circuits, simulating, and testing FPGA designs

#### TEACHING ASSISTANT EXPERIENCES

#### **CMOS Circut Designs, Layout, and Simulation**

Jan 17 - Jun 17

Part-time

Instructor: Prof. Jafar Sobhi

Responsibilities: Reviewed course content, graded assignment, tutored simulator, and assisted on final project

**VLSI Designs** 

Jan 18 - Jun 18

Instructor: Prof. Jafar Sobhi

Responsibilities: Reviewed course content, graded assignment, tutored simulator, and assisted on final project

**Electronics I, and II** 

Sep 20 - Jun 21

Instructors: Prof. Ahmad Ayatollahi, and Prof. Shahriar

Shahhoseini

Responsibilities: Reviewed course content, graded assignments, and assisted on final project

# SKILLED SOFTWARE

gem5, Sniper

Multi-core Simulator

Deep Learning, Image Processing, and Parallel Computing Toolboxes

MATLAB

Vivado, Vitis, VitisAI, and ISE

Xilinx

Virtuoso, Genus, and Innovus

Cadence