Alec Lu

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Education

Simon Fraser University (Burnaby, Canada)

- PhD Student (Computer Engineering) 2018 – Present
- Bachelor of Applied Science (Systems Engineering) 2012 – 2018

Research and Work Experience

Simon Fraser University (Burnaby, Canada) – Research Assistant Sept 2018 - Present

- Advised by Prof. Zhenman Fang and Prof. Lesley Shannon with a focus on big data analytics acceleration using FPGAs via High-level Synthesis (HLS) and RTL designs. See publications and projects for more details. Published eight papers and two recently got accepted.

Meta (Redmond, United States) – ASIC Design Engineer Intern Jun 2022 – Oct 2022

- Implemented and verified computer vision related hardware blocks using catapult HLS, based on the architecture specification document.
- Optimized HLS designs through automation for characterizing different μarchitecture details

Intel (Burnaby, Canada) – SoC Design Engineer Intern Jan 2017 – Dec 2017

- Implemented and verified RTL and firmware design features based on architecture specifications for a Xilinx FPGA-based SSD memory reliability testing platform.

Publications

Accepted Papers

2. Peiyan Dong, Mengshu Sun, **Alec Lu**, et al., "*HeatViT: Hardware-Efficient Adaptive Token Pruning for Vision Transformers*", IEEE International Symposium on High-performance Computer Architecture (HPCA 2023), Feb 2023

1. Xingyu Tian, Zhifan, Ye, **Alec Lu**, Zhenman Fang, " *SASA: A Scalable and Automatic Stencil Acceleration Framework for Optimized Hybrid Spatial and Temporal Parallelism on HBM-based FPGAs*", ACM Trans. Reconfig. Technol. Syst. (TRETS 2022), 2022

Published Conference Papers

6. Geng Yuan, Sung-En Chang, Qing Jin, **Alec Lu** et al., "*You Already Have It: A Generator-Free Low-Precision DNN Training Framework using Stochastic Rounding*", European Conference on Computer Vision (ECCV 2022), Oct 2022

5. Zhengang Li, Mengshu Sun, **Alec Lu** et al., "*Auto-ViT-Acc: FPGA-Aware Automatic Acceleration Framework for Vision Transformer with Mixed-Scheme Quantization*", 32nd International Conference on Field Programmable Logic and Applications (FPL 2022), Dec 2022

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4. Mengshu Sun, Zhengang Li, **Alec Lu** et al., "*FILM-QNN: Efficient FPGA Acceleration of Deep Neural Networks with Intra-Layer, Mixed-Precision Quantization*", The 30th ACM/SIGDA Int'l Symp. On Field-Programmable Gate Arrays (FPGA 2022), Virtual Conference, Feb 2022
3. **Alec Lu**, Zhenman Fang, Weihua Liu, Lesley Shannon, "*Demystifying Memory System of Modern Datacenter FPGAs for Software Programmers through Microbenchmarking*", The 29th ACM/SIGDA Int'l Symp. On Field-Programmable Gate Arrays (FPGA 2021), Virtual Conference, Feb 2021
2. **Alec Lu**, Zhenman Fang, Nazanin Farahpour, Lesley Shannon, "*CHIP-KNN: A Configurable and High-Performance K-Nearest Neighbors Accelerator on Cloud FPGA*", 2019 IEEE Int'l Conf. On Field-Programmable Technology (FPT 2020), Virtual Conference, Dec 2020
1. Eric Matthews, **Alec Lu**, Lesley Shannon, Zhenman Fang, "*Rethinking Integer Divider Design for FPGA-based Soft-Processors*", The 27th IEEE Int'l Symp. On Field-Programmable Custom Computing Machines (FCCM 2019), San Diego CA, pp. 289-291. Apr 2019

Published Journal Articles

2. **Alec Lu**, Zhenman Fang, Lesley Shannon, "*Demystifying the Soft and Hardened Memory Systems of Modern FPGAs for Software Programmers through Microbenchmarking*", ACM Trans. Reconfig. Technol. Syst. (TRETS 2021), 2021
1. Eric Matthews, **Alec Lu**, Lesley Shannon, Zhenman Fang, "*QuickDiv: Rethinking Integer Divider Design for FPGA-based Soft-Processors*", ACM Trans. Reconfig. Technol. Syst. (TRETS 2021), 2021

Open-Source Projects

uBench – https://github.com/SFU-HiAccel/uBench

- A suite of HLS-C/C++ microbenchmarks to evaluate the effective bandwidth, latency, and resource usage of the off-chip memory access and the accelerator-to-accelerator streaming on modern datacenter and embedded FPGAs

CHIP-KNN – https://github.com/SFU-HiAccel/CHIP-KNN

- An automated framework for configuring and generating high-performance K-Nearest Neighbors accelerators that can best utilize the off-chip memory bandwidth on cloud FPGAs.

Quick-Div – https://gitlab.com/sfu-rcl/Taiga

- A high-performance, data-dependent, variable-latency integer divider. It is designed in SystemVerilog and has been fully integrated with an FPGA RISC-V soft-processor, Taiga.

Skills

Experience in Software Engineering, RTL Design, and SW-HW Co-design

- Programming Languages: **C/C++, Python, Scala**
- Hardware Design Technologies: **SystemVerilog, Xilinx Vitis HLS, Vivado**