

## Thin Films: Sputtering Systems (Jaeger Ch 6 & Ruska Ch 7,)

- Can deposit any material on any substrate (in principal)
- Start with pumping down to high vacuum  $\sim 10^{-7}$  torr  
Removes residual gases eg oxygen from reaction
- Involves the creation of a plasma ie an ionized gas
- Start by backfilling chamber with the gas to ionize
- In sputtering use usually use inert gas: Argon (Ar)  
Hence no reaction with materials
- For plasma must have gas at moderate vacuum  
 $10^{-1}$  to  $10^{-3}$  torr
- Apply voltage injects current in gas to create + ionization  
either DC or AC (radio frequency)
- Plasma in electrode space undergoes "negative glow" discharge  
equal numbers of ions and electrons

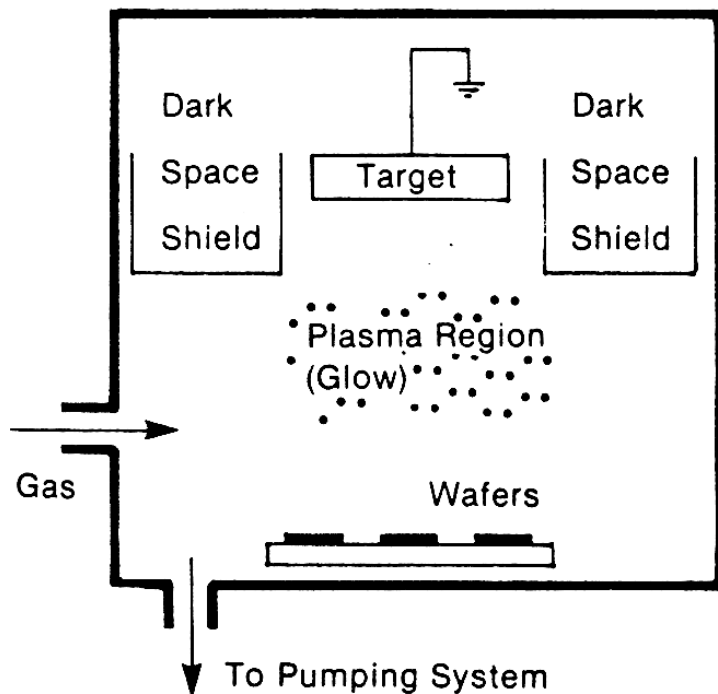


Figure 13.17 Typical sputtering equipment.

## General Sputtering Process

- Positive Ar ions move to cathode (negative electrode)
- Accelerated by voltage, gain energy
- $\text{Ar}^+$  ion hits target: knocks off target atom/molecule  
momentum transfer: Called sputtering
- Target atom then lands on substrate (wafer)
- Since momentum transfer does not heat target  
Thus no decomposition of target or substrate

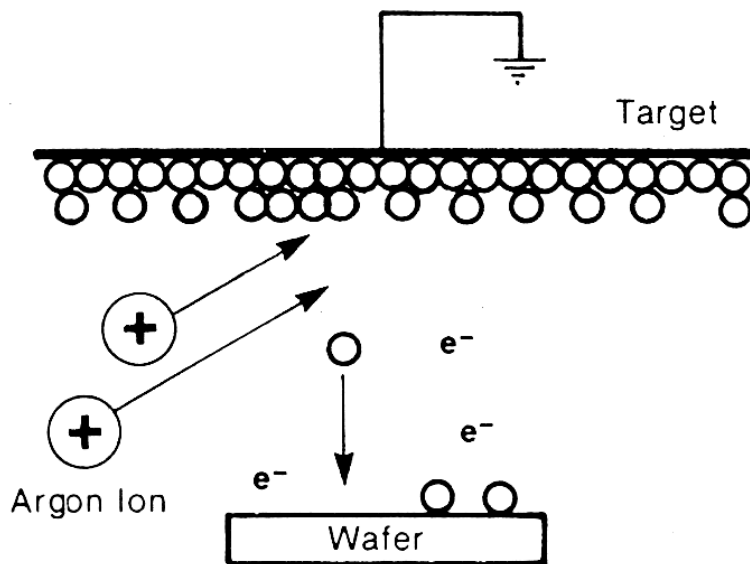
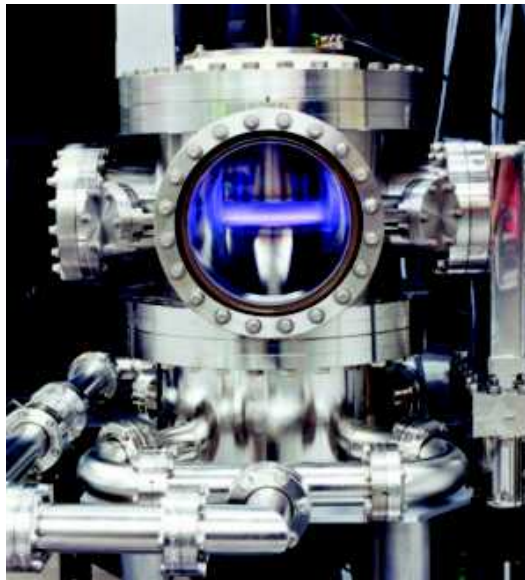


Figure 13.16 Principle of sputtering.



## Sputtering Deposition

- Sputtered atom 10 - 40 eV: velocity  $3-6 \times 10^3$  m/sec
- Mean free path 1 cm at typical 5 mTorr pressure
- Wafer spaced 5 - 10 cm apart

### Sputtered Atoms

- May undergo collisions: energy reduced to 1-2 eV
- Creates the film when hits the substrate
- May backscatter (reflect back) onto target or chamber
- Loss all energy and "thermalize" so drift around chamber
- Problem – then can coat chamber walls and other wafers

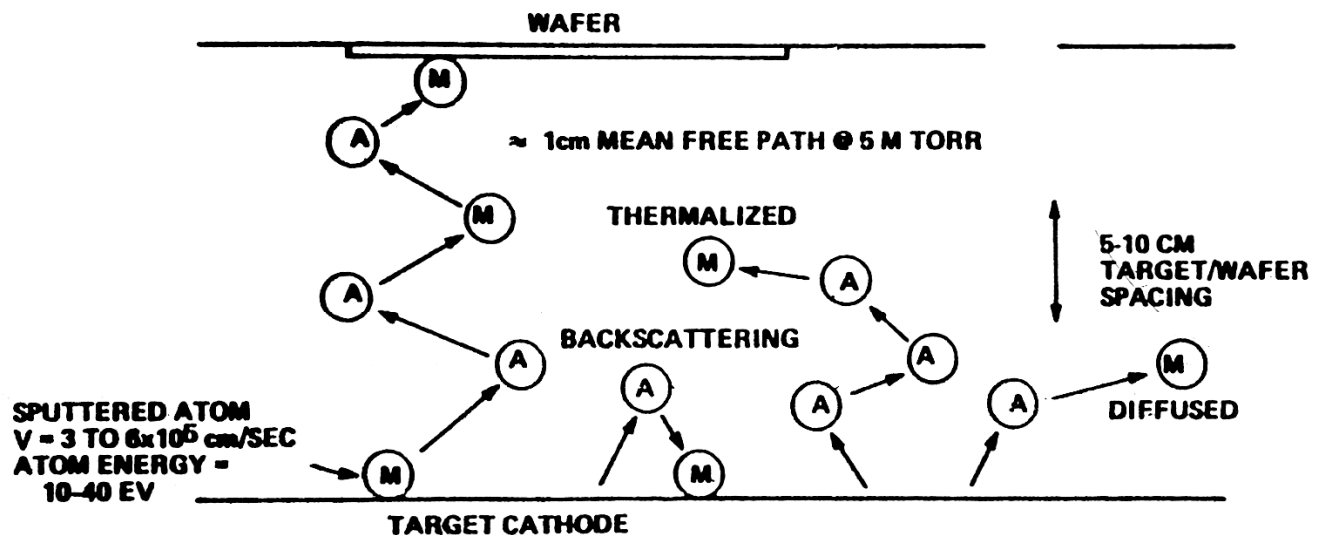
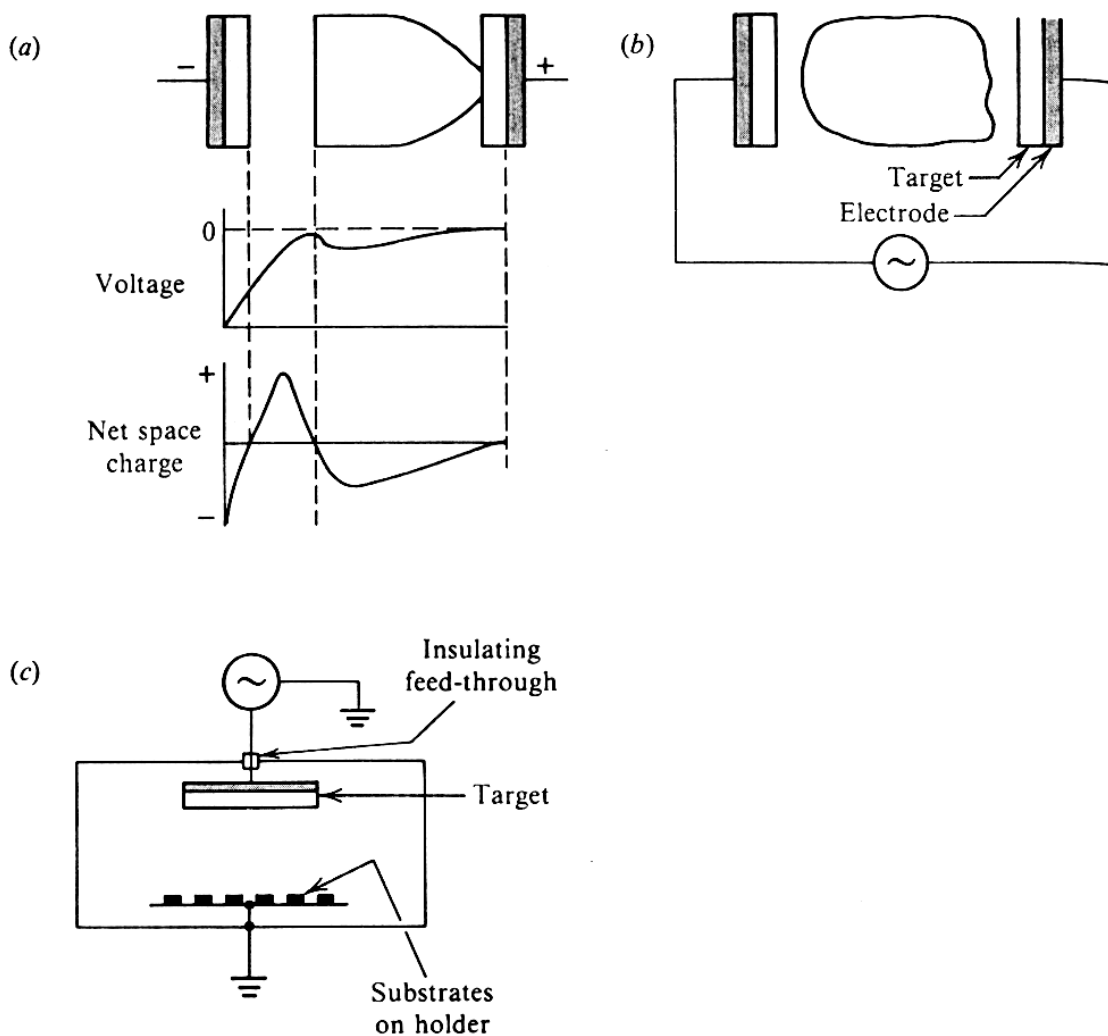


Fig. 12 Gas scattering events.

## DC Sputtering

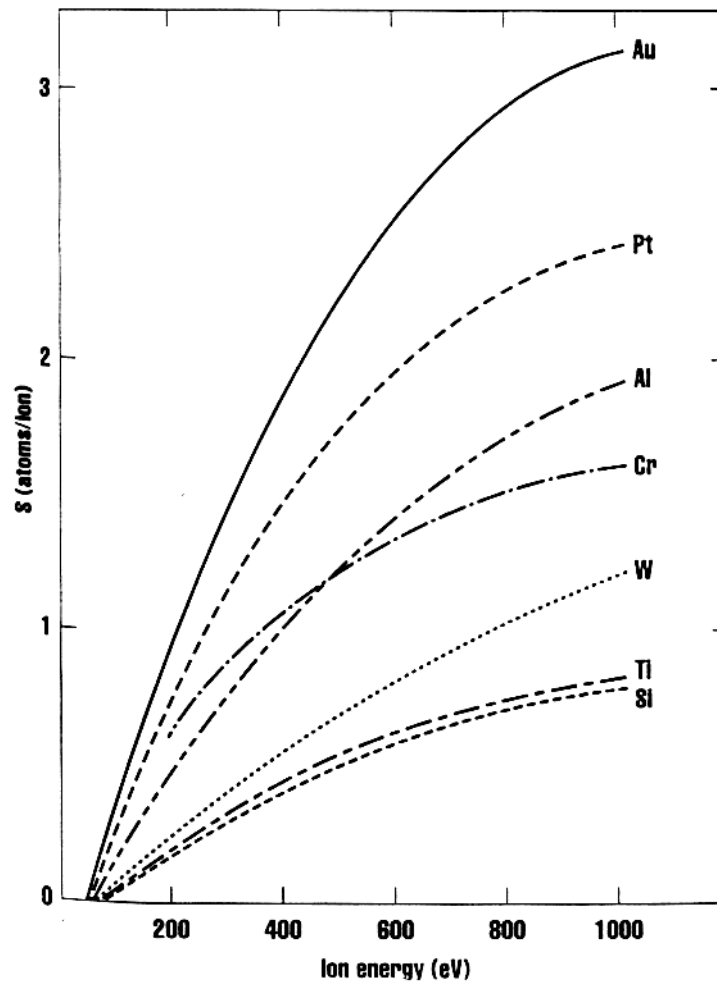
- Simplest is DC – get mostly a negative glow discharge nearly uniform voltage
- Near cathode get "cathode dark space"  
shortage of e, surplus of ions, large E field
- Near cathode get surplus of secondary electrons generated by impact on target
- DC sputtering requires conductive targets  
eg aluminum, metals etc.
- Sputtering enables alloy deposition eg AlSiCu
- DC best for conductive targets (eg metals)



**Figure 7-5** Methods of sputter deposition. (a) A dc discharge, showing cathode dark space and negative glow along with charge and voltage distributions. (After Ref. 3, used by permission.) (b) A symmetrical dc discharge. (c) A practical sputtering configuration including a target electrode and a substrate holder. (d)

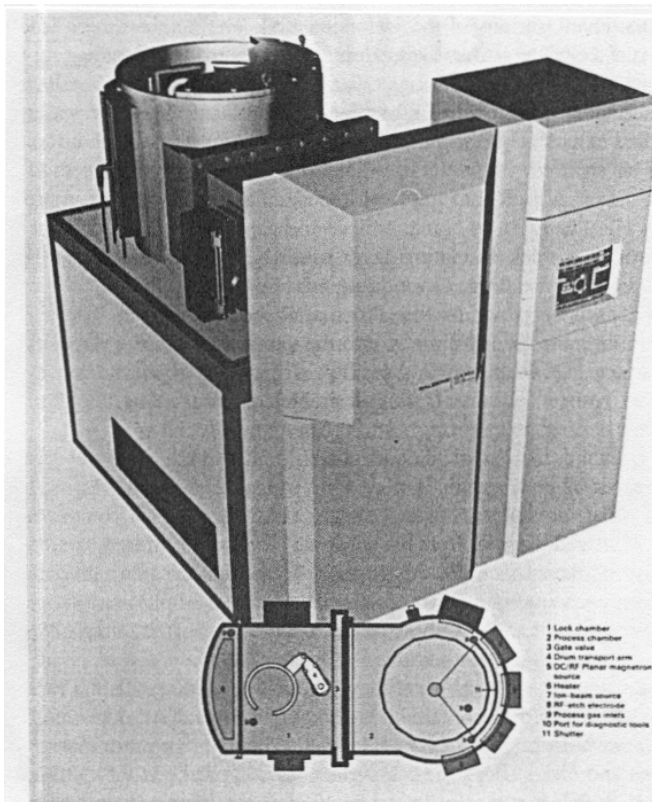
## Sputtering Deposition Rate

- Below threshold energy (10-30 eV) no sputtering
- Measure the sputter yield  $S$ :  
$$S = (\text{no. target ions released}) / (\text{no. incident ions})$$
- $S$  depends on material, ion type, and ion energy

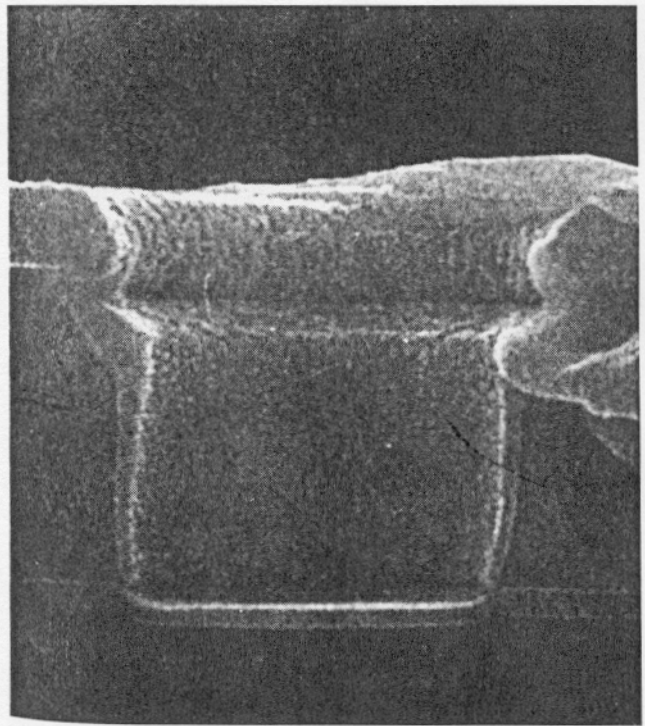


## Commercial Sputter Machine

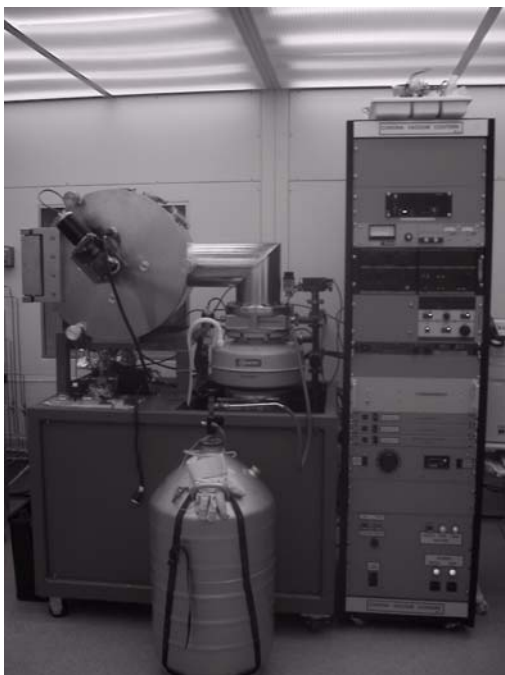
- Sputter machine cost \$100,000 (lab) - \$1,000,000 (production)



**Figure 12-24** Photograph and schematic of a commercial sputtering system used for silicon IC fabrication (courtesy Balzers).



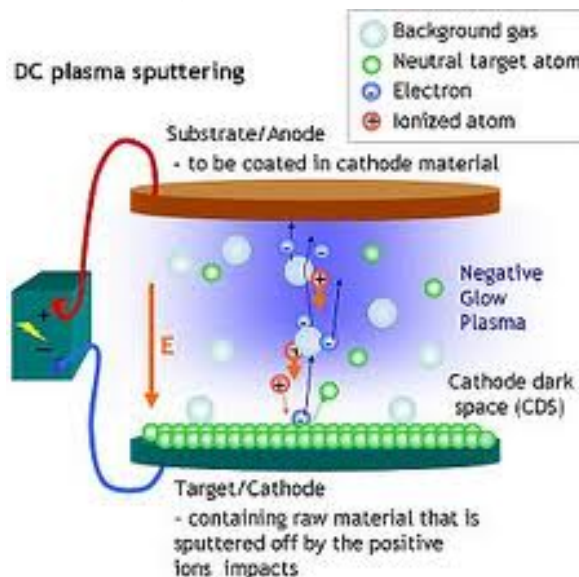
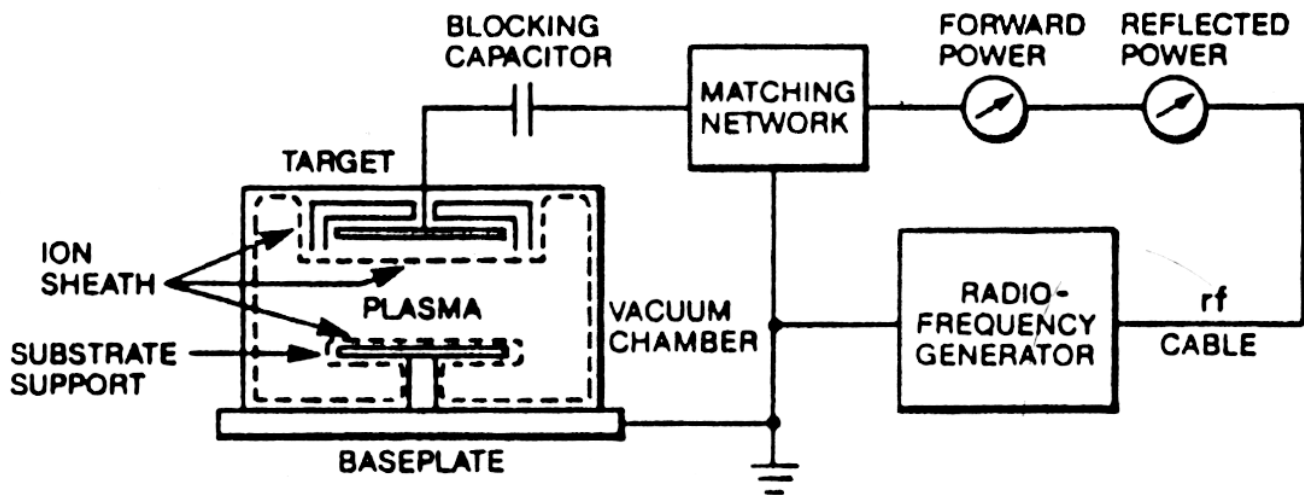
**Figure 12-27** Cross section electron micrograph of a high aspect ratio contact that has been sputter deposited with TiN (after Kohlase, Mändl, and Pamler, reprinted by permission, AIP).



SFU Corona Sputter

## AC Sputtering

- Creates the plasma using Radio Frequency (microwave) radiation
- Thus can sputter either conductors or insulators  
ie glass, ceramics
- RF sputtering will remove material from target and substrate
- Use 13.56 MHz RF:  
international agreed band so no radio interference there
- Use impedance matching network to get most power to plasma
- Usually much slower than DC so use when needed



## Sputtering Deposition Flux

- Sputtering rate depends on ion flux to target
- In DC plasma ion flux  $J$  follows Child-Langmuir equation

$$J = \frac{kV^{\frac{3}{2}}}{\sqrt{m_{ion}} D^2}$$

where  $V$  = voltage difference target to wafer

$D$  = dark space thickness

$m_{ion}$  = ion mass

$K$  = constant

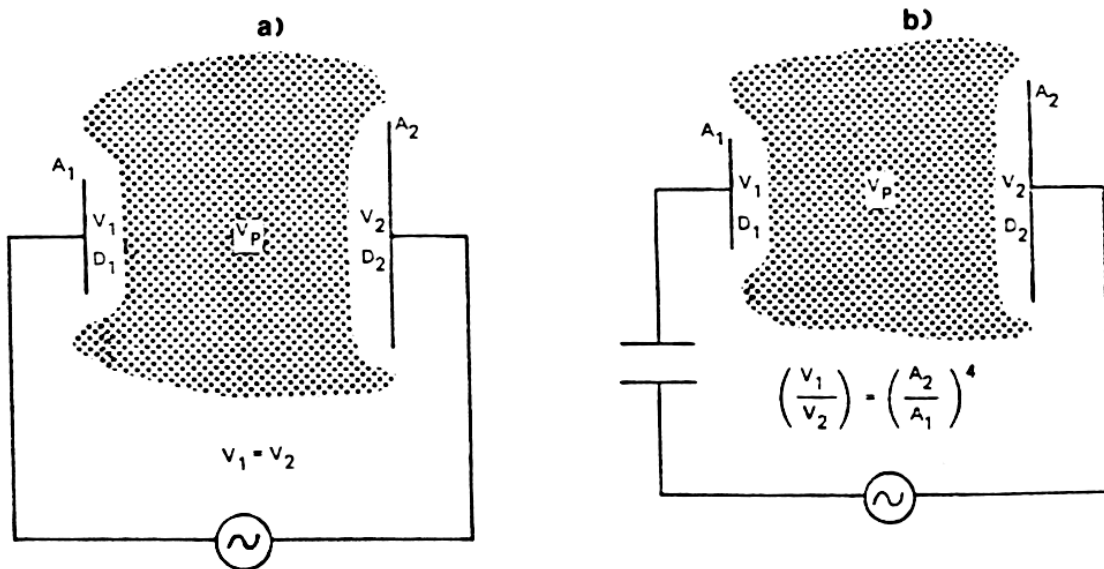
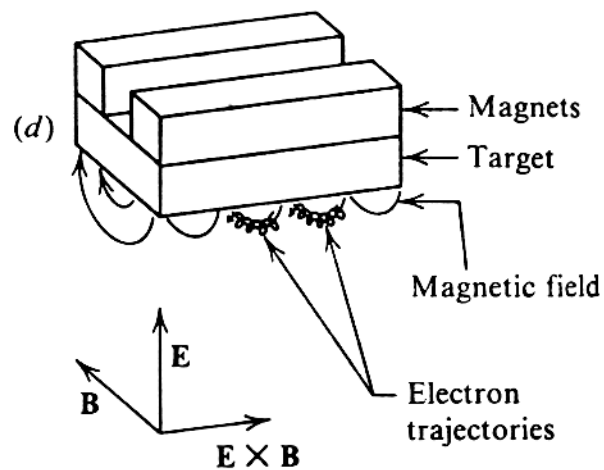


Fig. 18 (a) Voltage distribution with equal area electrodes and no blocking capacitor. Voltage distribution with unequal area electrodes and blocking capacitor<sup>10</sup>. Copyright 1970 International Business Machines Corporation; reprinted with permission.



## Magnetron Sputtering

- DC & RF sputtering:  
secondary electrons do not ionize Ar atoms
- Thus lower ion bombardment & sputter rate
- Solution Magnetron Sputtering
- Magnetic field confines e near target
- Creates more collisions & ionization
- Current goes from 1 mA/cm<sup>2</sup> (DC) to 10-100 mA/cm<sup>2</sup> (mag)



Magnetron sputtering: A magnetic field lengthens electron trajectories for greater ionization efficiency.

## Effects at Substrate

- Mostly target sputtered atoms land at substrate
- But also other species
- Fast neutral sputter gas: strike surface at high speed  
Gas collects in sputtered film
- Negative Ions: formed near cathode by secondary electrons  
usually impurity gases: N and O
- High energy Electrons: cause substrate heating
- Low energy neutral sputter gas: do not stick to film
- Contaminants from residual gas (Oxygen worse)
- X-ray damage from target

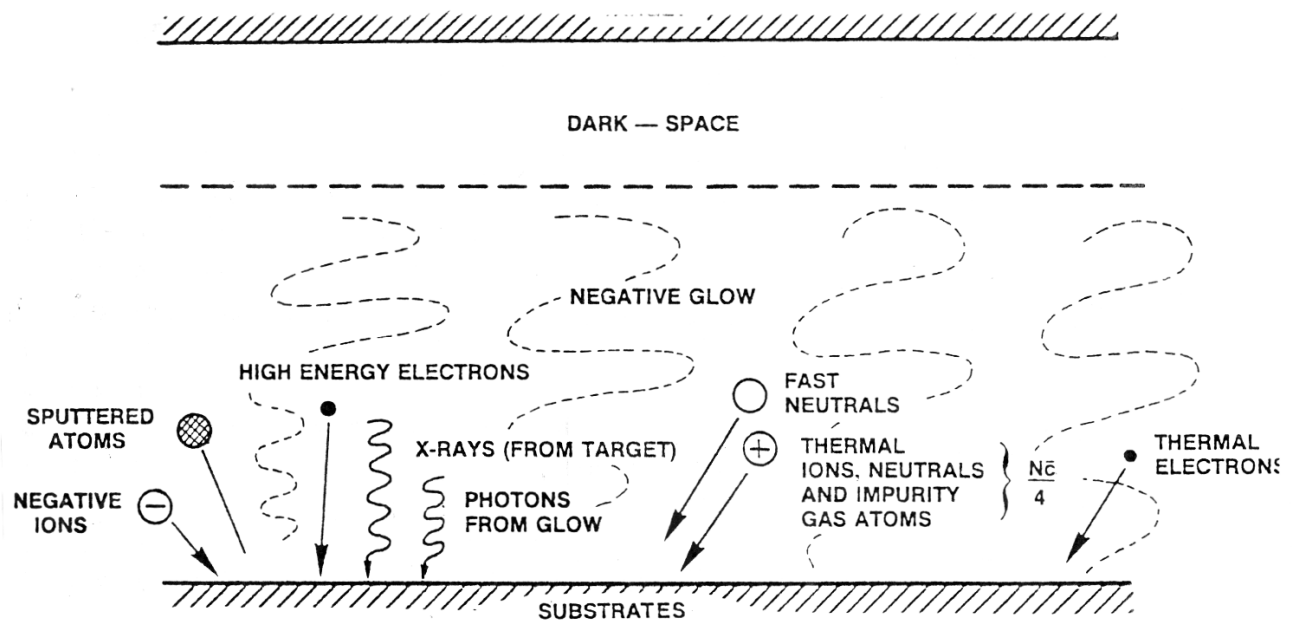


Fig. 13 Species arriving at the substrate in a sputtering system.

## Molecular Beam Processes

- Used to create complex thin layers
- Highly used in III-V compounds
- Have an many e-guns hitting many separate sources
- Control relative composition by separate rates
- Can put down monolayers of different compositions
- used in complex microwave and electro-optic devices

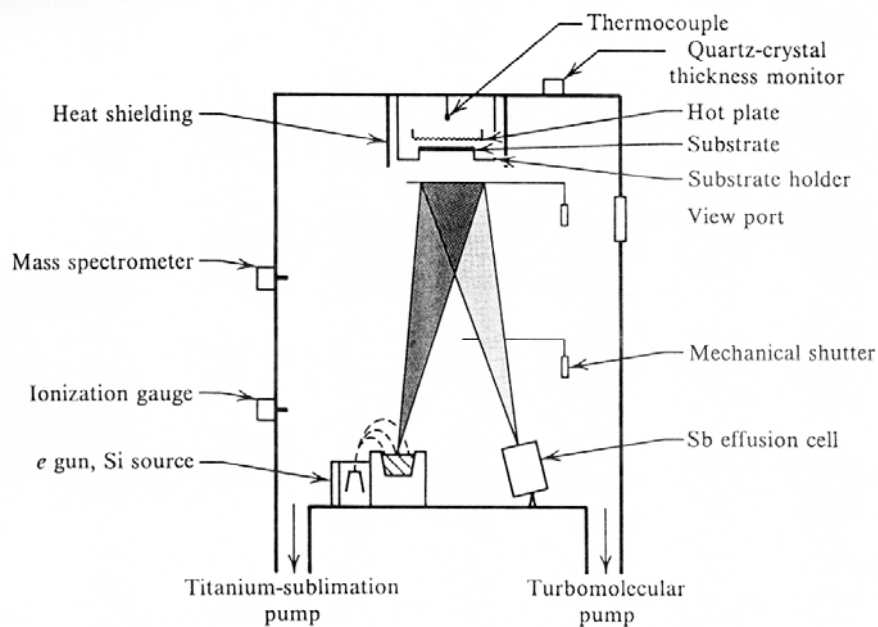
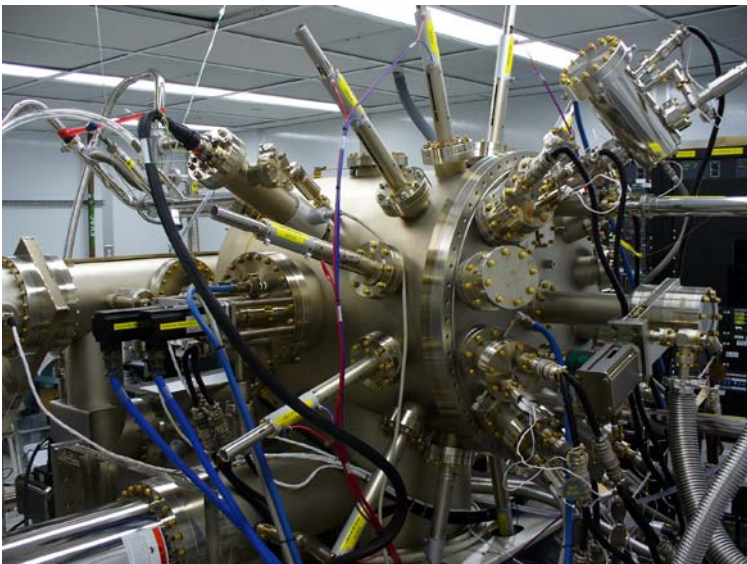


Figure 8-11 An apparatus for molecular-beam epitaxy. (Reference 19. Used by permission.)



## Conductor Usage in Typical IC's

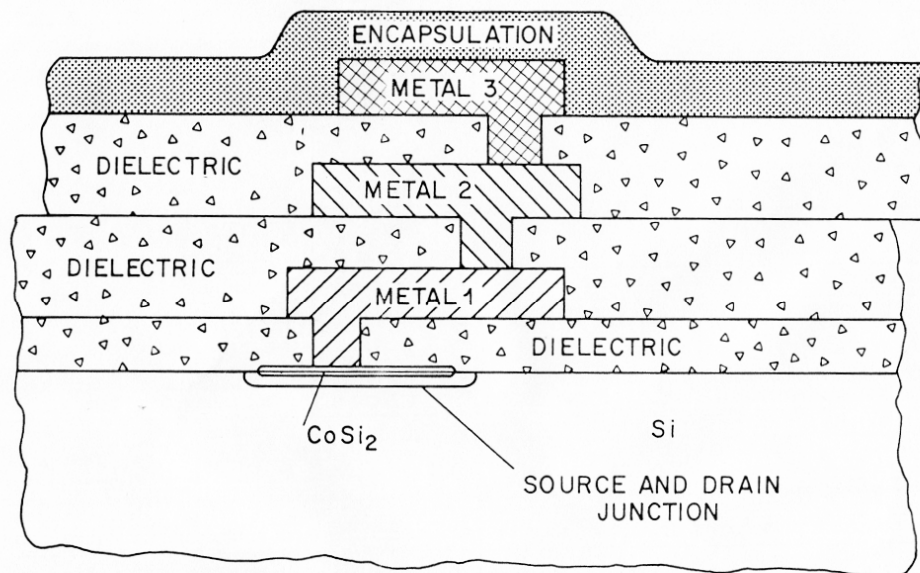
- Originally Al alloys and Poly Si
- Now much more complex alloys
- Metal conductors are mostly sputter deposited
- Reason is uniformity and use of complex alloys eg AlSiCu
- Most recent move to materials like copper

**TABLE 2**  
**Possible metallization choices for integrated circuits**

Application	Choices
Gates and interconnection and contacts	Polysilicon, silicides, nitrides, carbides, borides, refractory metals, aluminum, and combinations of two or more of above
Diffusion barrier	Nitrides, carbides, borides, Ti-W alloy, silicides
Top level	Aluminum
Selectively formed metallization on silicon only	Some silicides, tungsten, aluminum

## Multilayer Metallization Structure

- Common processes 3 or 4 metal layers + 2 poly layers
- Most advance 6-8 metal layers
- Problems with topology as layers added
- Upper layers often power
- Contact Cuts: 1<sup>st</sup> metal or Poly to substrate connections
- Vias: connections between different conducting layers.



**FIGURE 17**

A schematic drawing of a multilevel metallization structure.

## Electromigration

- Al can carry very high currents: 1 mA in 5 micron line
- Electromigration: movement of conductors due to current
- Major limit in current carrying capacity
  - Heating limit more than 10 times greater
- Electron "Wind" carries atoms with it
- Effect strongly affect by temperature
  - in an Arrhenius formula
- Measure the Mean Time to Failure (MTF)

$$MTF = \frac{K_e z x}{J^2} \exp\left(\frac{E_a}{kT}\right)$$

where  $E_a$  = activation energy

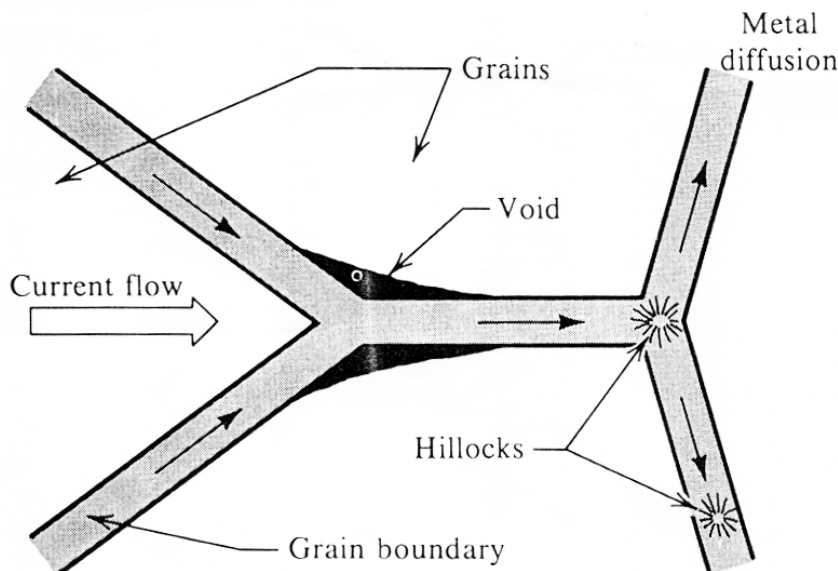
$J$  = current density

$K_e$  = empirical constant

$kT$  = thermal energy

$x$  = film width

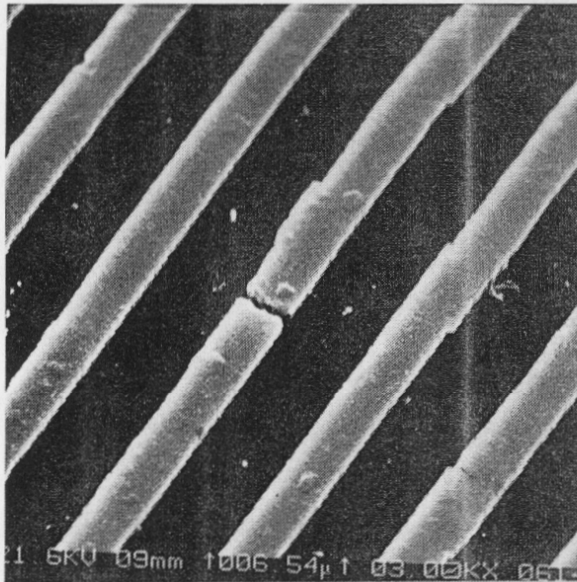
$z$  = film thickness



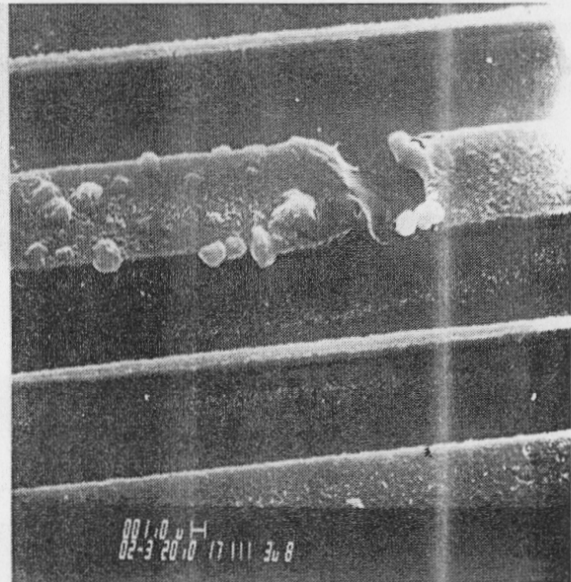
**Figure 7-6** The initial step in failure of a metallization stripe due to electromigration. Aluminum flow under the influence of current along grain boundaries, moving faster where the boundaries are parallel to the current flow. Voids are produced upstream of the fast flow region; hillocks, downstream.

## SEM of Electromigration Failures

- May see breaks in SEM on straight lines
- However breaks at metal steps: metal is thinnest there & J max  
Hard to see in SEM
- Addition of Copper to Al reduces the electromigration
- Hence use AlSiCu alloy (Si to suppress Si contact)
- Addition of TiW (Titanium, Tungsten) layers to Al now reduces electromigration



(a)



(b)

**FIGURE 13**

SEM micrographs of electromigration failure in aluminum runners, for (a) S-gun magnetron-deposited Al-0.5% Cu alloy and (b) In-source-evaporated Al-0.5% Cu alloy. (From Vaidya, Fraser, and Sinha, Ref. 38.)

## Metallizations now in Use

- Silicides (Metal:Si) done on poly Si  
decrease poly resistance: increases circuit speed

**TABLE 3**  
**Properties of various metallizations**

Metal or alloy	$\rho^a$ ( $\mu\Omega\text{-cm}$ )	$T_m^b$ ( $^{\circ}\text{C}$ )	$\alpha^c$ (ppm/ $^{\circ}\text{C}$ )	Reaction with Si at ( $^{\circ}\text{C}$ )	Stable on Si up to ( $^{\circ}\text{C}$ )
Al	2.7–3.0	660		$\sim 250$	$\sim 250$
Mo	6–15	2620	5	400–700	$\sim 400$
W	6–15	3410	4.5	600–700	$\sim 600$
MoSi <sub>2</sub>	40–100	1980	8.25	—	$> 1000$
TaSi <sub>2</sub>	38–50	$\sim 2200$	8.8–10.7	—	$\geq 1000$
TiSi <sub>2</sub>	13–16	1540	12.5	—	$\geq 950$
WSi <sub>2</sub>	30–70	2165	6.25, 7.9	—	$\geq 1000$
CoSi <sub>2</sub>	10–18	1326	10.14	—	$\leq 950$
NiSi <sub>2</sub>	$\sim 50$	993	12.06	—	$\leq 850$
PtSi	28–35	1229	—	—	$\leq 750$
Pt <sub>2</sub> Si	30–35	1398	—	—	$\leq 700$
HfN	30–100	$\sim 3000$		450–500	450
ZrN	20–100	2980		450–500	450
TiN	40–150	2950		450–500	450
TaN	$\sim 200$	3087		450–500	450
NbN	$\sim 50$	2300		450–500	450
TiC	$\sim 100$	3257		450–500	450
TaC	$\sim 100$	3985		—	—
TiB <sub>2</sub>	6–10			$> 600$	$> 600$

<sup>a</sup> $\rho$  = resistivity, typical thin film value.

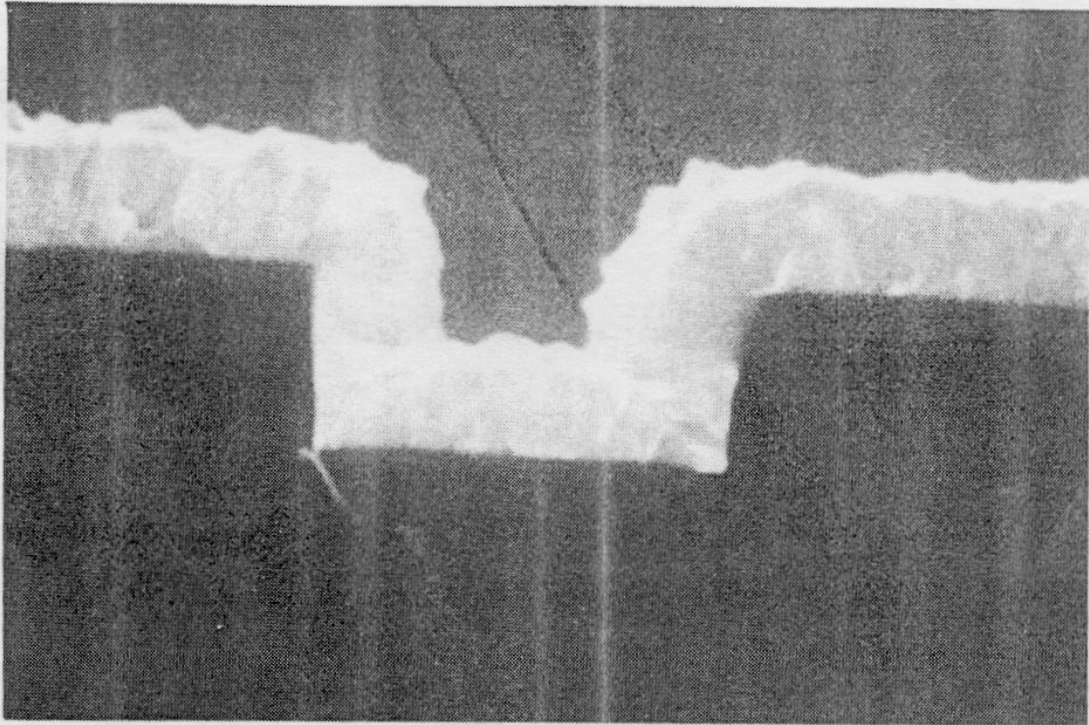
<sup>b</sup> $T_m$  = melting point.

<sup>c</sup> $\alpha$  = linear thermal expansion coefficient from Refs. 20 and 21.



## Other Metals

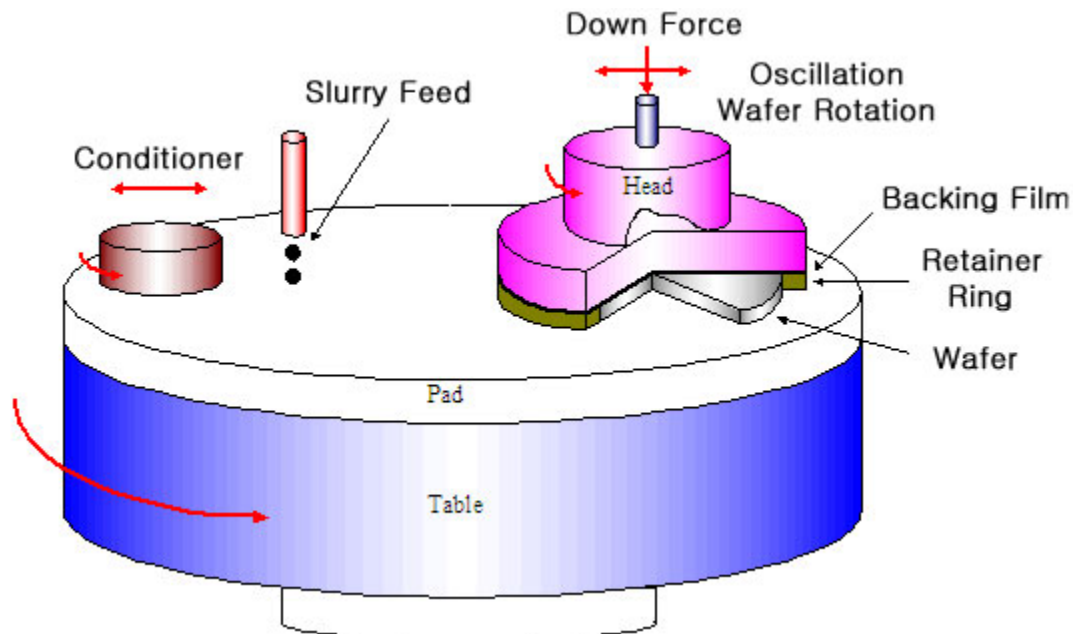
- Harder to deposit
- Rougher surface
- Harder to etch
- But more heat resistant than Al
- eg Tungsten (W)



An SEM photograph of a blanket deposited W film. Courtesy of Genus

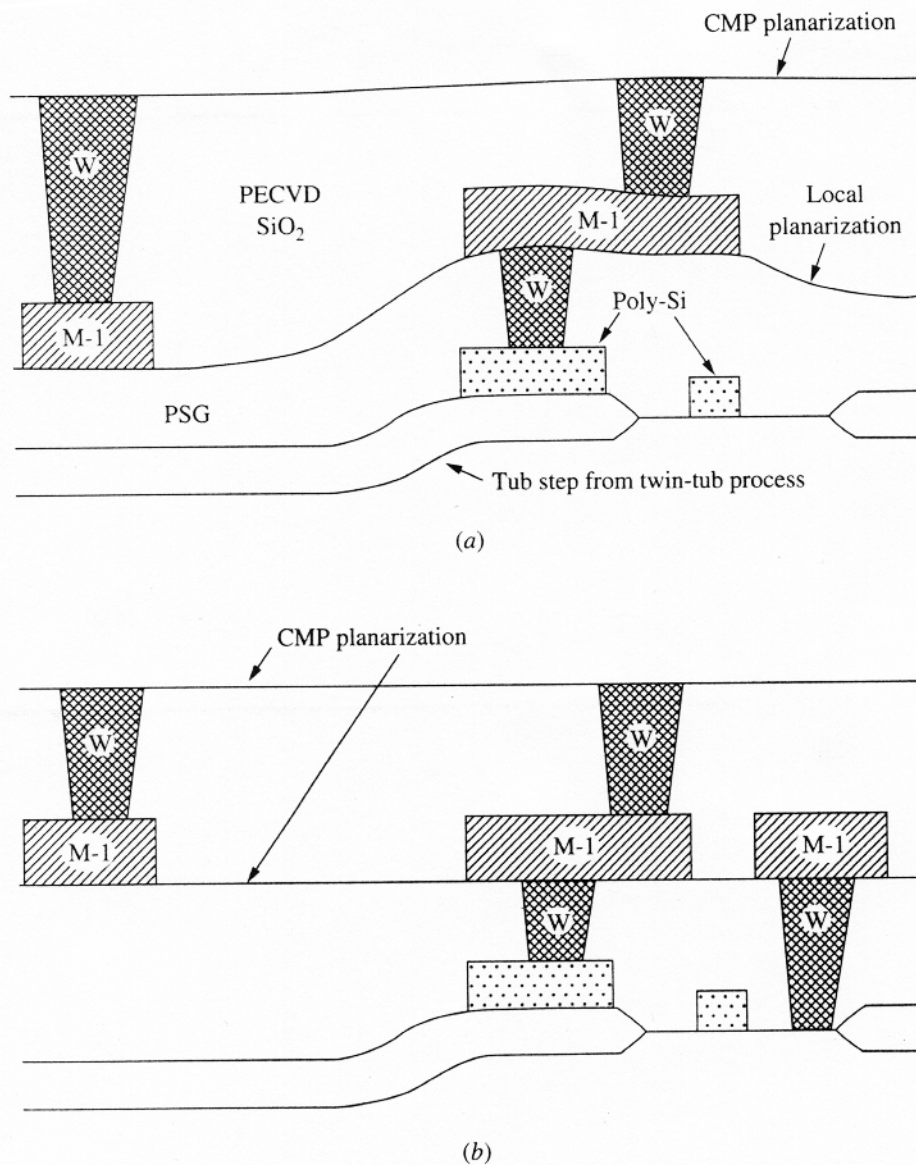
## Chemical Mechanical Polishing (CMP)

- Newest method to get wafer planarization
- As build up structure get topology
- Use Mechanical polishing to remove
- Combinations of grit and water
- Smooth to planer surface



## CMP and Metalization

- With CMP deposit Inter Layer Dielectrics (ILD)
- CMP until level
- Open vias and deposit metal plugs (Tungsten - W)
- CMP polish until plug is flush with ILD
- Deposit next metal
- Called Dual Damascene process

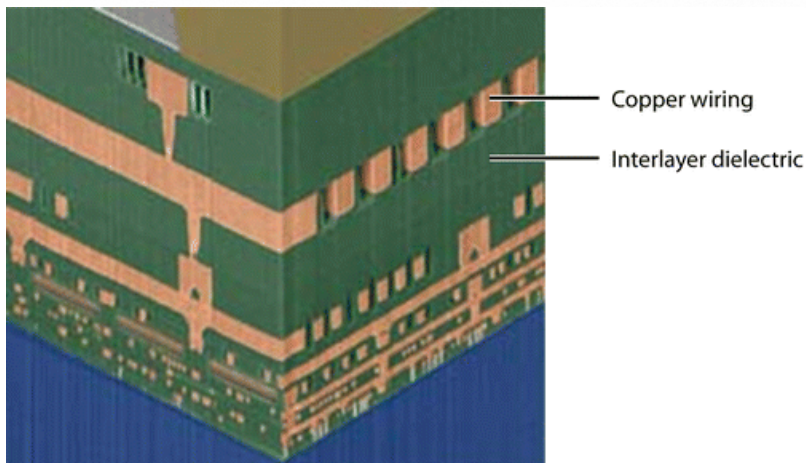
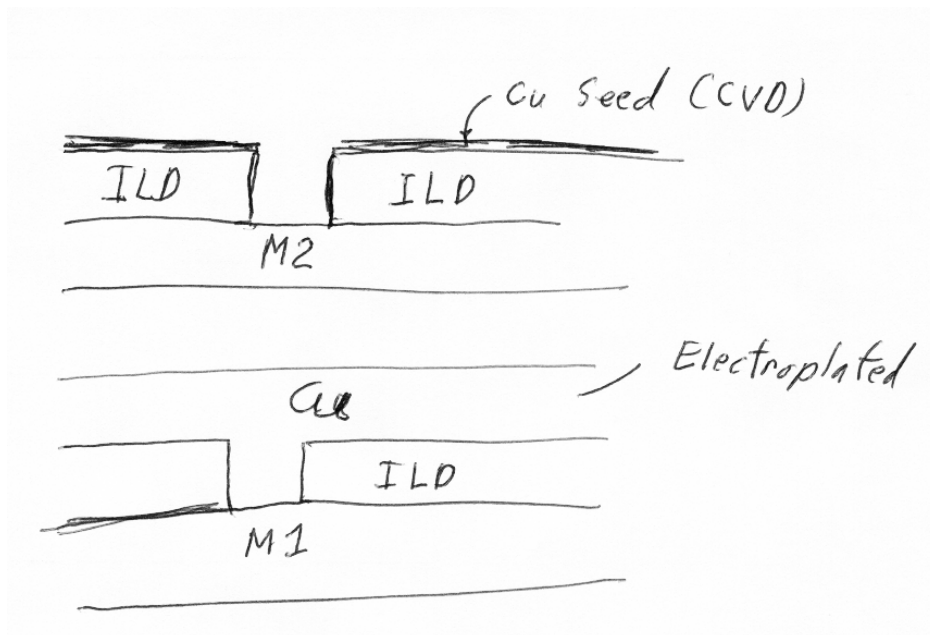


**FIGURE 46**

Via depth differences by different planarization approaches: (a) Large difference in via depths when CMP is used after local planarization; (b) vias of similar depth when CMP is used twice.

## Copper Conductors

- Copper deadly poison but high conductivity
- Forms traps in Si and has high diffusion coefficient
- IBM developed Cu process
- First Interlayer Dielectric is special Cu diffusion barrier
- Typically silicon nitride
- CVD deposit thin copper layer
- Acts as seed to Copper electroplating
- Done in wet Cu solution
- Then use CMP to planerize





## Metal Thickness Measurements: Profilometers

- Cannot measure metals with interference
- Use profileometers: mechanical stylus diamond tipped
- Stylus dragged over surface: pizoresistance measures change
- Can see 10 nm or less: must adjust force if measure resist
- Example: KLA Tencor Alpha Step 500 in lab

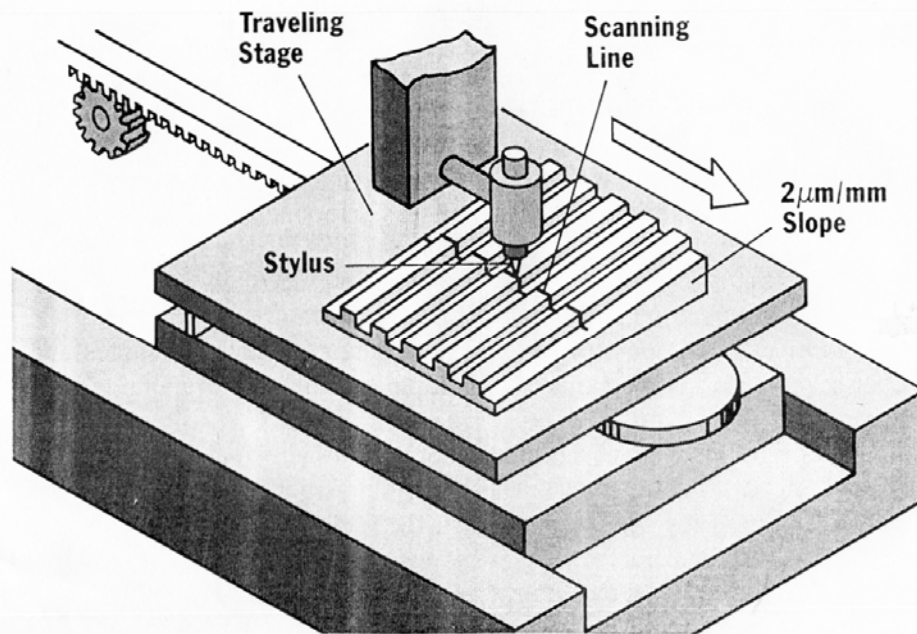


Fig. 43 Schematic drawing of a surface profilometer. Courtesy of Sloan Technology Corporation



Alpha-Step 500  
Profilometer

## Silicides in CMOS

- Silicide on Gates: reduce resistance
- Also in contact cuts  
reduces spiking (often Moly:Si used there)

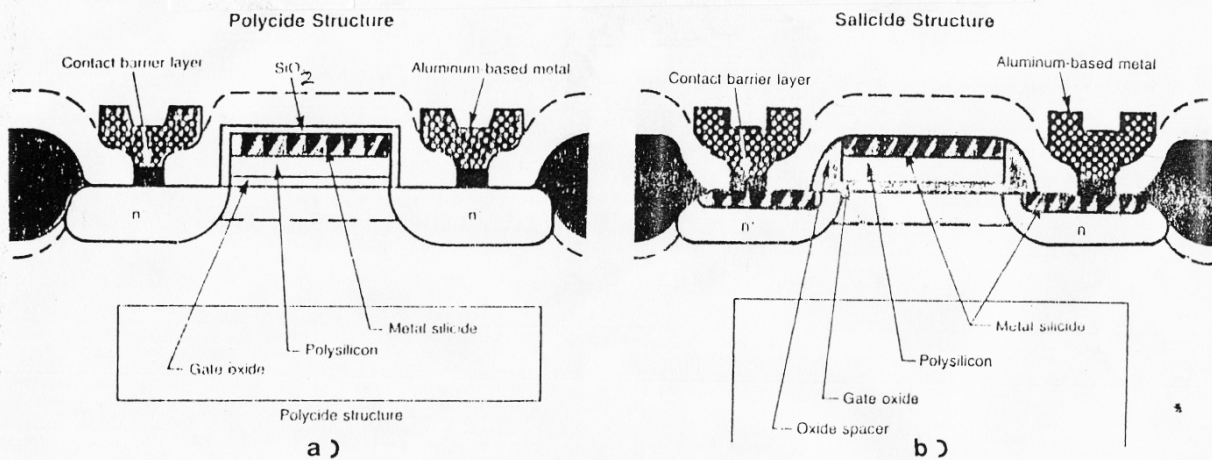


Fig. 2 (a) Polycide, and (b) Salicide structure. Reprinted by permission Semiconductor Internatl.

## Silicide Requirements for VLSI

- Silicides on poly are used in all  $<0.3$  micron processes

Table 1. SILICIDE MATERIAL PROPERTY REQUIREMENTS FOR VLSI<sup>2</sup>

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- Low Electrical Resistivity	- Stable Contact Formation to Aluminum Metallization
- Ease of Formation	- Excellent Adhesion and Low Stress
- Ease of Fine Line Pattern Transfer	- Good Electromigration Resistance
- Controlled Oxidation Properties and Stability in an Oxidizing Ambient	- Ohmic and Low Contact Resistance
- High Temperature Stability	- Stability throughout Subsequent high-temperature Processing, including Ion Implant and Diffusion
- Smooth Surface Features	
- Good Corrosion Resistance	

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properties and preparation of silicides and refractory metals for VLSI applications, including some new data that has been reported since the time Murarka's text was published.

## Silicide Formation

- 6 different methods of Silicide format
- Direct Metal reaction, Sputtering, and CVD the best

**Table 3. METHODS OF SILICIDE FORMATION**

Method of Formation	Advantages	Disadvantages
Direct Metallurgical Reaction. $M + xSi \Rightarrow MSi_x$ Metal deposited by evaporation, sputter, or CVD.	Both polycide and salicide structure can be formed. Selective etch possible.	$[M] / [Si]$ depends on phase formed. Sensitive to sintering environment. Rough surface.
Co-evaporation from an Independent Si and M Source.	Smooth surface. Sintering environment not as critical	$[M] / [Si]$ control difficult but possible. No selective etch possible. Poor step coverage.
Co-sputtering from Independent Si and M Targets.	Good control of $[M] / [Si]$ . Smooth films. Sintering environment not as critical. Deposition of sandwich possible.	Difficult calibration to achieve $[M] / [Si]$ control.
Sputtering from a Composite $MSi_x$ Target.	Excellent $[M] / [Si]$ control if correct target chosen. Good step coverage.	Contamination from Target.
Chemical Vapor Deposition: atmospheric, low-pressure, or plasma-enhanced.	High throughput. Excellent step coverage.	Rough surface. $[M] / [Si]$ control difficult but possible. Possible poor adhesion.



## Process Steps for Silicides

- Deposit poly, then poly sidewall protection/spacer
- Deposit metal & react to form silicide  
Note there is a separate mask for silicide location
- Remove non reacted metal

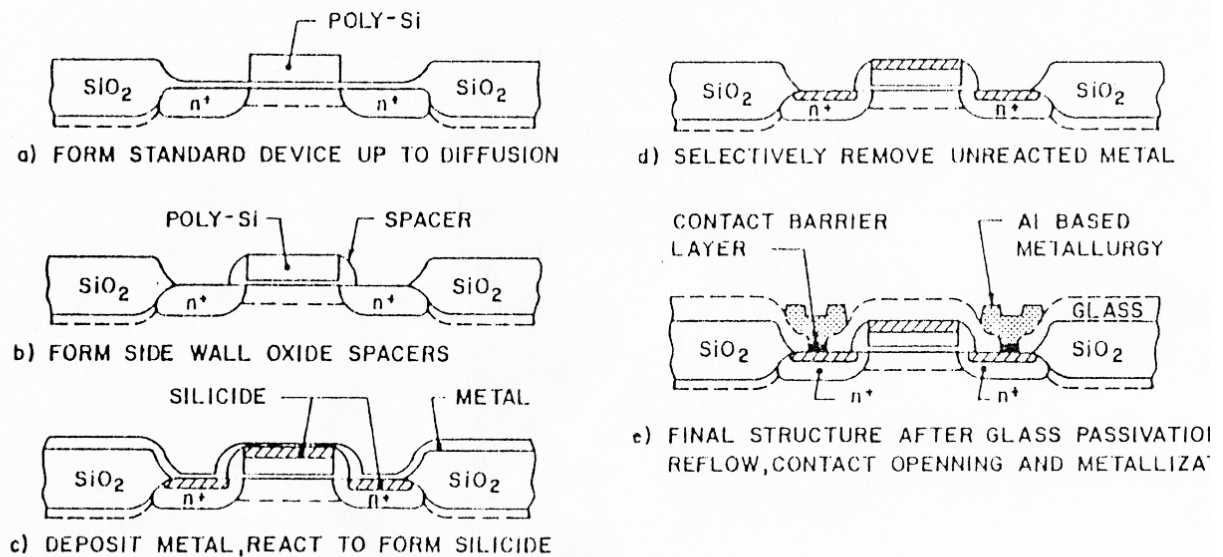


Fig. 13 Silicide process flow and final structure. <sup>28</sup>. (© 1985 IEEE. )

## Resistivity of Silicides

- Note: Al is 2.6 micro-ohm cm
- Silicides 4-30 times worse
- But still ~10-100 lower resistance than poly
- Hence circuits faster

**Table 2. Resistivity of Silicide Films Annealed at  $\leq 1000^{\circ}\text{C}$  (in  $\mu\Omega\text{-cm}$ ).**

Material	Metal + Poly-Si	Metal + Si Crystal	Co-Sputter	Co-Evaporation	CVD
TiSi <sub>2</sub>	13	15	25	21	21
TaSi <sub>2</sub>	35		50		38
MoSi <sub>2</sub>	90	15	100	40	120
WSi <sub>2</sub>			70	30	40
PtSi	28		35		

## Properties of Silicides

- Silicides much higher melting but higher thermal conduction
- Still allows higher temperature operation

Table 5. PROPERTIES OF SILICIDES AND REFRACTORY METALS

Material	Melting Point (°C)	Resistivity ( $\mu\Omega$ -cm)	Thermal Coefficient of Expansion ( $10^{-6}/^{\circ}\text{C}$ )
Si	1420	500 (heavily doped poly)	3.0
TiSi <sub>2</sub>	1540	13-17	10.5
MoSi <sub>2</sub>	1870	22-100	8.2
TaSi <sub>2</sub>	2400	8-45	8.8
WSi <sub>2</sub>	2050	14-17	6.2
Ti	1690	43-47	8.5
Mo	2620	5	5.0
Ta	2996	13-16	6.5
W	3382	5.3	4.5