Thin Films: Sputtering Systems
(Jaeger Ch 6 & Ruska Ch 7,)

- Sputtering: gas plasma transfers atoms from target to substrate
- Can deposit any material on any substrate (in principal)
- Start with pumping down to high vacuum $\sim 10^{-7}$ torr
  - Removes residual gases eg oxygen from reaction
- Sputtering involves the creation of a plasma ie an ionized gas
- Start by backfilling chamber with the gas to be ionized
- In regular sputtering use usually use inert gas: Argon (Ar)
  - Hence no reaction with materials
- For plasma must have gas at moderate vacuum $10^{-1}$ to $10^{-3}$ torr
- Applied voltage injects current in gas to create + ionization
- Use either DC or AC (radio frequency)
- Plasma in electrode space undergoes "negative glow" discharge
- Reason equal numbers of ions and electrons

![Diagram of sputtering system](image_url)

**Figure 13.17** Typical sputtering equipment.
General Sputtering Process

- Positive $\text{Ar}^+$ ions move to cathode (negative target electrode)
- Accelerated by voltage, gain energy
- $\text{Ar}^+$ ion hits target: knocks of target atom/molecule
  momentum transfer: called sputtering
- Target atom then lands on substrate (wafer)
- Since momentum transfer does not heat target much
- Thus no decomposition of target or substrate
- Clear advantage over evaporation methods
- Targets are mounted on metal holders, often water cooled

Figure 13.16  Principle of sputtering.
Sputtering Deposition

- Sputtered atom 10 - 40 eV: velocity 3-6x10³ m/sec
- Mean free path 1 cm at typical 5 mTorr pressure
- Wafer spaced 5 - 10 cm apart

Sputtered Atoms

- May undergo collisions: energy reduced to 1-2 eV
- Creates the film when hits the substrate
- May backscatter (reflect back) onto target or chamber
- Loss all energy and "thermalize" so drift around chamber
- Problem – then can coat chamber walls and other wafers

Fig. 12 Gas scattering events.
DC Sputtering

- Simplest is DC – get mostly a negative glow discharge
- Nearly uniform voltage across target
- Near cathode get "cathode dark space"
- Reason shortage of e, surplus of ions, large E field
- Also get surplus of secondary e generated by impact on target
- DC sputtering requires conductive targets: best for metals
  - eg aluminum, gold, nickel etc.
- Sputtering enables alloy deposition eg AlSiCu
- Keeps composition nearly same as target unlike evaporation

![Diagram of DC sputtering](image)

*Figure 7-5 Methods of sputter deposition. (a) A dc discharge, showing cathode dark space and negative glow along with charge and voltage distributions. (After Ref. 3, used by permission.) (b) A symmetrical dc discharge. (c) A practical sputtering configuration including a target electrode and a substrate holder. (d)*
Sputtering Deposition Rate

- Below threshold energy (~10-30 eV) no sputtering
- Above threshold sputtering rises with eV
- Eventually starts to saturate
- Measure the sputter yield S:
  \[ S = \frac{\text{no. target ions released}}{\text{no. incident ions}} \]
- S depends on material, ion type, and ion energy
Commercial Sputter Machine

- Sputter machine cost $200,000 (lab) - $2,000,000 (production)

SFU Corona Sputter
**AC Sputtering**

- Creates the plasma using Radio Frequency (microwave) radiation
- Thus can sputter either conductors or insulators ie glass, ceramics
- RF sputtering will remove material from target and substrate
- Use 13.56 MHz RF: international agreed band so no radio interference there
- Use impedance matching network to get most power to plasma
- Usually much slower than DC so use when needed
Sputtering Deposition Flux

- Sputtering rate depends on ion flux to target
- In DC plasma ion flux $J$ follows Child-Langmuir equation

$$J = \frac{kV^{\frac{3}{2}}}{\sqrt{m_{ion}D^2}}$$

where $V =$ voltage difference target to wafer
$D =$ dark space thickness
$m_{ion} =$ ion mass
$K =$ constant

Fig. 18 (a) Voltage distribution with equal area electrodes and no blocking capacitor. Voltage distribution with unequal area electrodes and blocking capacitor\textsuperscript{10}. Copyright 1970 International Business Machines Corporation; reprinted with permission.
Magnetron Sputtering

- DC & RF sputtering: secondary electrons do not ionize Ar atoms
- Thus lower ion bombardment & sputter rate
- Solution Magnetron Sputtering
- Magnetic field confines e near target
- Creates more collisions & ionization
- Current goes from 1 mA/cm$^2$ (DC) to 10-100 mA/cm$^2$ (mag)
Effects at Substrate

- Mostly target sputtered atoms land at substrate
- But also other species are accelerated
- Fast neutral sputter gas: strike surface at high speed
  Gas collects in sputtered film
- Negative Ions: formed near cathode by secondary electrons
  usually impurity gases: N and O
- High energy Electrons: cause substrate heating
- Thus may water cool substrate
- Low energy neutral sputter gas: do not stick to film
- Contaminants from residual gas (Oxygen worse)
- May react during deposition (eg oxidize sputtered metal)
- Significant problem in aluminum: creates dull, high resistance Al
- X-ray damage from target can damage wafer
- Usually need final low temperature sinter to repair damage

---

Fig. 13 Species arriving at the substrate in a sputtering system.
Molecular Beam Processes

- Used to create complex thin layers
- Highly used in III-V compounds
- Have many e-guns hitting many separate sources
- Control relative composition by separate rates
- Can put down monolayers of different compositions
- Used in complex microwave and electro-optic devices

*Figure 8-11 An apparatus for molecular-beam epitaxy. (Reference 19. Used by permission.)*
Conductor Usage in Typical IC's

- Originally Al alloys and Poly Si
- Now much more complex alloys
- Regular Metal conductors are mostly sputter deposited
- Reason is uniformity and use of complex alloys eg AlSiCu
- Most recent move to copper upper level conductors
- Combination of supper and other processes

TABLE 2
Possible metallization choices for integrated circuits

<table>
<thead>
<tr>
<th>Application</th>
<th>Choices</th>
</tr>
</thead>
<tbody>
<tr>
<td>Gates and interconnection and contacts</td>
<td>Polysilicon, silicides, nitrides, carbides, borides,</td>
</tr>
<tr>
<td></td>
<td>refractory metals, aluminum, and combinations of</td>
</tr>
<tr>
<td></td>
<td>two or more of above</td>
</tr>
<tr>
<td>Diffusion barrier</td>
<td>Nitrides, carbides, borides, Ti-W alloy, silicides</td>
</tr>
<tr>
<td>Top level</td>
<td>Aluminum</td>
</tr>
<tr>
<td>Selectively formed metallization on silicon only</td>
<td>Some silicides, tungsten, aluminum</td>
</tr>
</tbody>
</table>
**Multilayer Metallization Structure**

- Common processes 3 or 4 metal layers + 2 poly layers
- Most advanced 6-8 metal layers + poly
- Problems with topology as layers added
- Each layer pattern causes topology changes in higher layers
- Eg steps over lines or down vias.
- Upper layers often power/ground lines
- Openings are called by two names
- Contact Cuts: 1st metal or Poly to substrate connections
- Vias: connections between different conducting layers.

---

**Figure 17**

A schematic drawing of a multilevel metallization structure.
**Electromigration**

- Al can carry very high currents: 1 mA in 5 micron line
- Electromigration: movement of conductors due to current
- Major limit in current carrying capacity
  - Heating limit more than 10 times greater
- Electron "Wind" carries atoms with it
- Effect strongly affect by temperature
  - in an Arrhenius formula
- Measure the Mean Time to Failure (MTF)

\[
MTF = \frac{K_e zx}{J^2} \exp\left(\frac{E_a}{kT}\right)
\]

where \(E_a\) = activation energy

- \(J\) = current density
- \(K_e\) = empirical constant
- \(kT\) = thermal energy
- \(x\) = film width
- \(z\) = film thickness

*Figure 7-6* The initial step in failure of a metallization stripe due to electromigration. Aluminum flows under the influence of current along grain boundaries, moving faster where the boundaries are parallel to the current flow. Voids are produced upstream of the fast flow region; hillocks, downstream.
SEM of Electromigration Failures

- May see breaks in SEM on straight lines
- However breaks at metal steps: metal is thinnest there & J max Hard to see in SEM
- Addition of Copper to Al reduces the electromigration
- Hence use AlSiCu alloy (Si to suppress Si contact)
- Addition of TiW (Titanium, Tungsten) layers to Al now reduces electromigration

![SEM micrographs of electromigration failure in aluminum runners, for (a) S-gun magnetron-deposited Al–0.5% Cu alloy and (b) In-source-evaporated Al–0.5% Cu alloy. (From Vaidya, Fraser, and Sinha, Ref. 38.)](image)
Metallizations now in Use

- Silicides (Metal:Si) done on poly Si
decrease poly resistance: increases circuit speed

<table>
<thead>
<tr>
<th>Metal or alloy</th>
<th>(\rho^a) ((\mu\Omega\cdot\text{cm}))</th>
<th>(T_m^b) (°C)</th>
<th>(\alpha^c) (ppm/°C)</th>
<th>Reaction with Si at (\alpha^c) (°C)</th>
<th>Stable on Si up to (\alpha^c) (°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Al</td>
<td>2.7–3.0</td>
<td>660</td>
<td></td>
<td>~250</td>
<td>~250</td>
</tr>
<tr>
<td>Mo</td>
<td>6–15</td>
<td>2620</td>
<td>5</td>
<td>400–700</td>
<td>~400</td>
</tr>
<tr>
<td>W</td>
<td>6–15</td>
<td>3410</td>
<td>4.5</td>
<td>600–700</td>
<td>~600</td>
</tr>
<tr>
<td>MoSi₂</td>
<td>40–100</td>
<td>1980</td>
<td>8.25</td>
<td></td>
<td>&gt;1000</td>
</tr>
<tr>
<td>TaSi₂</td>
<td>38–50</td>
<td>~2200</td>
<td>8.8–10.7</td>
<td></td>
<td>≥1000</td>
</tr>
<tr>
<td>TiSi₂</td>
<td>13–16</td>
<td>1540</td>
<td>12.5</td>
<td></td>
<td>≥950</td>
</tr>
<tr>
<td>WSi₂</td>
<td>30–70</td>
<td>2165</td>
<td>6.25, 7.9</td>
<td></td>
<td>≥1000</td>
</tr>
<tr>
<td>CoSi₂</td>
<td>10–18</td>
<td>1326</td>
<td>10.14</td>
<td></td>
<td>≤950</td>
</tr>
<tr>
<td>NiSi₂</td>
<td>~50</td>
<td>993</td>
<td>12.06</td>
<td></td>
<td>≤850</td>
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<tr>
<td>PtSi</td>
<td>28–35</td>
<td>1229</td>
<td></td>
<td></td>
<td>≤750</td>
</tr>
<tr>
<td>Pt₂Si</td>
<td>30–35</td>
<td>1398</td>
<td></td>
<td></td>
<td>≤700</td>
</tr>
<tr>
<td>HiN</td>
<td>30–100</td>
<td>~3000</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>ZrN</td>
<td>20–100</td>
<td>2980</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>TiN</td>
<td>40–150</td>
<td>2950</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>TaN</td>
<td>~200</td>
<td>3087</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>NbN</td>
<td>~50</td>
<td>2300</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>TiC</td>
<td>~100</td>
<td>3257</td>
<td></td>
<td>450–500</td>
<td>450</td>
</tr>
<tr>
<td>TaC</td>
<td>~100</td>
<td>3985</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>TiB₂</td>
<td>6–10</td>
<td></td>
<td></td>
<td>&gt;600</td>
<td>&gt;600</td>
</tr>
</tbody>
</table>

\(a\) \(\rho\) = resistivity, typical thin film value.

\(b\) \(T_m\) = melting point.

\(c\) \(\alpha\) = linear thermal expansion coefficient from Refs. 20 and 21.
Metals Beyond Aluminum

- Harder to deposit but needed for special applications
- Three types
- Copper (now replacing Al – see later)
- Gold: used for III-V materials but not in silicon
- Refractory metals Tungsten (W)
- Rougher surface
- Harder to etch
- But more heat resistant than Al
- eg Tungsten (W)

An SEM photograph of a blanket deposited W film. Courtesy of Genus
Chemical Mechanical Polishing (CMP)

- Newest method to get wafer planerization
- As build up structure get topology
- Use Mechanical polishing to remove
- Combinations of grit and water
- Smooth to planer surface
CMP and Metalization

- With CMP deposit Inter Layer Dielectrics (ILD)
- CMP until level
- Open vias and deposit metal plugs (Tungsten - W)
- CMP polish until plug is flush with ILD
- Deposit next metal
- Called Dual Damascene process

**FIGURE 46**
Via depth differences by different planarization approaches: (a) Large difference in via depths when CMP is used after local planarization; (b) vias of similar depth when CMP is used twice.
Copper Conductors

- Copper deadly poison but high conductivity
- Forms traps in Si and has high diffusion coefficient
- IBM developed Cu process
- First Interlayer Dielectric is special Cu diffusion barrier
- Typically silicon nitride
- CVD deposit thin copper layer
- Acts as seed to Copper electroplating
- Done in wet Cu solution
- Then use CMP to planerize

---

Metal Thickness Measurements: Profilometers

- Cannot measure metals with optical interference
- Use profilometers: mechanical stylus diamond tipped
- Stylus dragged over surface: pizoresistance measures change
- Can see 10 nm or less: must adjust force if measure resist
- Example: KLA Tencor Alpha Step 500 in lab

Fig. 43 Schematic drawing of a surface profilometer. Courtesy of Sloan Technology Corporation

Alpha-Step 500 Profilometer
Profilometer: Resist, Metal and Oxide

- Profilometer really only useful after photolithography step
- Must find pattern with several steps
- Must bring Stylus down in contact with wafer with right force
- Also need to level the wafer (done electronically on screen)
- Two outputs: plots (basically screen prints)
- In plot place cursors at top and bottom of curves get difference
- Data file – import to excel for analysis eg roughness
Silicides in CMOS

• Problem for high speed devices: Poly Si too resistive
• With small gates hundreds of ohms.
• Large resistance means distribution of V across gate
• Slows gate charging
• Adding a Silicide: metal silicon alloy on poly Gates
• Reduce resistance >10x
• Also used in contact cuts
  reduces spiking (often Moly:Si used there)

Fig. 2 (a) Polycide, and (b) Salicide structure. Reprinted by permission Semiconductor Internatl.
Silicide Requirements for VLSI

- Silicides on poly are used in all <0.3 micron processes
- Important point: some electro-optic devices need to remove silide
- Silicide absorbs light – poly transmits
- Eg Photograte optical sensors
- Usually a mask level for patterning silicide

<table>
<thead>
<tr>
<th>Table 1. SILICIDE MATERIAL PROPERTY REQUIREMENTS FOR VLSI²</th>
</tr>
</thead>
<tbody>
<tr>
<td>- Low Electrical Resistivity</td>
</tr>
<tr>
<td>- Ease of Formation</td>
</tr>
<tr>
<td>- Ease of Fine Line Pattern Transfer</td>
</tr>
<tr>
<td>- Controlled Oxidation Properties and Stability in an Oxidizing Ambient</td>
</tr>
<tr>
<td>- High Temperature Stability</td>
</tr>
<tr>
<td>- Smooth Surface Features</td>
</tr>
<tr>
<td>- Good Corrosion Resistance</td>
</tr>
<tr>
<td>- Stable Contact Formation to Aluminum Metallization</td>
</tr>
<tr>
<td>- Excellent Adhesion and Low Stress</td>
</tr>
<tr>
<td>- Good Electromigration Resistance</td>
</tr>
<tr>
<td>- Ohmic and Low Contact Resistance</td>
</tr>
<tr>
<td>- Stability throughout Subsequent high-temperature Processing, including Ion Implant and Diffusion</td>
</tr>
</tbody>
</table>

properties and preparation of silicides and refractory metals for VLSI applications, including some new data that has been reported since the time Murarka's text was published.
**Silicide Formation**

- 6 different methods of Silicide format
- Direct Metal reaction, Sputtering, and CVD the best

<table>
<thead>
<tr>
<th>Method of Formation</th>
<th>Advantages</th>
<th>Disadvantages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Direct Metallurgical Reaction.</td>
<td>Both polycide and salicide structure can be formed.</td>
<td>[M] /[Si] depends on phase formed. Sensitive to sintering environment. Rough surface.</td>
</tr>
<tr>
<td>$M + xSi \Rightarrow MSi_x$</td>
<td>Selective etch possible.</td>
<td></td>
</tr>
<tr>
<td>Metal deposited by evaporation, sputter, or CVD.</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Sputtering from a Composite MSi$_x$ Target.</td>
<td>Excellent [M] /[Si] control if correct target chosen. Good step coverage.</td>
<td>Contamination from Target.</td>
</tr>
</tbody>
</table>
Process Steps for Silicides

- Deposit poly, then poly sidewall protection/spacer
- Deposit metal & react to from silicide
  Note there is a separate mask for silicide location
- Remove none reacted metal

![Diagram of Salicide process flow and final structure](image)

Fig. 13  Salicide process flow and final structure.  (© 1985 IEEE.)
Resistivity of Silicides

- Note: Al is 2.6 micro-ohm cm
- Silicides 4-30 times worse
- But still ~10-100 lower resistance than poly
- Hence circuits faster

<table>
<thead>
<tr>
<th>Material</th>
<th>Metal + Poly-Si</th>
<th>Metal + Si Crystal</th>
<th>Co-Sputter</th>
<th>Co-Evaporation</th>
<th>CVD</th>
</tr>
</thead>
<tbody>
<tr>
<td>TiSi$_2$</td>
<td>13</td>
<td>15</td>
<td>25</td>
<td>21</td>
<td>21</td>
</tr>
<tr>
<td>TaSi$_2$</td>
<td>35</td>
<td>50</td>
<td>21</td>
<td>21</td>
<td>38</td>
</tr>
<tr>
<td>MoSi$_2$</td>
<td>90</td>
<td>15</td>
<td>100</td>
<td>40</td>
<td>120</td>
</tr>
<tr>
<td>WSi$_2$</td>
<td>70</td>
<td>30</td>
<td>40</td>
<td>40</td>
<td></td>
</tr>
<tr>
<td>PtSi</td>
<td>28</td>
<td>35</td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
Properties of Silicides

- Silicides much higher melting but higher thermal conduction
- Still allows higher temperature operation

<table>
<thead>
<tr>
<th>Material</th>
<th>Melting Point (°C)</th>
<th>Resistivity (µΩ·cm)</th>
<th>Thermal Coefficient of Expansion ($10^{-6}$/°C)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Si</td>
<td>1420</td>
<td>500 (heavily doped poly)</td>
<td>3.0</td>
</tr>
<tr>
<td>TiSi$_2$</td>
<td>1540</td>
<td>13-17</td>
<td>10.5</td>
</tr>
<tr>
<td>MoSi$_2$</td>
<td>1870</td>
<td>22-100</td>
<td>8.2</td>
</tr>
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<td>TaSi$_2$</td>
<td>2400</td>
<td>8-45</td>
<td>8.8</td>
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<td>2050</td>
<td>14-17</td>
<td>6.2</td>
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<td>Ti</td>
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</tr>
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<td>Mo</td>
<td>2620</td>
<td>5</td>
<td>5.0</td>
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<tr>
<td>Ta</td>
<td>2996</td>
<td>13-16</td>
<td>6.5</td>
</tr>
<tr>
<td>W</td>
<td>3382</td>
<td>5.3</td>
<td>4.5</td>
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</table>