DESIGN OF PC-PROGRAMMABLE DIGITAL HEARING-TESTING DEVICE

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Abstract

The design of PC programmable digital Hearing-Testing Device is described in this paper targeting the testing of hearing impaired- ness in a laboratory environment. It is used to measure the response of each ear at different frequencies and at different sound pressure level (SPL). The device input is the serial 12-bit data and 7-bit control signal from USB connection while the output signal is sound waves with frequency range from 20 Hz to 20 KHz. This device is designed and simulated in 0.18 μm CMOS technology. It is composed of digital components except for the active filter. The device is designed as a single chip to fit on a 32 Ω headphones and powered by 1.3V supply. The device is designed without using any ADC and DAC converters. Improved designs of 12-Bit counter, clock generator and control are proposed. PWM generator is designed using digital components only to provide more accuracy and reliability. A second order, Butter-worth active low-pass filter is used as demodulator. The SPL output of the device is PC controllable through the USB connection.

Keywords*: Digital circuit; hearing-testing device; mixed signal circuits; VLSI circuit design.*

1. Introduction

Previously, hearing related devices have been integrated using bipolar circuit techniques as described in [1]. Recently, such devices are being implemented using CMOS technologies to obtain low-power mixed signal systems-on-a-chip. Different kinds of such devices are available in the market like digitally programmable analog processors [3]-[6] or embedded DSP processors [7]-[8]. Digitally programmable analog processors are low cost and low power devices whereas the others have more reliability and lower design time.

Other challenge with hearing testing/aid is the power supply. 1.1V to 1.5V battery is used for circuit operation. To overcome the voltage requirement in CMOS technologies or low power constraints, supply multipliers based on charge pumps [2] are used [3],[8]. However; these doublers increase the die area and the number of discrete components. Therefore, power efficiency is reduced. Some state-of–the-art implementations [8] use special CMOS process optimizations which may increase the final integration cost.

In this paper, we propose a design approach based on digital design techniques. This CMOS circuit design avoids the use of voltage multipliers and it is intended for full integration, on a single chip, in a standard CMOS technology without any process enhancement. Moreover, all components, except headphone and coupling and bypass capacitors are designed on a single mixed-signal IC. All the components except active low-pass filter are digital. Therefore, the design provides the needed flexibility and reliability without using complex DSP algorithms. The detailed designs of USB controller, 12-Bit data register and 7-Bit control register are not discussed here. In the following sections, we will first describe all the blocks briefly. Then we will discuss the implementation in CMOS 0.18 μm process along with the simulation results.

2. Architecture

The complete architecture of the proposed design is shown in Fig. 1. All the blocks, except the H-Bridge and active low-pass filter blocks, are designed using digital design techniques. This is to achieve more flexibility, accuracy and reliability. Other features offered by our device are:

- Full audio-range output (from 20 Hz to 20 KHz)
- No ADC or DAC converters is used
- Fully digital PWM generator
- 11 to 107 dB SPL range controlled by digital control block
- 12-Bit accurate resolution
- No complex DSP algorithms is used

The description of each block is presented in the next sections.

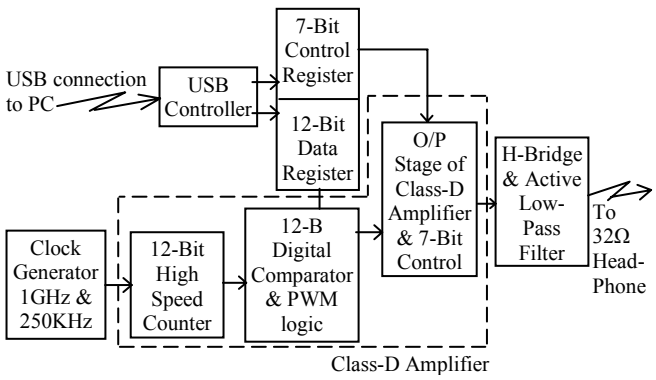

Fig. 1: Architecture of Proposed Design

2.1. Clock Generator

Two clock frequencies, 1 GHz and 250 KHz, are generated using digital design technique. 1GHz clock is used in 12-Bit high speed counter and 250 KHz clock is used for resetting the Counter to 0, sampling input data in input registers (12-Bit data register and 7-Bit control register) and resetting PWM pulse to logic high level. 1 GHz clock is generated using ring-oscillator. 250 KHz clock is then generated by dividing the 1-GHz pulse by 4096 using several stages of edge-triggered D flip-flops.

2.2. 12-Bit High-Speed Counter

This is the most important block to generate PWM pulses digitally. It is operating at 1 GHz speed. 12-Bit high speed Counter is implemented using 12-bit high speed up-counter and 12-bit register to store the data. Conditional-sum based 12-bit adder, known for its short time delay [9], is used to implement the high-speed up counter. The structure of the adder is simplified to perform as up-Counter. One of the two inputs is permanently grounded and carry-in is permanently connected to V_{DD}. Then the whole structure is simplified to reach the desired high speed.

2.3. 12-Bit Digital Comparator and PWM logic

12-Bit digital comparator circuit compares the 12-bit data of the register with 12-bit up-counter value and reset output to low if both are equal. PWM logic latches this momentary pulse to low level until rising edge of the reset signal is detected. As soon as the PWM output goes low, the clock signal to the 12-bit high-speed Counter is disabled to reduce the switching activity and dynamic power consumption. These clock pulses are recovered again when the PWM output signal goes high.

2.4. Class-D Amplifier Output Stage and 7-Bit Control Logic

Some designs of Class-D amplifier output stage are described in [10] to [13]. Output stage of Class-D amplifier is designed in H-bridge pattern to generate differential output. The 7-bit control signal is used to control the output sound pressure level (SPL) from 11 dB to 107 dB.

2.5. Active Low-Pass Filter

Active low-pass filter is used to generate sinusoidal audio waveforms from PWM pulses. One active low-pass filter is used in each H-Bridge branch. Second order, non-inverting, dual feedback configuration of Butterworth filter is used [14]. Most of the designs, [10] – [13], adopted passive low-pass filter using inductor. On-chip inductor occupies large area (of the IC chip) and their quality factor is low. Therefore, we used

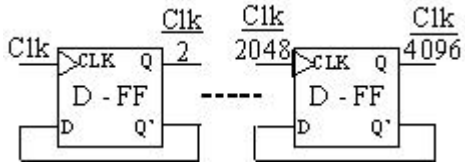

Fig. 2: Clock divider circuit

active-low pass filter design, based on basic circuit elements: resistors, capacitors and op-amp. These circuit elements are easy to integrate on a single chip. Active low-pass filters offer lower chip area and better performance than their passive counterpart for audio signals.

3. Implementation and Simulation Results

In this section, we will describe the design implementation and simulation results of all the building blocks.

3.1. Clock Generator

1 GHz clock pulse is generated using a ring-oscillator (a chain of odd-number inverters). 1 GHz pulse is divided by 4096 by several stages of D-FF as shown in Fig. 2.

'CLK' signal of each stage is connected to Q output of previous stage. D and Q' of the same flip-flop are connected together to invert logic level of Q and Q' signals on every rising edge of the input clock. Therefore, the frequency of Q and Q' is half of the input clock. A total of 12 D-FF are required to divide 1 GHz clock by 4096.

The simulation results obtained for the clock generator are shown below in Fig. 3 and Fig. 4. The actual time periods measured for 1 GHz and 250 KHz are 1.013 nsec and 4.1499 µsec. Therefore, actual frequency obtained is 0.99 GHz and 241 KHz.

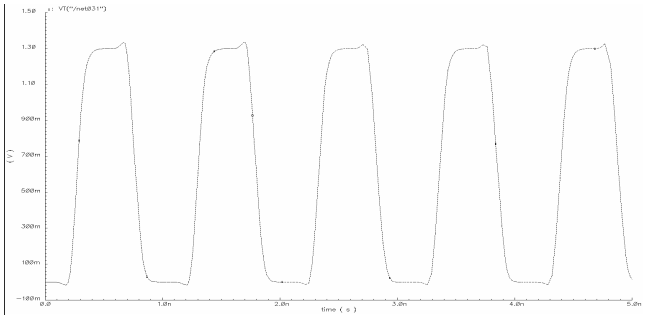
Fig. 3: 1GHz Clock Pulses

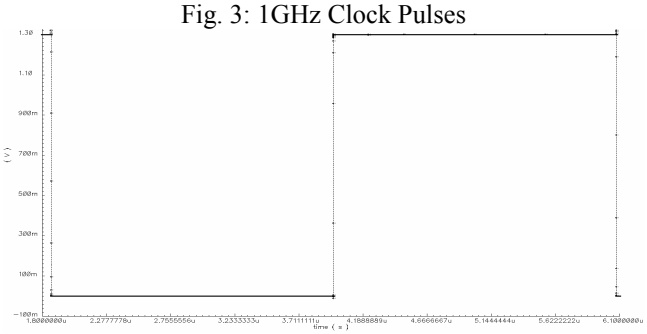
Fig. 4: 250KHz Clock Pulse

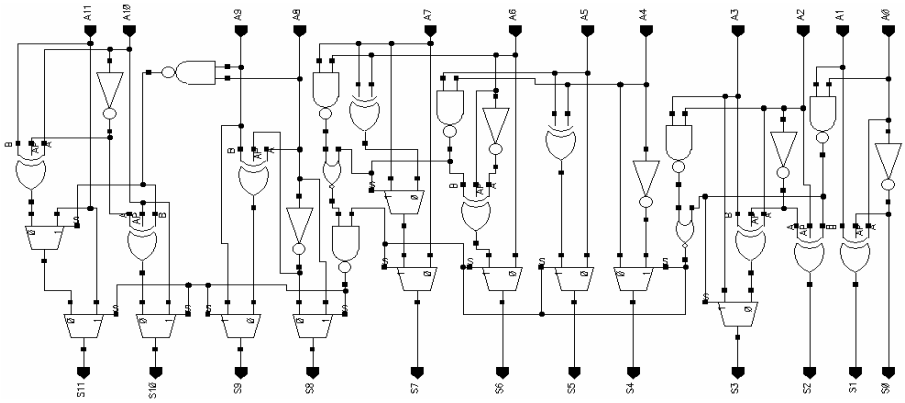

Fig. 5: 12-Bit Adder design for 12-Bit High Speed Counter

3.2. 12-Bit High-Speed Counter

This block consists of a 12-bit adder and a 12-bit register. The 12-bit register can be designed easily using D-FF. The Design of the 12-bit adder (to add a bit '1') is shown in Fig. 5. The basic structure of conditional-sum adder is described in [9] and [15]. Both of them used multiplexers as the basic building block. We designed the 12-bit up counter using 2 NOR, 6 NAND, 6 INV, 7 XOR, 2 simplified XOR (both A and A' is available externally instead of inverting in XOR block) and 11 MUX gates. We simplified our 12-bit adder design by connecting one input to ground and the carry-in to the power supply (V_{DD}). Our counter operates at 1 GHz frequency with 1.3V supply.

3.3. 12-Bit Digital Comparator and PWM Logic

The 12-bit digital comparator was designed using XNOR, NAND and NOR gates. Multiple stages of NAND and NOR gates are used to avoid high fan-in.

The PWM Logic is designed using modified D-FF. The clock sensitivity is changed to active-low and D input is connected to V_{DD}. Q' is used to deliver the output PWM signal.

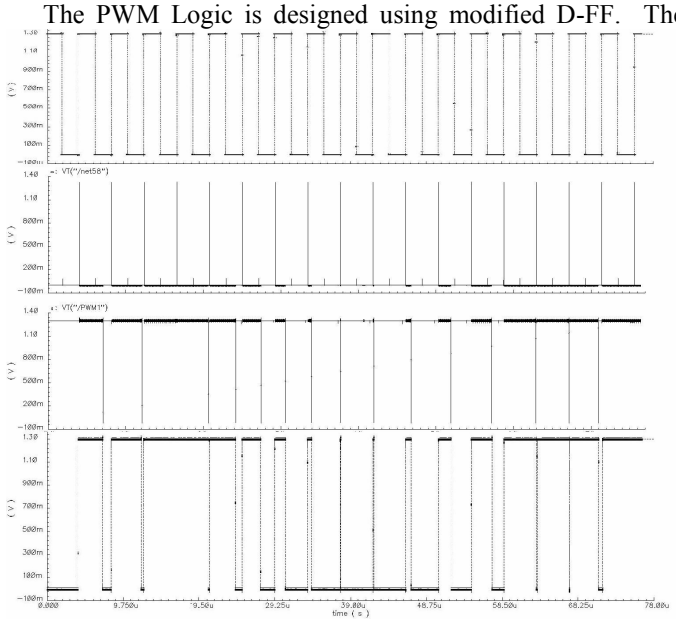

Fig. 6: (1) 250KHz Clock, (2) Reset Input to PWM Logic, (3) Digital Comparator Output and (4) Digitally generated PWM

The simulation waveforms for input and output of PWM logic are shown in Fig. 6. The PWM pulses goes high when momentary reset pulse (Fig. 6(2)) is available. The PWM output goes low when low level pulse (Fig. 6(3)) is detected at the input. The pulse-width of reset pulse (Fig. 6(2)) and digital comparator output (Fig. 6(3)) are 2nsec and 1nsec respectively. Fig. 6(4) shows the PWM pulses generated for 20 KHz audio signal.

3.4. Class-D Amplifier Output Stage and 7-Bit Control Logic

Different Class-D amplifier output stage designs are described in [10] to [13]. Among them, we used multiple stages of MOS transistors. The 7-Bit control logic is the most challenging part of the overall design. It was implemented based on digital design technique. This turned out to be very challenging for SPL below 20dB, and especially below 10dB. The output sound pressure level (SPL) is controlled from 11 to 107dB in steps of 1dB or 2dB.

3.5. Active Low-Pass Filter

The 2nd order active low-pass filter is designed with non-inverting op-amp configuration. Dual feedback loops are used to implement Butterworth filter as described in [14]. Two op-amps, designed in CMOS technology, are used. The first op-amp is used to tune the gain of the active low-pass filter. The second op-amp implements the 2nd order low-pass filter. Both op-amps have different output stage. The output stage of the first op-amp is designed with small size transistors. However; the output stage of the second op-amp is designed with very large transistors to reduce the output stage resistance and to supply sufficient current. The cut-off frequency is set to 100 KHz to get flat response up to 20 KHz audio input. 250 KHz sampling frequency is used in our design to obtain very low noise and distortion up to 20 KHz frequency. The values of resistors and capacitors are calculated by considering above mentioned specifications. The output audio wave for 20 KHz frequency is shown in Fig. 7.

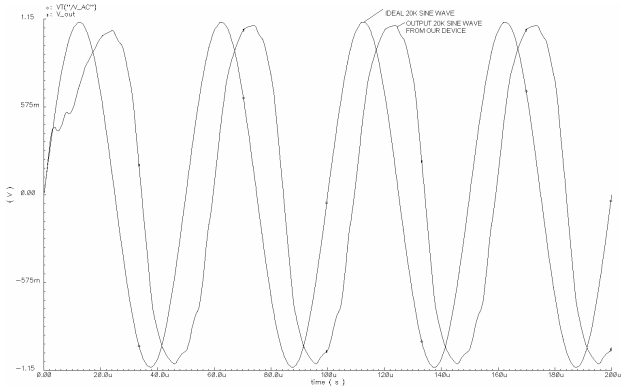

Fig. 7: Ideal 20K Sine Wave and 20K Output Wave from Our Device

4. Conclusion

The design of PC programmable digital Hearing-Testing Device, for high accuracy and reliability applications, is presented. The device is designed as a single chip to fit on a 32 Ω headphones and powered by 1.3V supply. The device is designed without using any ADC and DAC converters. New designs of 12-Bit counter, clock signals generator and control circuits are used.

Digital design technique is used to generate clock pulses. Improved design of the clock divider, using D-FF, is also presented. The requirement of ADC and DAC is eliminated by using a 12-bit high-speed Counter. The SPL of the device is PC controllable (through the USB connection) from 11 to 107 dB in steps of 1dB or 2dB. Simulation results, in the form of input and output waveforms of main design blocks, are also presented. This PC controlled device offers portability with increased flexibility and controllability of the output sound waves in a hearing impaired-ness testing laboratory.

References

[1] A. C. van der Woerd, "Analog circuits for a single-chip infrared controlled hearing aid" , *J. of Analog Integrated Circuits Signal Processing*, vol. 3, pp. 91-103, 1993.

[2] P. Favrat, P. Deval and M. J. Declercq, "An improved voltage doubler in a standard CMOS technology", *Proc. of IEEE International Symposium of Circuits and Systems*, vol. 1, 1997, pp. 249-252.

[3] F. Callias, F. H. Salchli, *et al.*, "A set of four IC's in CMOS technology for a programmable hearing aids," *IEEE J. Solid-State Circuits*, vol. 24, pp. 301–312, Apr. 1989.

[4] D. Wayne, M. Rives, *et al.* "A singlechip hearing aid with one volt switched-capacitor filters," in *Proc. IEEE Custom Integrated Circuits Conf.*, 1992, pp. 7.5.1–7.5.4.

[5] A. B. Bhattacharyya, *et al.*, "A micropower analog hearing aid on low-voltage CMOS digital process," in *Proc. 9th Int. Conf. VLSI Design*, Jan. 1996, pp. 85–89.

[6] J. F. Duque-Carrillo, P. Malcovati, *et al.*, "VERDI: An acoustically programable and adjustable CMOS mixed-mode signal processor for hearing aids applications," *IEEE J. Solid-State Circuits*, vol. 31, pp. 634–645, May 1996.

[7] H. Neuteboom, M. A. E. Janssens, *et al.*, "A singlebattery, 0.9 V-operated digital sound processing IC inlcuding AD/DA and IR receiver with 2mWpower consumption," in *IEEE Int. Solid-State Circuits Conf. Dig. Tech. Papers*, 1997, pp. 98–99.

[8] D. G. Gata, W. Sjursen, J. R. Hochschild, J. W. Fattaruso, L. Fang, G. R. Iannelli, Z. Jiang, C. M. Branch, J. A. Holmes, M. L. Skorcz, E. M. Petilli, S. Chen, G.Wakeman, D. A. Preves, andW. A. Severin, "A 1.1-V 270-μA mixed-signal hearing aid chip," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1670–1678, Dec. 2002.

[9] K. K. Parhi, "Fast VLSI Binary Addition", *SIPS 97 - Design and Implementation., 1997 IEEE Workshop on Signal Processing Systems*, Nov. 1997, pp. 232 – 241.

[10] K. P. Sozanski, R. Strzelecki and Z. Fedyczak, "Digital Control Circuit for Class-D Audio Power Amplifier", *IEEE 32nd Annual Power Electronics Specialists Conference*, June 2001, pp. 1245 - 1250 vol.2.

[11] I. D. Mosely, P. H. Mellor and C. M. Bingham, "Effect of dead time on harmonic distortion in class-D audio power amplifiers", *Electronics Letters*, 10th June 1999, Vol. 35, No. 12, pp. 950 – 952.

[12] V. M. Tousi, F. Sahandi, M. Atarodi and M. Shojaei, "A 3.3V/1W Class D Audio Power Amplifier with 103dB DR and 90% Efficiency", *Proc. of 23rd International Conference on Microelectronics*, Vol. 2, May 2002, pp. 581-584.

[13] A. R. Oliva, S. S. Ang and T. V. Vo, "A Multi-Loop Voltage-Feedback Filterless Class-D Switching Audio Amplifier using Unipolar Pulse-Width-Modulation", *IEEE Transactions on Consumer Electronics*, Vol. 50, No. 1, Feb. 2004, pp. 312-319.

[14] D. Meador, *ANALOG SIGNAL PROCESSING WITH LAPLACE TRANSFORMS AND ACTIVE FILTER DESIGN.* by Delmar – Thomson Learning, 2002.

[15] N. H. E. Waste and D. Harris, *CMOS VLSI DESIGN: A CIRCUITS AND SYSTEMS PERSPECTIVE.* Third Edition, by Addison-Wesley – Pearson Education Inc., 2004.