ATM FORUM:Technical Committee Working Group
ATM_Forum/94-0413
****

SOURCE: Bellcore
Deh-phone Hsing and Ljiljana Trajkovic
445 South Street
Morristown, N.J. 07960
Phone: (201) 829-4634, (201) 829-4531
Email:dpkh@corvus.bellcore.com
Email: ljilja@thumper.bellcore.com

****

TITLE: Simulation Studies of CDV Tolerance - Single Node Configuration

****

DATE: May 10 - 13, 1994

****

DISTRIBUTION TO: ATM Forum Technical Working Group Members

****

ABSTRACT

We investigate the one-point Cell Delay Variation and the Cell Transfer Delay for a given constant bit rate connection under Test Scenarios 1 through 4 described in contribution ATM_Forum/94-265. Furthermore, we studied the buffer occupancy at the multiplexor. This contribution provides a summary of our initial results.

****

NOTICE

1. Introduction

We investigate the one-point Cell Delay Variation (CDV) and the Cell Transfer Delay (CTD) for a given constant bit rate (CBR) connection under Test Scenarios 1 through 4 described in the contribution ATM_Forum/94-265 [1]. Furthermore, we studied the buffer occupancy at the multiplexor. This contribution provides a summary of our initial results.

We consider the single node configuration (Configuration 1 described in ATM_Forum/94-265) as shown in Figure 1. An ATM multiplexor is used to model a network element where traffic from various sources is converging. A common buffer is shared by all the input ports in our model.

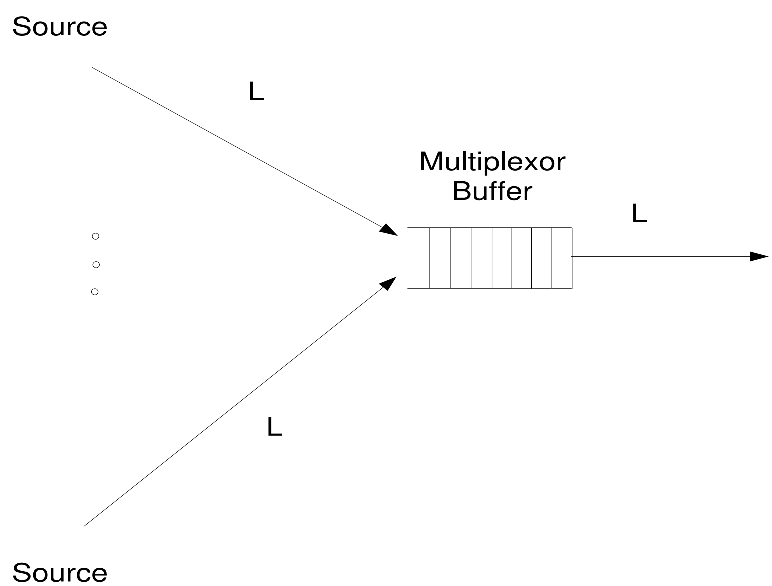

Figure 1. Single Node Model.

In the FIFO scheduling scheme, cells that arrive first are transmitted first. If cells arrive from various sources simultaneously, they are processed in a decreasing order of the bit rates of the associated connections. Each cell, after being generated at the source, experiences 1 cell time (2.831 microseconds, the time required to send 424 bits at 149.76 Mbps) delay before it is placed in the multiplexor buffer. Another 1 cell time delay will be introduced at the output of the multiplexor buffer for each transmitted cell in addition to any queuing delays incurred.

For a given connection, the one-point CDV is defined as the theoretical arrival time minus the actual arrival time at a specified measurement point. In our case, the one-point CDV is measured after a cell leaves the multiplexor buffer. The algorithm used to calculate the one-point CDV is given in Figure 2. This algorithm is equivalent to the Generic Cell Rate Algorithm (GCRA) used in the Forum UNI Specification Version 3.0 [2] in defining traffic conformance. The CTD is measured from the time when a cell is generated at the source to the time when the same cell leaves the multiplexor.

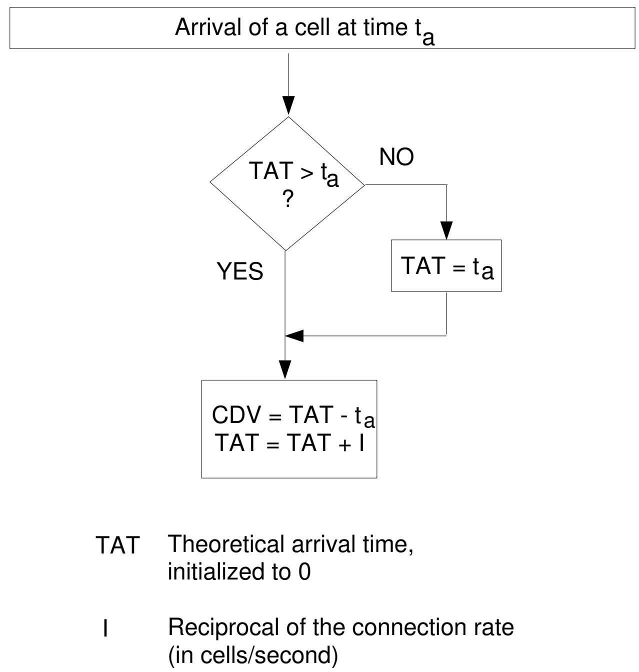

Figure 2. One-point CDV Calculation.

2. Simulation Results and Discussion

We provide one-point CDV and CTD histograms for each test scenario. Furthermore, for each test scenario, we provide histograms of the multiplexor buffer occupancy observed after each cell enters the multiplexor buffer.

Figures 3 to 9 show results of Test Scenarios 1 to 4 under FIFO scheme. The simulation run length is 5 seconds. The load of the output link of the multiplexor is approximately 91% in Test Scenario 1. The load of the output link of the multiplexor varies: from 55% to 95% in Test Scenario 2, from 35% to 95% in Test Scenario 3, and from 43% to 93% in Test Scenario 4, as the load of the background Poisson traffic increases. The following observations are based on the simulation results:

- Distributions of the one-point CDV and the CTD vary widely.
- CTD is less than 60 microseconds if there is no background Poisson traffic.
- CTD increases as the background Poisson traffic load increases. In all investigated scenarios CTD is less than the inter-cell spacing of the slowest source.
- Maximum CTD gives a reasonable estimate of the one-point CDV bound for the fast sources. For the slow sources this approximation over-estimates the actual one-point CDV bound.
- Difference of the maximum CTD and minimum CTD could under-estimate the one-point CDV bound.
- Buffer occupancy is no greater than 21 cells with no background Poisson traffic.
- Buffer occupancy increases as the background Poisson traffic load increases. At the same load level, the more the Poisson source contributes, the worse the buffer occupancy

becomes. In all investigated scenarios, if the load is not greater than 80%, the observed buffer occupancy is no greater than 30 cells (Figures 3 to 9).

– Maximum buffer occupancy observed at loads greater than 80% falls between the 10^{-5} and 10^{-6} quantiles obtained from M/D/1 queue (Table 1).

Table 1: The Queue Length Statistics (in cells) of an M/D/1.

	40%	50%	60%	70%	80%	90%
10^{-5} quantile	7	9	12	17	27	56
10^{-6} quantile	9	11	15	21	32	67
10^{-9} quantile	13	17	22	31	48	100

References

[1] ATM_Forum/94-265, "Common Scenarios for Simulation Studies of Cell Delay Variation Tolerance," March 1994.

[2] ATM User-Network Interface Specification, Version 3.0, 1993.

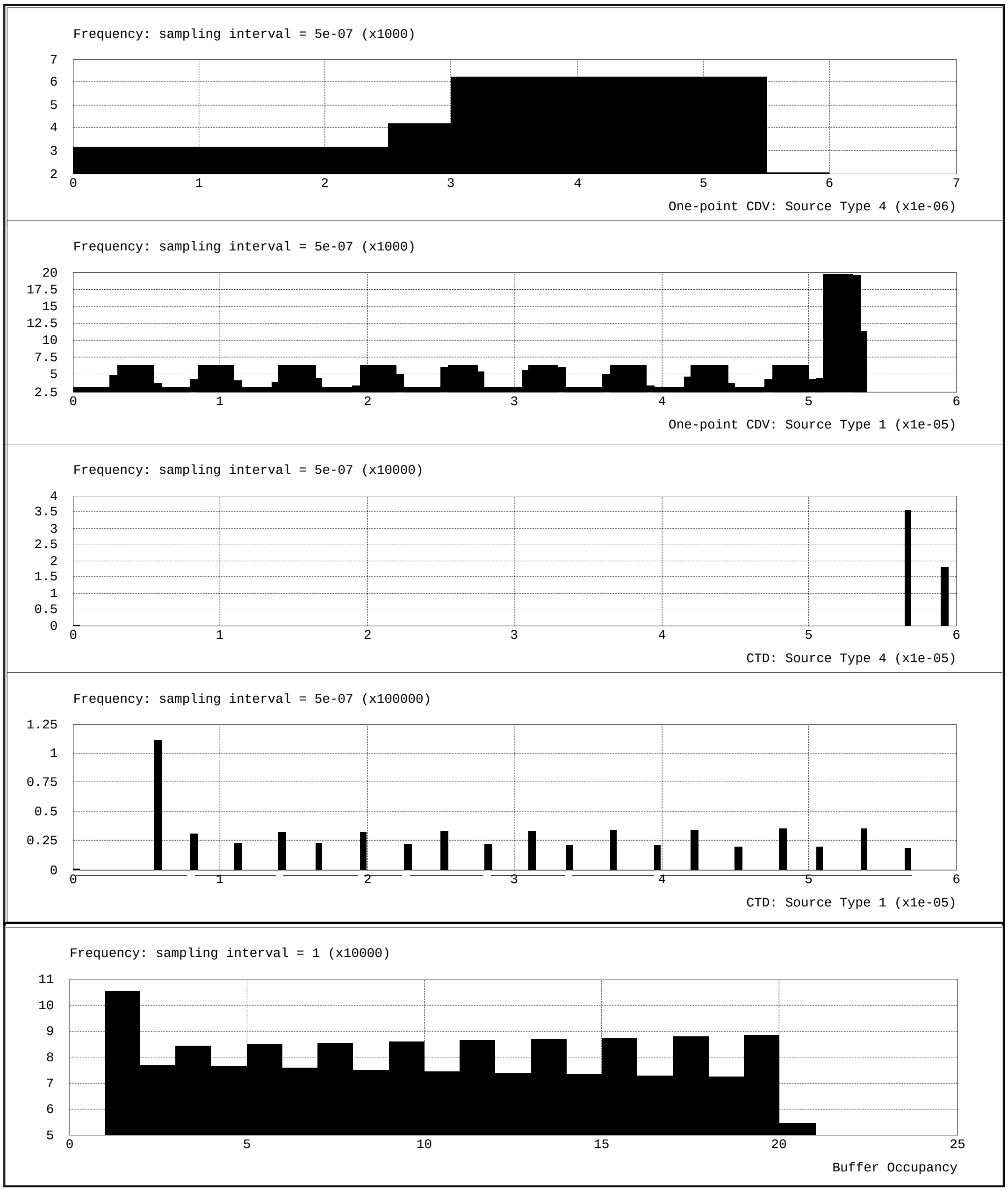

Figure 3: Test Scenario 1 - FIFO.

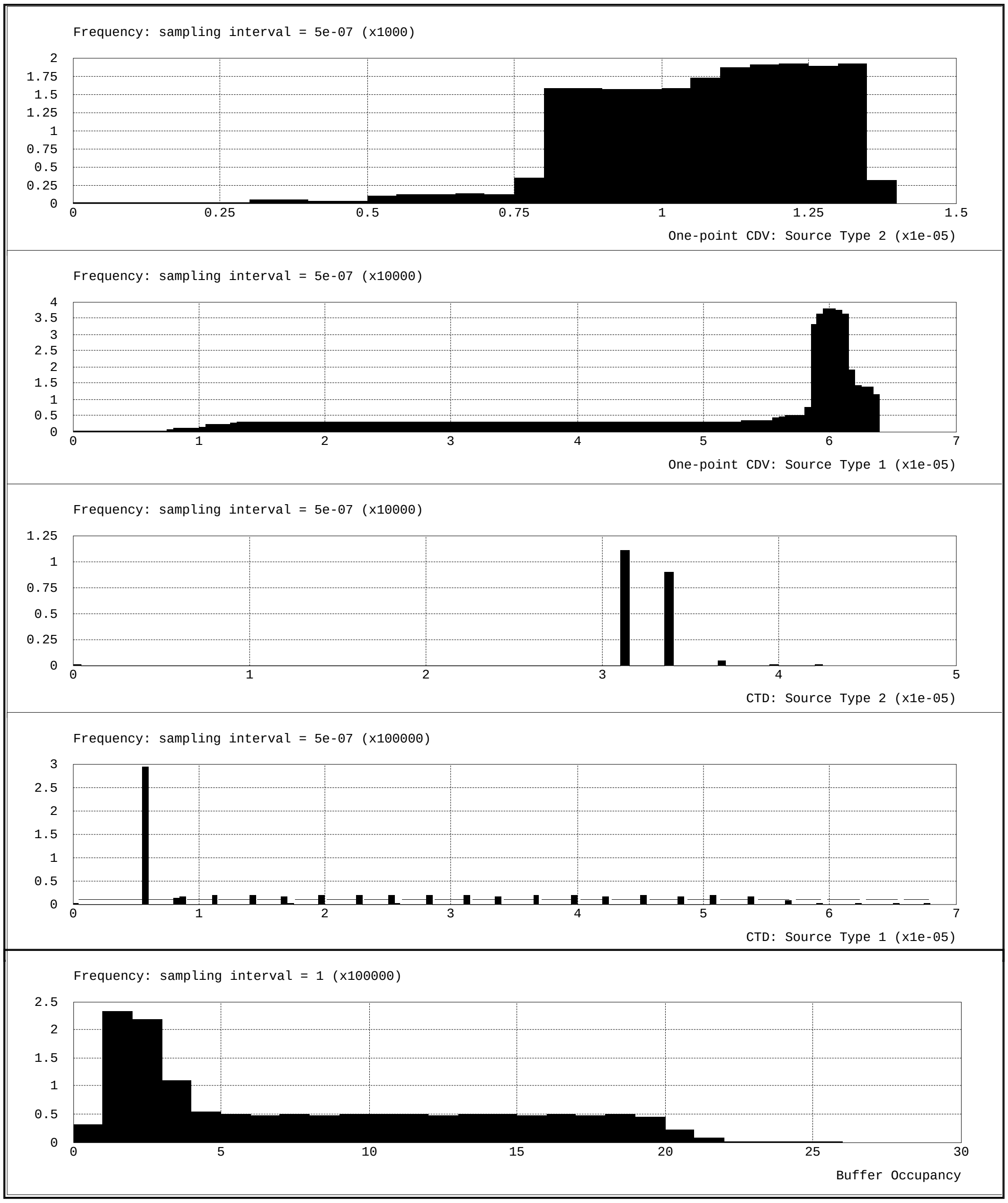

Figure 4: Test Scenario 2 (80% load) - FIFO.

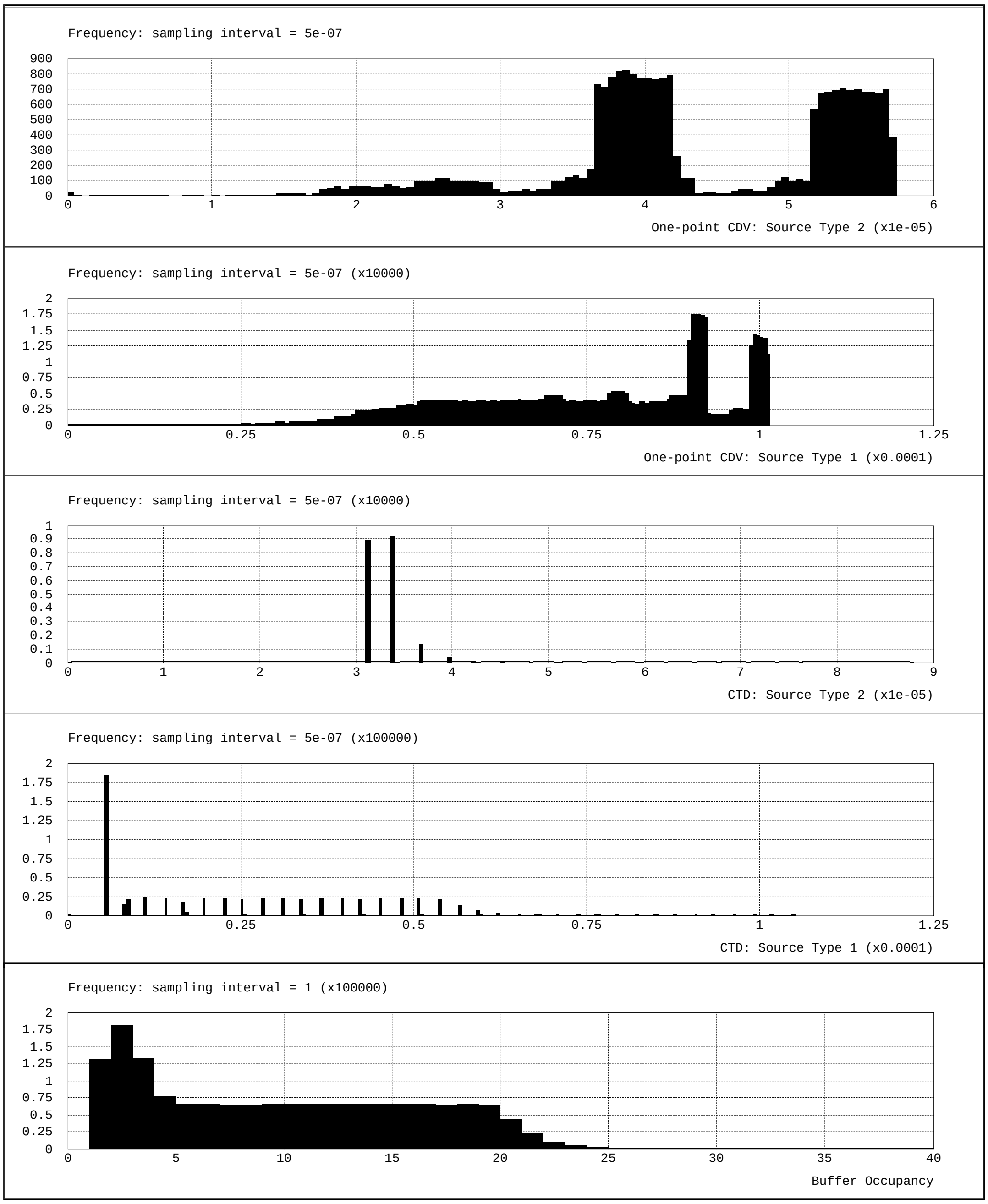

Figure 5: Test Scenario 2 (90% load) - FIFO.

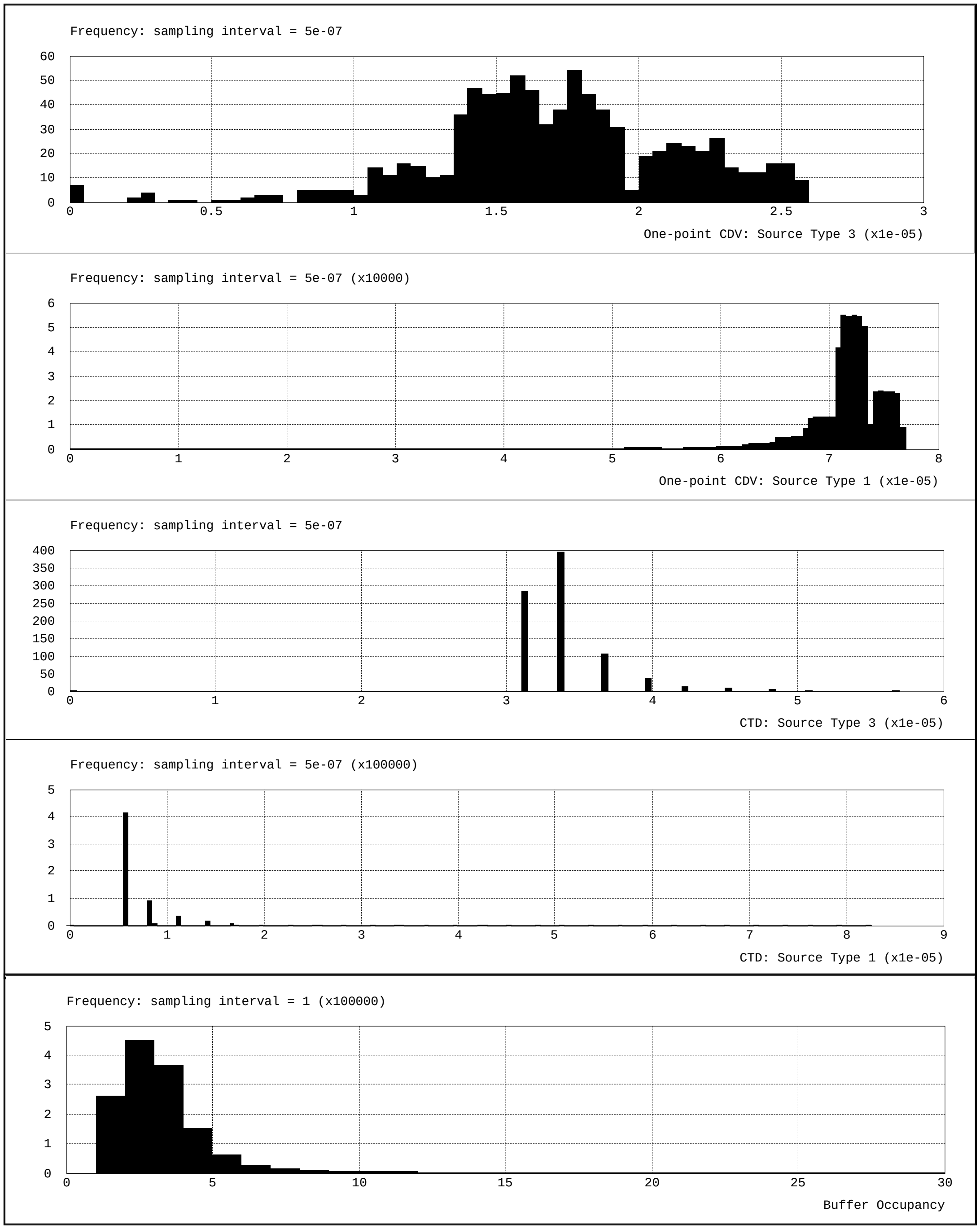

Figure 6: Test Scenario 3 (80% load) - FIFO.

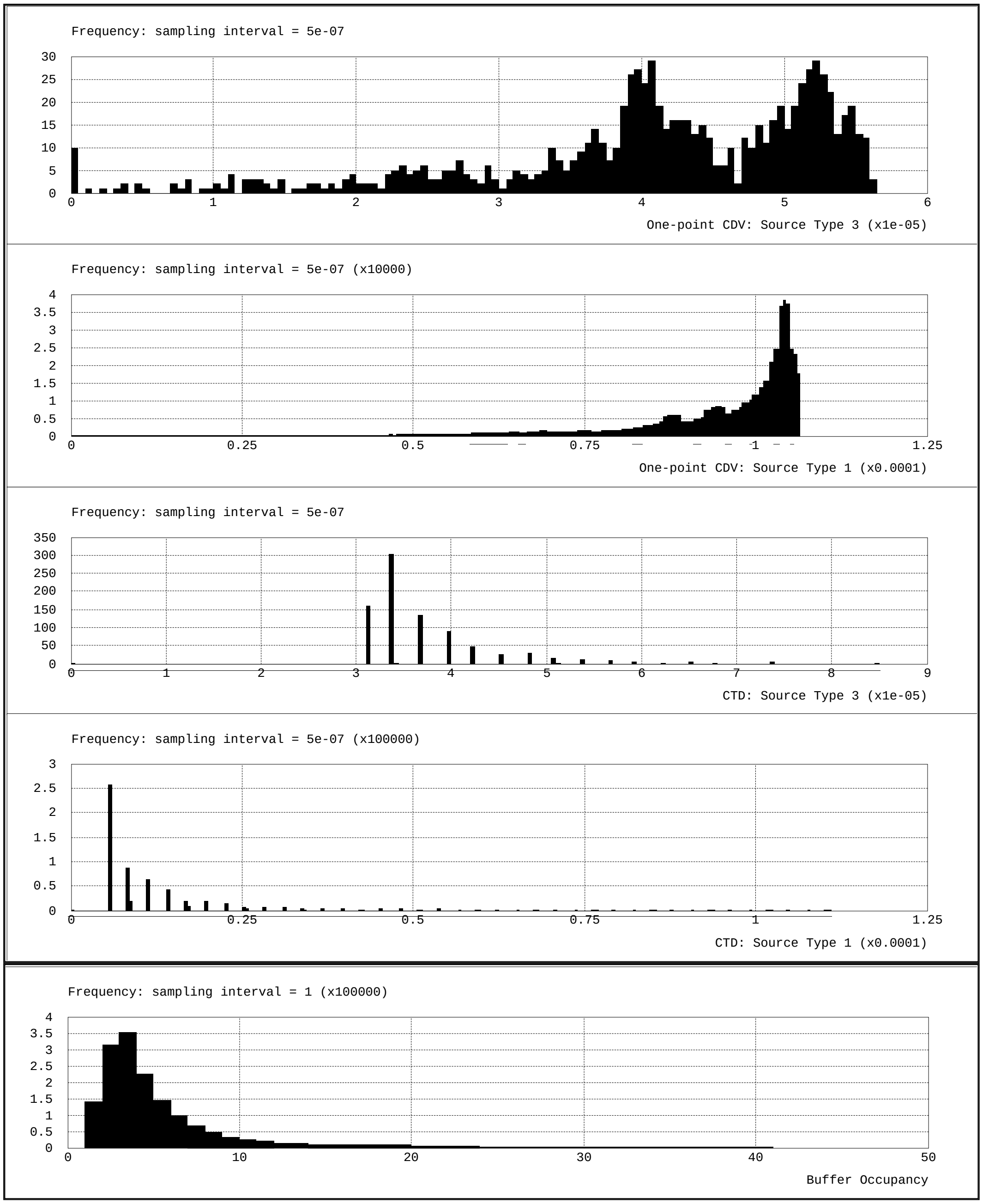

Figure 7: Test Scenario 3 (90% load) - FIFO.

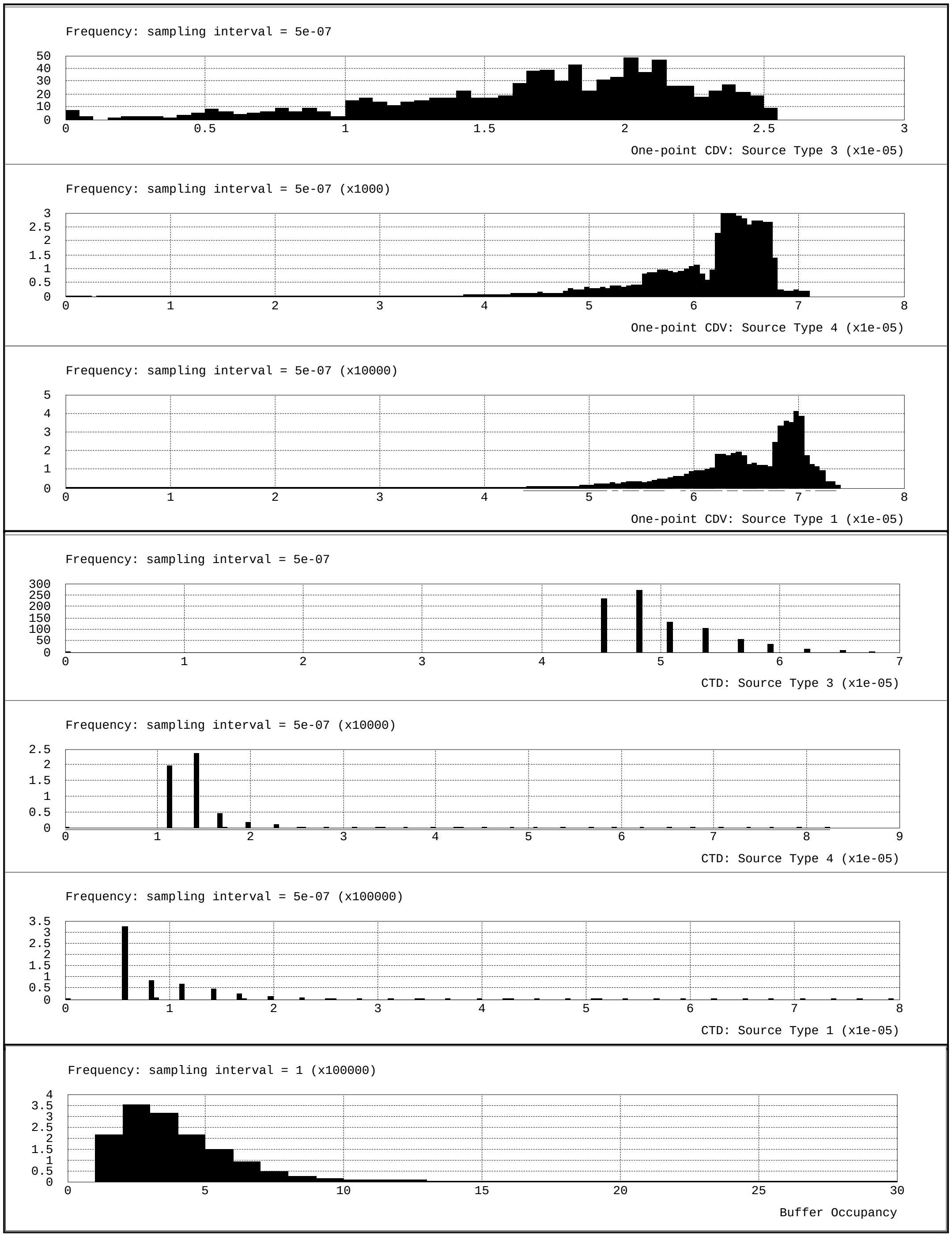

Figure 8: Test Scenario 4 (83% load) - FIFO.

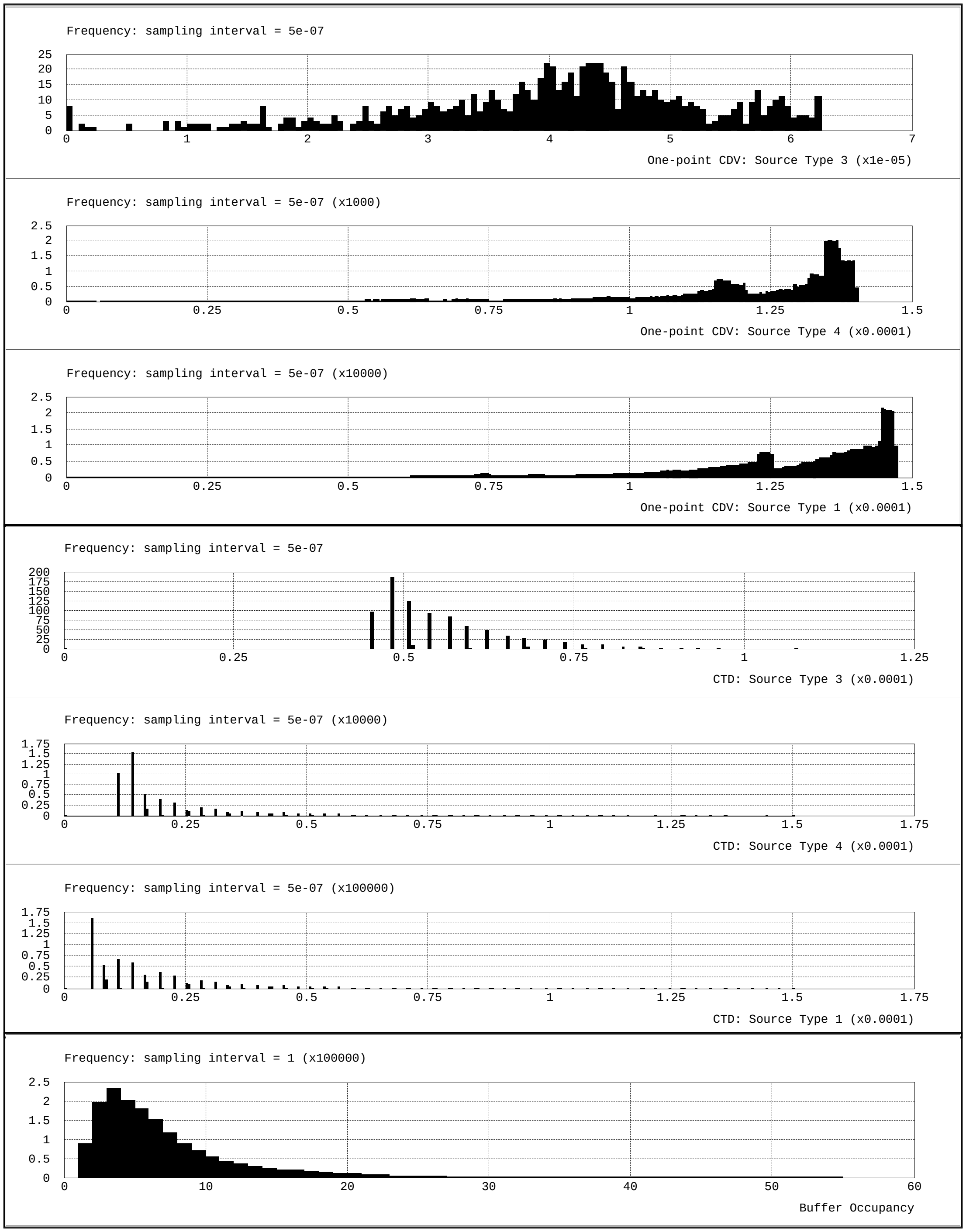

Figure 9: Test Scenario 4 (93% load) - FIFO.