ANALYSIS OF FEEDBACK STRUCTURES AND THEIR EFFECT ON MULTIPLE DC OPERATING POINTS

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Abstract

DC operating points of a circuit are the solutions of a set of nonlinear algebraic equations. This problem is usually hard to solve, even by using numerical approximative methods. This is the reason that we first confine ourselves to estimate qualitatively the *number* of circuit's operating points by analyzing its topology using the Nielsen-Willson theorem. As a result, we obtain the set of transistors that *could* possibly cause multiple dc operating points. In a second step, we apply a new method for testing each transistor in this set. After replacing such a transistor, we perform dc analysis and investigate if this transistor can cause so called "positive feedback," in which case the circuit possesses multiple dc operating points.

1 Introduction

Any design or simulation of a nonlinear circuit requires finding its dc operating point(s) first. Common methods for finding a dc operating point require that the starting value of a numerical process be close enough to the unknown solution. The determination of convergence areas for each solution—let alone the exact solution itself—used to be rather hard in practice. This is the reason that our approach first merely determines whether a circuit's solution is unique or whether there are multiple solutions.

Instead of aiming at an exact (quantitative) solution, we first analyze the circuits structure qualitatively, i.e., we find the effect of circuits topology on the number of dc operating points. Only after the first step is completed, we improve our method further.

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1.1 Problem statement

DC operating points are solutions (i.e., zero points) of a set of nonlinear equations

$$\mathbf{F}(\mathbf{x}) = \mathbf{0}$$

constructed from

- Kirchhoff's Voltage Law
$$\mathbf{B}^T\mathbf{u} = \mathbf{0}$$
- Kirchhoff's Current Law
$$\mathbf{A}\mathbf{i} = \mathbf{0}$$
- and the characteristics of the circuits elements
$$f_k(\mathbf{i}, \mathbf{u}) = 0.$$

These equations must be solved during the design process of virtually any electronic circuit. Unfortunately, this can be done analytically only in some simple cases. Hence, nonlinear approximative methods (e.g., Newton's method) are necessary, especially for more complex circuits with highly nonlinear elements characteristics.

1.2 Topological approach

In a simplified approach, we only consider the mere *topology* of the network. That means taking into account only:

- the circuit's elements connections to each other, and
- certain more general features of the element's characteristics (e.g., continuity and/or boundedness).

Parameters such as resistor's values, amplifying factors, and the *exact* appearance of the characteristics are ignored. Thus, the network is reduced to a graph consisting of nodes and branches, which will be examined instead.

Hence, all conclusions concerning the circuit's behavior must be guessed from certain basic patterns and the way elements are connected. This enables us to deduce the circuit's behavior merely due to its topology, instead of having to solve complicated nonlinear equations.

2 Proposed method

First, we extract the circuits topological structures which might cause multiple dc operating points. The theorem of Nielsen and Willson [8] states that for that purpose we must find all circuit's feedback structures (FS) as shown in Fig. 1 (top). After finding all FS [2], we analyze each transistor in a FS separately,and find if it can indeed cause multiple dc operating points.

To achieve that goal we have developed the following method: We take one FS-transistor (assuming, without loss of generality, that transistor is of npn type) and replace it by a test circuit, as shown in Fig. 1 (bottom).

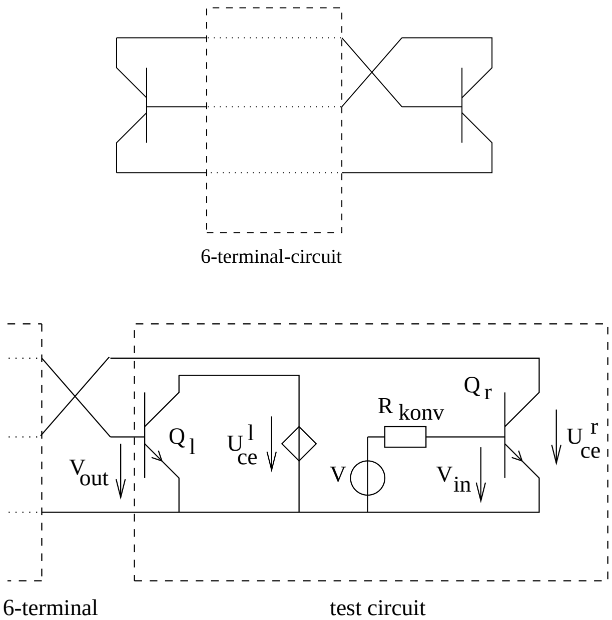

Figure 1: Top: FS composed of two bipolar transistors: The remaining of the circuit is enclosed in the 6-terminal circuit. Bottom: Replacing the right FS-transistor (assumed to be npn type) by a test circuit.

The test circuit consists of two transistors (Q_l on the left and Q_r on the right) identical to the replaced transistor, a resistor R_{konv}, an independent voltage source V, and an ideal voltage-controlled voltage source with voltage $U_{ce}^l = 1 \cdot U_{ce}^r$.

We perform a dc analysis on the complete circuit by increasing the voltage V resulting in a rise of v_{in}, and we plot $v_{out} = f(v_{in})$. The parameters for varying v_{in} are V_{start}, V_{stop}, the stepsize ΔV, and the resistor value R_{konv} for limiting the current $i_b(Q_R)$ if necessary and, hence, enlarging the convergence region of the simulator (values of approximately $10^{-6}\Omega - -10^{-2}\Omega$ will usually suffice).

2.1 The number of dc operating points

The intersecting points of $v_{out}(v_{in})$ and v_{in} are solutions of the base-emitter-voltage U_{be} of the FS transistor under investigation [3, 7]. In addition, the stability of a solution can be seen from $v_{out} = f(v_{in})$: v_{out} intersecting v_{in} from bottom left to top right means an unstable solution, the other case indicating a stable one (Fig. 2).

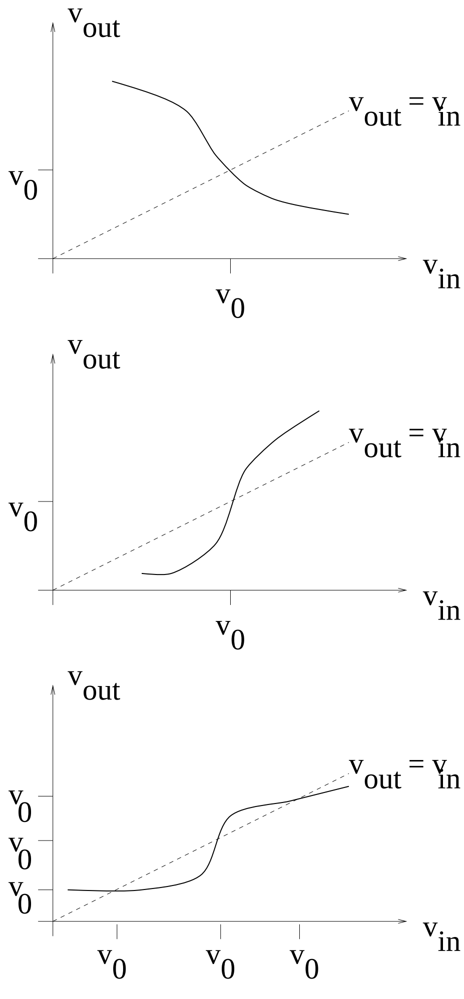

Figure 2: Solutions of $v_{out} = f(v_{in})$. Cases: a) stable, b) unstable, and c) bistable solutions v_0.

Hence, for an *unstable* operating point v_u:

$$
\begin{array}{lll}
v_{out} = v_{in} & \text{for} & v_{in} = v_u \\
v_{out} < v_{in} & \text{for} & v_{in} < v_u \\
v_{out} > v_{in} & \text{for} & v_{in} > v_u
\end{array}
$$

which implies:

$$\frac{d}{dv_{in}} v_{out}(v_{in}) > 1.$$

At a *stable* operating point v_s:

$$\begin{array}{lll} v_{out} = v_{in} & \text{for} & v_{in} = v_s \\ v_{out} > v_{in} & \text{for} & v_{in} < v_s \\ v_{out} < v_{in} & \text{for} & v_{in} > v_s \end{array}$$

which implies:

$$\frac{d}{dv_{in}} v_{out}(v_{in}) < 1.$$

2.2 Proof of equivalence

Theorem: If $v_1 = -U$, then both duplicated transistors have the same voltages and currents, and, hence, the same dc operating point as the original transistor.

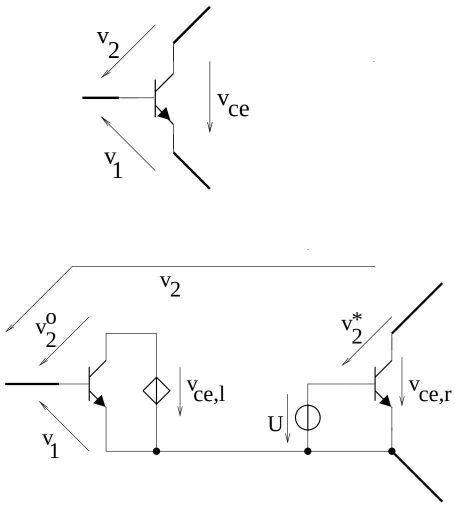

Figure 3: Circuit used in the proof of the main result.

Proof: From $v_{ce,r} = v_2 - v_1$ with $v_1 = -U$ follows:

$$v_{ce,r} = v_2 + U.$$

With $v_{ce,r} = v_2^* + U$, we get $v_2^* = v_2$. From $v_{ce,r} = v_2 - v_1$ and $v_{ce,l} = v_2^0 - v_1$, with $v_{ce,l} = v_{ce,r}$, we find $v_2^0 = v_2$.

In summary:

$$\begin{array}{rcl} v_1 & = & -U \\ v_{ce,l} & = & v_{ce,r} \\ v_2^* & = & v_2 \\ v_2^0 & = & v_2. \end{array}$$

Hence, all corresponding voltages are identical.

From the Ebers-Moll transistor model:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} 1 & -\alpha_r \\ -\alpha_f & 1 \end{pmatrix} \begin{pmatrix} f_1(v_1) \\ f_2(v_2) \end{pmatrix}$$

it follows that the corresponding currents are also identical.

Hence, the dc operating points of all three transistors are equivalent. Q.E.D.

2.3 Generalization

Although the method was introduced for npn bipolar transistors, it applies for pnp transistors as well. If we have reverse biasing (instead of forward one) collector and emitter terminal pins must be interchanged in the replacement.

Cutting loops and positive feedback are basic principles in control engineering. Hence,we can assume the method to be applicable for FET and other types of transistors as well.

3 Examples

We give two examples to illustrate the proposed method:

3.1 Flip-Flop circuit

The Flip-Flop circuit and its operating points are shown in Fig. 4 and 5, respectively.

```
Q1 3 2 0 modn
Q2 5 4 0 modn
.MODEL modn NPN BF=99 BR=49 IS=1E-6
Rc1 1 3 2k
Rc2 1 5 2k
Rb1 2 5 61k
Rb2 3 4 61k
Vcc 1 0 12
```

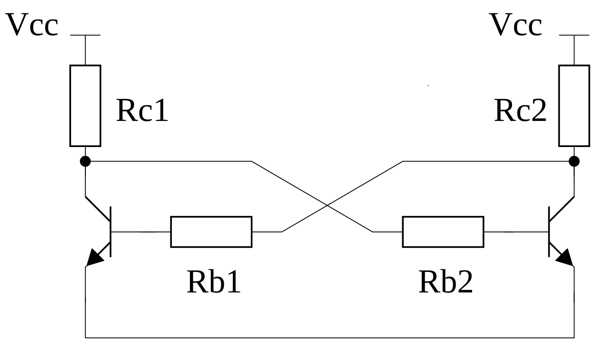

Figure 4: Flip-Flop circuit.

3.2 Latch-up circuit

The circuit and its operating points are shown in Fig. 6 and 7, respectively.

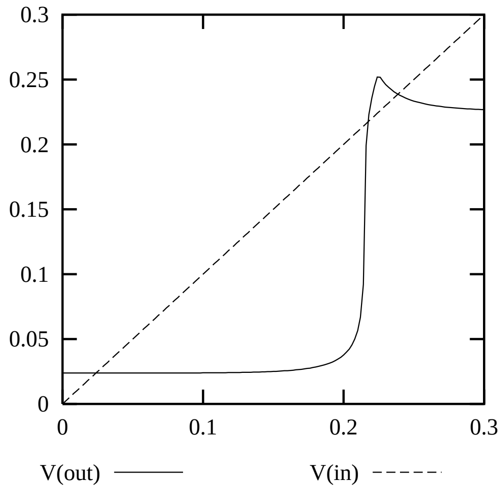

Figure 5: Flip-flop circuits: Dashed line: v_{in}, solid line: $v_{out}(v_{in})$, Result: two stable operating points at: $V_{in} \approx 0.02V$ and $V_{in} \approx 0.22V$ and one unstable solution at $V_{in} \approx 0.21V$.

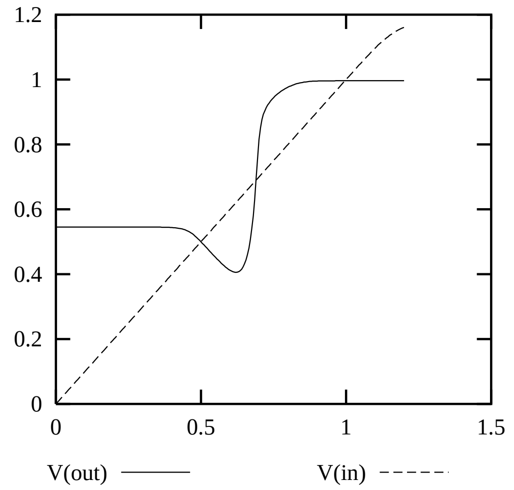

Figure 7: Latch-up circuit: Dashed line: V_{in}, solid line $v_{out}(v_{in})$. Result: two operating points at $V_{in} \approx 0.5V$ and $V_{in} \approx 1V$, and one unstable solution at $V_{ein} \approx 0.7V$.

```
Q1 1 2 4 modp
Q2 2 1 0 modn
.MODEL modp PNP BF=33 BR=10 IS=1E-14
.MODEL modn NPN BF=99 BR=49 IS=1E-14
Rein 44 4 1u
R 1 2 100
V1 44 0 1
```

Latch-up circuits can sustain large currents. These currents may be so large that they cause overflow errors in a simulator. Note that here the input resistance of only $R_{ein} = 1\mu\Omega$ is sufficient to limit the current.

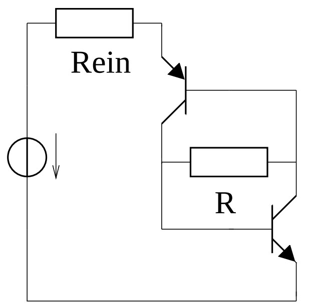

Figure 6: Latch-up circuit with $R = 100\Omega$ ([6], p. 96).

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