ANALYSIS OF FEEDBACK STRUCTURES IN FET CIRCUITS

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Abstract

Common numerical approaches for determining a circuit's dc operating points usually yield no more than one solution. Even applications of homotopy methods have performed with a limited success. We propose here a new method: a combination of investigating the circuit's topology and analyzing the circuit numerically. The method, named *test for positive feedback structures*, was previously introduced to determine which *bipolar* transistor, being part of a feedback structure, can cause *positive* feedback, and if so, what will be the circuit's operating points. In this paper we show that the method can be extended also to circuits with field effect transistors (FET's).

1 Introduction

In general, in this paper we deal with determining dc operation points of a given circuit. Circuit simulators use approximative methods (e.g., Newton-Raphson algorithm) to determine a circuits' dc operating points. These methods require "good" starting points that are close enough to the unknown solution. Although in many cases default initial values are sufficient for simulators to converge to a solution, they fail to reliably indicate if there are multiple solutions. Without a priori knowledge neither solutions themselves, nor a mere convergence area for each solution can be determined.

That is the reason that we devised a method that attempts to extract useful information about the circuit *before* the computational process. One of the criteria for extracting such information is provided by certain topological results related to transistor circuits.

Hence, instead of aiming at an exact (quantitative) solution, we first analyze the circuit's structure qualitatively. Then, at a later stage, we refine the approach by performing a numerical analysis in order to find the effect of the circuit's structure on the number of dc operating points.

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2 Problem statement

DC operating points are solutions (i.e., zero points) of a set of nonlinear equations [5]

$$\mathbf{F}(\mathbf{x}) = \mathbf{0}$$

constructed from

- Kirchhoff's Voltage Law
$$\mathbf{B}^T\mathbf{u} = \mathbf{0}$$
- Kirchhoff's Current Law
$$\mathbf{A}\mathbf{i} = \mathbf{0}$$
- and the characteristics of the circuits elements
$$f_k(\mathbf{i}, \mathbf{u}) = 0.$$

These equations must be solved during the design process of virtually any electronic circuit. Solving this set of equations purely numerically means ignoring the circuits electrical properties and peculiarities that we intend to take into account when applying our method.

3 Topological approach

One approach of qualitatively analyzing circuits is confining the circuit to the mere *topology* [6] of the network, which means considering only the way circuit's elements are connected to each other.

Nielsen and Willson [7] have found a unique structure that may cause multiple dc operating points in *bipolar* transistor circuits. A circuit may possess multiple dc operating points *only if* it possesses a feedback structure (FS) as shown in Fig. 1 (top). Willson [10] extended this result to include field effect transistors (FET). An FET feedback structure is shown in Fig. 1 (bottom).

The algorithm given in [3] for finding FS's can be used to detect FS's no matter whether they consist of bipolar transistors or of FET's. Since existence of a FS is only a necessary, but not sufficient condition for a transistor circuit to posses multiple dc operating points, additional analysis is required. The reason is that the number of dc operating points depends on the network parameters, which are ignored in the topological analysis.

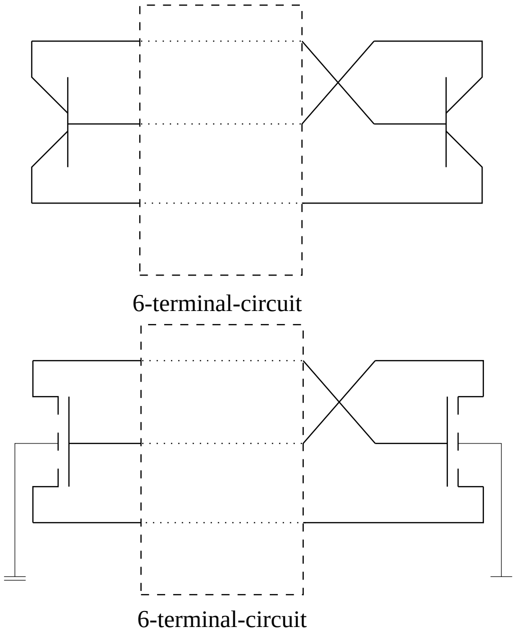

Figure 1: Feedback structure consisting of two bipolar transistors (top), and two FET's (bottom). The rest of the circuit is enclosed in a box. The type of a transistor (n type or p type) is irrelevant.

4 Field Effect Transistor models

4.1 Shichman-Hodges model

The large-signal behavior of an n-channel MOSFET can be described using the Shichman-Hodges [8] model:

$$i_g = 0.$$

If $v_{ds} > 0$, then $i_{dr} = \hat{f}(v_{gs}, v_{ds}) :=$

$$\begin{cases} 0 \\ \text{if} \quad v_{gs} - v_{to} < 0 \\ \text{(off state)} \\ \\ K(1+\lambda v_{ds}) \cdot (2(v_{gs} - v_{to})v_{ds} - v_{ds}^2) \\ \text{if} \quad v_{gs} - v_{to} \geq v_{ds} \geq 0 \\ \text{(active/linear state)} \\ \\ K(1+\lambda v_{ds}) \cdot (v_{gs} - v_{to})^2 \\ \text{if} \quad 0 \leq v_{gs} - v_{to} \leq v_{ds} \\ \text{(saturation or pinch-off state)} \end{cases}.$$

If $v_{ds} < 0$, then $i_{rd} = \hat{f}(v_{gd}, v_{sd})$.
Furthermore, $i_{rd} = -i_{dr}$ and $v_{sd} = -v_{ds}$, with $K = \frac{k'}{2}\frac{W}{L}$ and $k' = \mu_n C_{0x}$.

The Shichman-Hodges MOSFET model can be viewed as being analog to the Ebers-Moll model used for bipolar transistors. It follows from $i_g = 0$ and $i_g = -i_1 - i_2$ that $i_1 = -i_2$, which with $i_{dr} = \hat{f}(v_{gs}, v_{ds})$ gives the Ebers-Moll like equivalent for a MOSFET model:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} := \begin{pmatrix} -i_d \\ i_d \end{pmatrix} = \begin{pmatrix} -\hat{f}(-v_1, v_2 - v_1) \\ \hat{f}(-v_1, v_2 - v_1) \end{pmatrix}.$$

4.2 Tadeusiewicz model

Tadeusiewicz proved [8] that a MOSFET can be modeled as:

$$\tilde{i}_1 = f(v_{gs}, v_{gd}) :=$$

$$\begin{cases} K(1+\lambda \| v_{gs} - v_{gd} \|)(v_{gs} - v_{to})^2 & \text{if} \quad v_{gs} \geq v_{to} \\ 0 & \text{if} \quad v_{gs} < v_{to}. \end{cases}$$

$$\tilde{i}_2 = f(v_{gd}, v_{gs}) :=$$

$$\begin{cases} K(1+\lambda \| v_{gd} - v_{gs} \|)(v_{gd} - v_{to})^2 & \text{if} \quad v_{gd} \geq v_{to} \\ 0 & \text{if} \quad v_{gd} < v_{to}. \end{cases}$$

Taking the bulk of the pn junctions into account, with $\hat{i}_d(v) = I_s(e^{\frac{v}{v_T}} - 1)$, gives:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} =$$

$$\begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{pmatrix} -f(-v_1, -v_2) \\ -f(-v_2, -v_1) \end{pmatrix} + \begin{pmatrix} \hat{i}_d(v_{bs}) \\ \hat{i}_d(v_{bd}) \end{pmatrix}.$$

Compared to the Shichman-Hodges model, the Tadeusiewicz model employs only one expression for the functions $\tilde{i}_1$ and $\tilde{i}_2$. The only piecewise function is the one describing v_{gs}, but there is no distinction between the *active* and the *pinch-off* transistor state. In order to adapt the Tadeusiewicz model to the Ebers-Moll structure, we have used signs different from those found in [8],

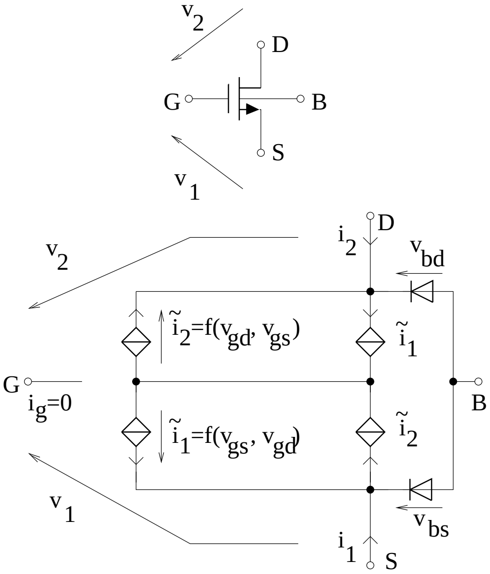

Figure 2: Tadeusiewicz MOSFET model.

Because the bulk of an n type MOSFET is usually biased to the lowest potential in the circuit, the bulk diodes are in a blocking state. Hence, the term $\hat{i}_d$ can be cancelled:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} 1 & -1 \\ -1 & 1 \end{pmatrix} \begin{pmatrix} -f(-v_1, -v_2) \\ -f(-v_2, -v_1) \end{pmatrix} \tag{1}$$

4.3 Ebers-Moll transistor model

For the sake of completeness, we give here the Ebers-Moll-model for bipolar transistors:

$$\begin{pmatrix} i_1 \\ i_2 \end{pmatrix} = \begin{pmatrix} 1 & -\alpha_r \\ -\alpha_f & 1 \end{pmatrix} \begin{pmatrix} f_1(v_1) \\ f_2(v_2) \end{pmatrix},$$

where $f_k(v_k) = m_k(e^{n_k \cdot v_k} - 1)$.

Transistor parameters $\alpha_f, \alpha_r \in (0,1)$ are constant and satisfy the sign relationship $m_k n_k > 0$. Furthermore, they satisfy the *reciprocity relation* obtained from the device physics: $\alpha_f m_1 = \alpha_r m_2$, and the *no gain property* $\alpha_r \leq \frac{m_1}{m_2} \leq \frac{1}{\alpha_f}$ and $n_1 = n_2$. In case of npn transistor type $m_k, n_k < 0$, while for pnp transistors $m_k, n_k > 0$.

In the above equations, the voltages and currents denote the junction variables:

$$\begin{aligned} v_1 &= u_{emitter-base} \\ v_2 &= u_{collector-base} \\ i_1 &= i_{emitter} \\ i_2 &= i_{collector}. \end{aligned}$$

Hence, $i_{base} = -(i_1 + i_2)$.

5 Test for positive feedback structures in circuits with FET's

5.1 Replacing transistors in a feedback structure

In [2, 4] the bipolar transistor under investigation (FS-transistor), belonging to a feedback structure FS, was replaced by the circuit shown in Fig. 3.

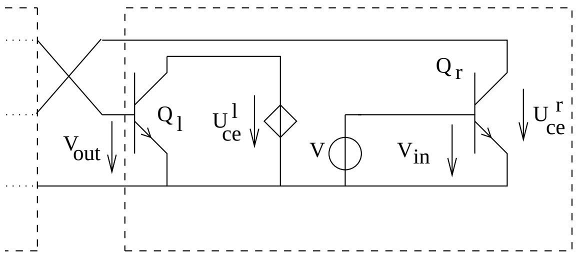

Figure 3: Replacing the bipolar FS-transistor (npn type) by a test circuit.

In the case of circuits consisting of FET's, we replace an FET that belongs to a FS with the circuit shown in Fig. 4 according to the principle of "replacing elements equivalently" as described in [2, 4]).

5.2 Proof of equivalence

It is vital for all replacements that it does not alter the solutions of the circuit. Otherwise, the simulations results will be incorrect.

The circuit operating points are the intersecting points of v_{out} and v_{in}. We prove that at these points the replacement circuit behaves exactly as the original FET that was replaced.

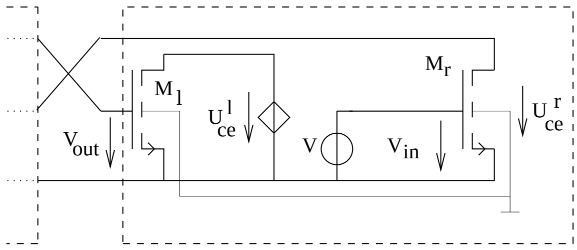

Figure 4: Replacing the MOSFET FS-transistor (n type) by a test circuit.

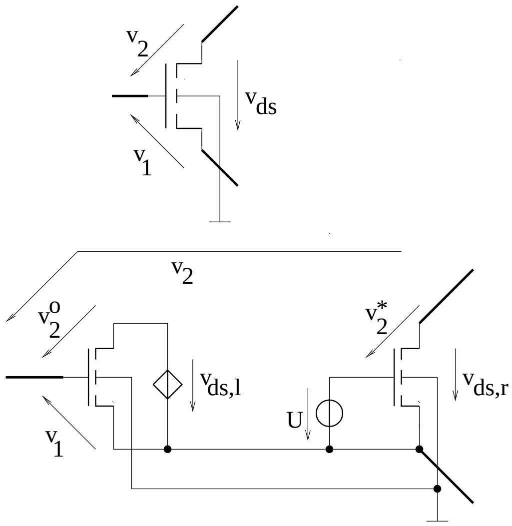

Figure 5: Proof of equivalence: replacing the MOSFET for the feedback test.

Theorem: If $v_1 = -U$, then both replacing transistors have the same voltages and currents, and, hence, the same operating point as the original transistor.

Proof: The proof is analog to the proof given in [2]. It follows from $v_{ds,r} = v_2 - v_1$, with $v_1 = -U$, that $v_{ds,r} = v_2 + U$. With $v_{ds,r} = v_2^* + U$, we obtain $v_2^* = v_2$. From $v_{ds,r} = v_2 - v_1$ and $v_{ds,l} = v_2^0 - v_1$, with $v_{ds,l} = v_{ds,r}$, we find that $v_2^0 = v_2$.

In summary:

$$\begin{aligned} v_1 &= -U \\ v_{ds,l} &= v_{ds,r} \\ v_2^* &= v_2 \\ v_2^0 &= v_2. \end{aligned}$$

Hence all corresponding voltages are identical.

For determining the FET's currents we need to employ an FET model. We choose the Tadeusiewicz model [8] given by Equation (1). The corresponding currents are also identical, i.e.,

$$\begin{matrix} v_1^* = v_1 \\ v_2^* = v_2 \end{matrix} \quad \text{implies} \quad \begin{matrix} i_1^* = i_1 \\ i_2^* = i_2. \end{matrix}$$

Hence, the dc operating points of all three transistors are equivalent. Q.E.D.

5.3 Bulk connection

Until now we always connected the bulk connections of the two replacing FET's to the bulk of the original FET under investigation. The reason is that, usually, the bulk potential in FET circuits is nearly constant. Nevertheless, we have demonstrated that at a dc operating point all other circuit variables are equivalent to those of the replaced transistor. Hence, the bulk potential can not deviate from the original value either.

5.4 Simplified FS-transistor replacement

Due to the large FET's input resistance ($R_{in} \to \infty$), it can be shown that the simplified circuit shown in Fig. 6 is an adequate replacement circuit. Furthermore, because FET's gate-current is zero (irrelevant of the transistor model), we can open the gate terminal without altering the circuit's behavior. For example, this can be observed if the model in Fig. 2 is used to substitute the FET on the left shown in Fig. 5. The reason is that the FET on the left only controls the closed loop current through the source and the drain caused by the controlled source $v_{ds,l}$. Hence, i_d has no effect on the rest of the circuit. Note that this behavior is different from the bipolar transistor case.

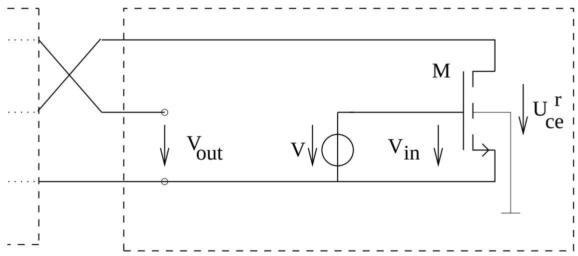

Figure 6: Simplified circuit for testing an n type MOSFET FS-transistor.

5.5 Results of the analysis

According to [2, 4], replacing the FET under investigation implies cutting open the closed feedback loop. After this is done, we increase the dc value of v_{in} and observe the plot $v_{out} = f(v_{in})$. The result is interpreted as in the case discussed in [2, 4], Solutions of $\mathbf{F}(\mathbf{x}) = \mathbf{0}$ are intersection points with

$$v_{out} = v_{in}.$$

The stability of the solution is determined from the slope at the intersection point.

$$\frac{d}{dv_{in}}\, v_{out}(v_{in}) \;<\; 1$$

implies a stable dc operating point, while

$$\frac{d}{dv_{in}}\, v_{out}(v_{in}) \;>\; 1$$

implies an unstable solution. This test must be performed for each transistor that belongs to at least one feedback structure.

6 Principles of the proposed method

The proposed method is based on the fact that elements with characteristics that are monotone and continuous mappings (such as those used in transistor models) may cause multiple dc operating points only if they belong to a *positive* feedback structure. (For op-amp circuits see [1], p. 192.)

The Nielsen-Willson result [7] establishes only necessary topological conditions that *can* cause multiple dc operating points. A feedback structure does not cause multiple dc operating points unless it acts as a *positive* feedback. For each FET belonging to a feedback structure, using the method presented in this paper, we can determine in most cases (see restrictions) the solutions of $\mathbf{F}(\mathbf{x}) = \mathbf{0}$ and *if* this very transistor causes multiple operating points.

7 Restrictions

The results of our method may in some cases depend on the states of other transistors. Even if the simulator converges to "wrong" operating points of *other* transistors, our method correctly determines the dc operating points and their number *for the transistor under investigation.* Nevertheless, this result is false because of the "wrong" dc operating point of the remaining transistors.

From the proof of the equivalence, we can state that the proposed method finds all dc operating points caused by the FS-transistor under investigation *provided* that *all* other transistors are operating at their correct dc operating points.

8 Example: flip-flop circuit

We illustrate the proposed method by using a flip-flop circuit. The SPICE input file for the circuit is:

```
.MODEL modn NMOS1 VTO=1.0
+ GAMMA=0.2 PHI=0.6

Vdd 5 0 5
M1 1 2 0 0 modn W=5U L=2U
M2 2 1 0 0 modn W=5U L=2U

Rc1 1 5 1 30k
Rc2 5 2 30k
```

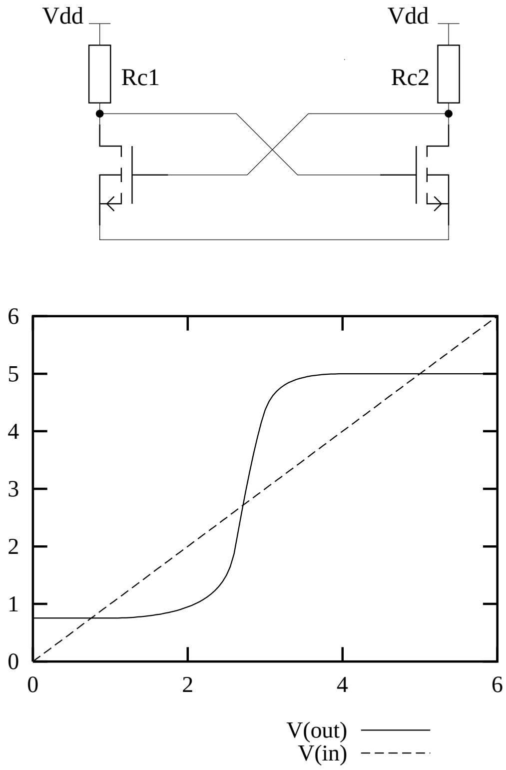

Figure 7: MOSFET flip-flop circuit (top). Results (bottom): dashed line v_{in}, solid line $v_{out}(v_{in})$. Two stable dc operating points located at $V_{in} \approx 0.8V$ and $V_{in} \approx 5V$, and one unstable solution at $V_{in} \approx 2.4V$.

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