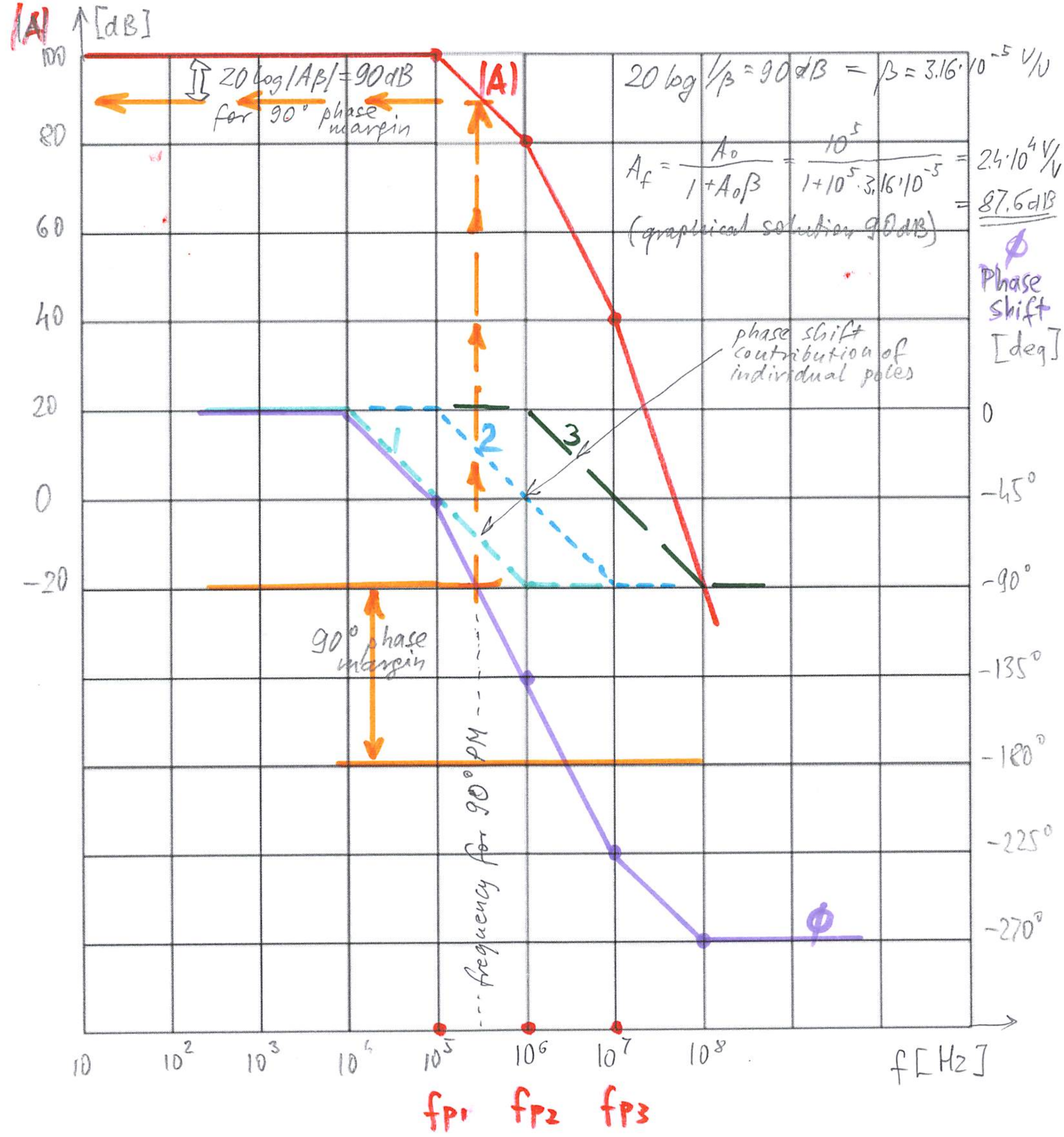
Problem 1

For the three-pole amplifier for which $A_0 = 10^5$ V/V and having poles at 10^5 Hz, 10^6 Hz and 10^7 Hz, and with frequency-independent feedback, what is the minimum closed-loop voltage gain that can be obtained for phase margins of 90° and 45°?



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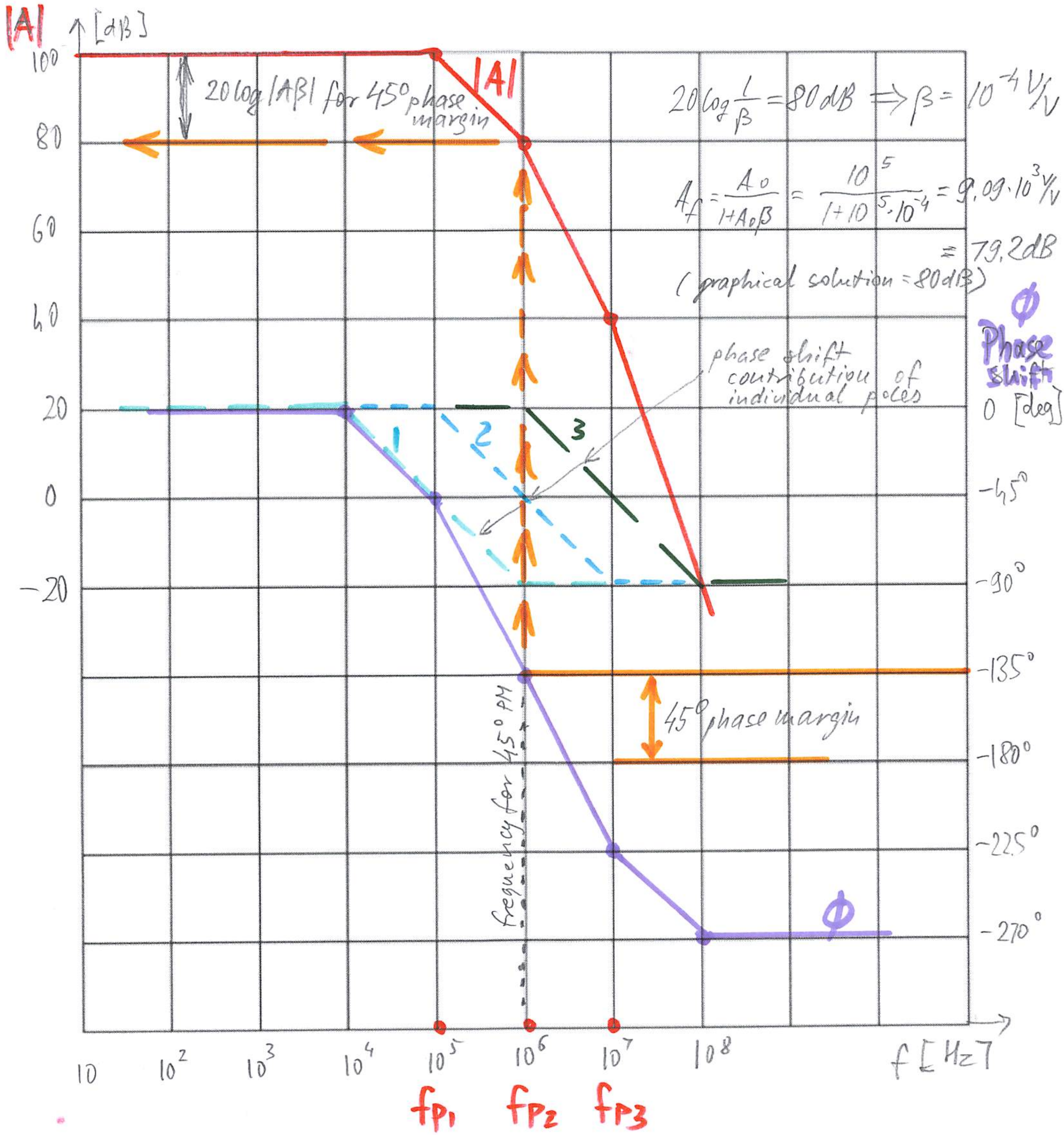

Problem 2

Consider a feedback amplifier for which the open-loop gain A(s) is given by:

$$A(s)=\frac{10{,}000}{\left(1+s/10^4\right)\left(1+s/10^5\right)^2}$$

If the feedback factor β is independent of frequency, find the frequency at which the phase shift is 180°, and find the critical value of β at which oscillation will commence.

Solve the problem using formulas, as well as graphically. Compare both results.

$$A(j\omega)=\frac{10^4}{\left(1+j\frac{\omega}{10^4}\right)\left(1+j\frac{\omega}{10^5}\right)^2}$$

$$A_0 = 20\log(10^4) = 80\,dB$$

phase shift: $\phi = -\tan^{-1}\left(\frac{\omega}{10^4}\right) - 2\cdot\tan^{-1}\left(\frac{\omega}{10^5}\right)$

$$180^\circ = -\tan^{-1}\left(\frac{\omega_{180}}{10^4}\right) - 2\tan^{-1}\left(\frac{\omega_{180}}{10^5}\right)$$

① iteration: assume $\omega_{180} = 10^5$

$$-\tan^{-1}\left(\frac{10^5}{10^4}\right) - 2\tan^{-1}\left(\frac{10^5}{10^5}\right) = -84.3^\circ - 2\cdot 45^\circ = 174.3^\circ$$

② iteration:

assume $\omega_{180} = 1.1\cdot 10^5$

$$-\tan^{-1}\left(\frac{1.1\cdot 10^5}{10^4}\right) - 2\tan^{-1}\left(\frac{1.1\cdot 10^5}{10^5}\right) = -84.8^\circ - 2\cdot 47.7^\circ = 180.2^\circ$$

solution: $\omega_{180} = 1.095\cdot 10^5$ rad/sec

Gain at the ω_{180} frequency: $|A| = \dfrac{10^4}{\sqrt{1+\left(\frac{1.095\cdot 10^5}{10^4}\right)^2}\cdot\left\{\sqrt{1+\left(\frac{1.095\cdot 10^5}{10^5}\right)^2}\right\}^2} = 413.6\ V/V$

$$20\log 413.6 = 52.3\,dB$$

For stable operation:

$$|A|\cdot\beta_{cr} < 1$$

$$413.6\cdot\beta_{cr} < 1$$

$$\beta_{cr} < 2.418\cdot 10^{-3}$$

The oscillation will commence for $\beta \geq 2.42\cdot 10^{-3}$

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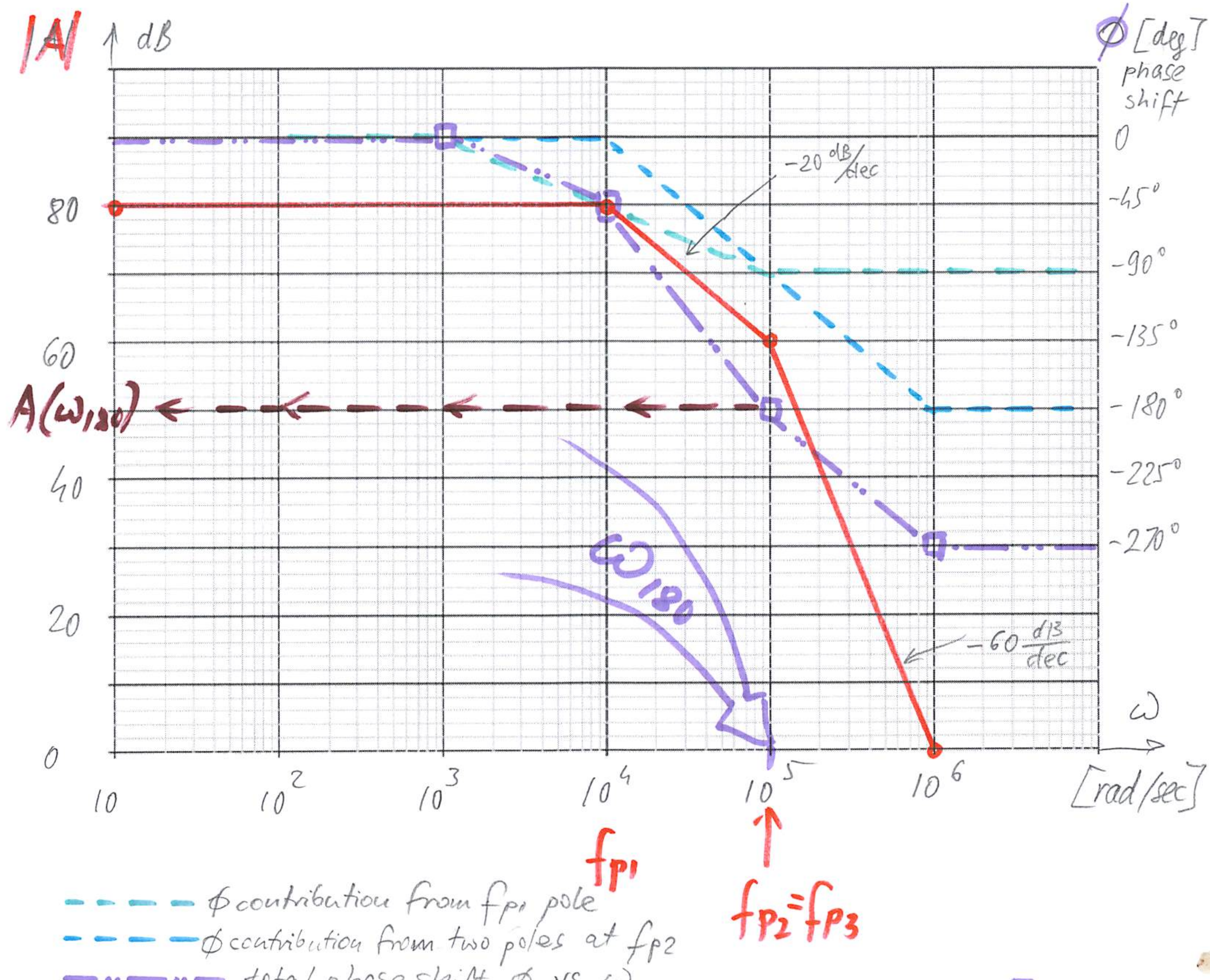


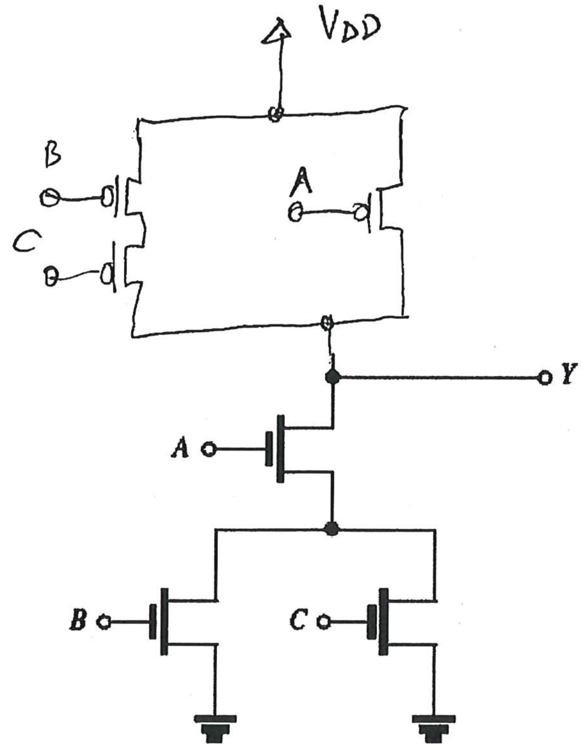
$\omega_{180} \approx 10^5$ rd/sec

A(at ω_{180}) = 50 dB

Problem 3

Find the pull-up network (PUN) that correspond to the pull-down network (PDN) shown below, and hence draw the complete CMOS logic circuit.

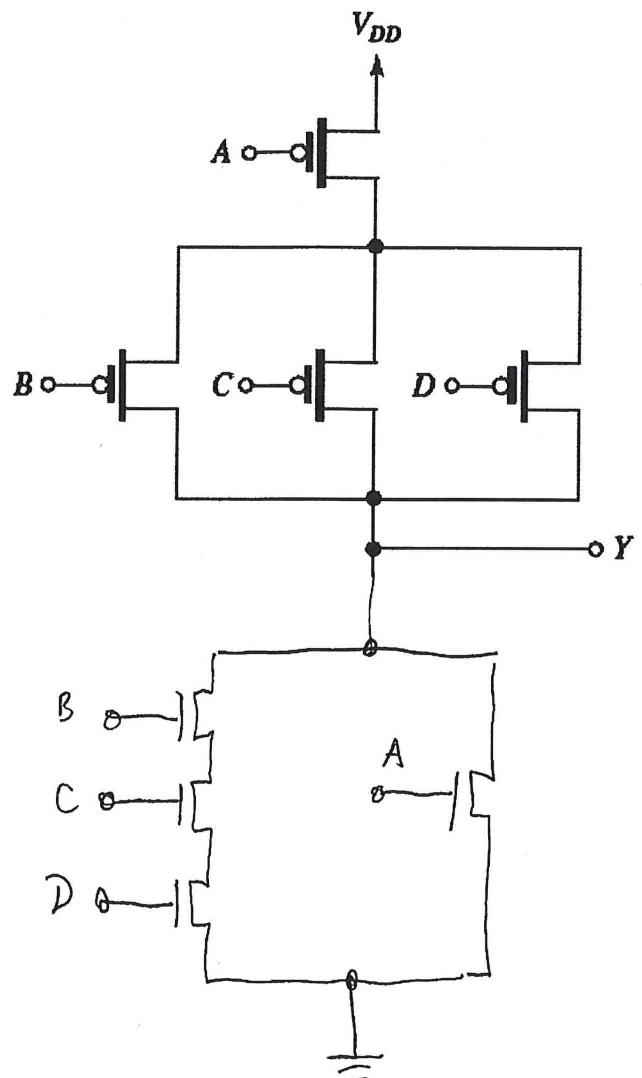
What is the Boolean function realized by this gate?



$Y = \overline{A \cdot (B + C)}$

Problem 4

Find the pull-down network (PDN) that correspond to the pull-up network (PUN) shown below, and hence draw the complete CMOS logic circuit.
What is the Boolean function realized by this gate?



$Y = \overline{A + B \cdot C \cdot D}$