ENSC 325 MICROELECTRONICS II Spring 2022

Experiment 1
Current Mirrors

Due: Feb. 7, 2022, before 4:00 PM.

Lab reports should be delivered to the ENSC 325 bin in the ENSC Receptionist office (ASB 9886). The office closes at 4:00 PM sharp.

In the Title page of the Report there should be a Table declaring the amount of work provided by each member of the Lab Group, in percentage, which must be signed by all members of the Lab Group. All signatures must be hand-written, no electronic signatures are permitted.

The Lab reports must take no more than 10 pages (excluding the title page), single-side printed, single column format, font Times 12. Figures and plots must be a part of the body of the report, and not attached at the end as Appendices. The contents of Appendices, if any are included, will be not graded.

After the Lab report due date, do not disassemble your circuit if possible, but keep it for the Lab demonstration session that will take place soon after the grading is done.

1.0 Objective

In this experiment, we will examine techniques for current biasing. Current biasing using current sources and/or current sinks is a popular biasing technique that permits an easy control of small-signal transconductance values of BJT and MOS transistors. The current source and current sink are circuits whose current should be independent of the voltage across their terminals. Typical requirements for current sources/sinks include high output resistance, wide range of output voltage, and independence from supply variations or temperature variation. A current source/sink connected in parallel with the reference circuit forms the current mirror, in which the output current should mirror the reference current (with some degree of accuracy).

To show your understanding of the lab, your write-up should contain:
- Calculations requested in the Prelab,
- Details on measurement technique(s) applied,
- Results presented in a graphical form,
- Discussion of results.

2.0 Prelab

- Using the material from the textbook and lecture slides calculate the theoretical values of I_{REF}, I_{OUT} and the minimum output voltage required for the circuit to operate as a

current source/sink, V_{MIN}, for all the circuits shown in Figures 1 to 4. Your calculations should be included in your Lab report and compared with measurement results.

• Calculate the output resistances of the current mirrors measured in Sec.3.1(c), 3.2(b), and 3.3(b) and compare them with measurement results.

3.0 Procedure

3.1 Simple NPN Current Mirror

a) Construct the simple current mirror shown in Fig. 1. In the circuit use the BJT transistor pair (V_{BE} mismatch ±5mV) or individual transistors (V_{BE} mismatch slightly worse than ±5mV) from the CA3046 chip. **Make sure that pin 13 (Emitter of Q_5) is ALWAYS connected to $-V_{EE}$** (see Note in p.4). The CA3046 devices are sensitive to electrostatic discharge; follow proper IC handling procedures.

b) Let the power supplies $-V_{EE} = 0$V and $V_{CC} = 10$V, and $R_{REF} = 5$kΩ. Measure the I_{REF} and I_{OUT} currents. Compare with theoretical values of I_{REF} and I_{OUT} using the npn transistor β values from the CA3046 data sheet.

c) Using the same BJT transistors as in (b) construct the circuit shown in Fig.2, with $R_{REF} = 5$kΩ and variable V_{OUT}. Varying the V_{OUT} voltage from 0 to 10V measure the I_{OUT} vs. V_{OUT} characteristics of the current mirror. From the plot, find the V_{MIN} and the small-signal output resistance.

d) Compare the measured output resistance and V_{MIN} with the theoretical values calculated in the Prelab, and discuss the results.

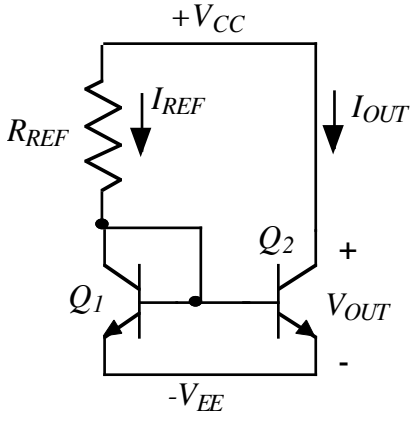


Figure 1

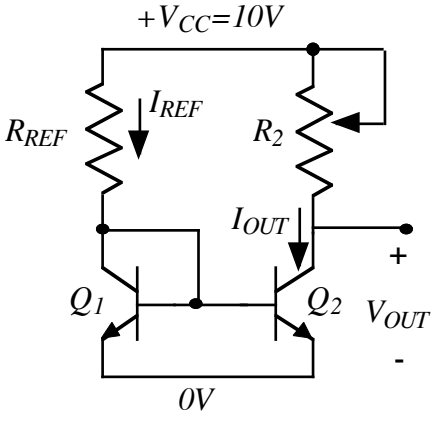


Figure 2

3.2 Simple PNP Current Mirror

a) Construct the circuit shown in Fig.3. As BJT transistors, use two discrete PNP BJTs 2N3906 and R_{REF}=5kΩ. In order to match the transistor V_{BE} voltages, use two 200Ω trimpots (R_1 and R_2). Adjust R_1 and R_2 so the $I_{REF} = I_{OUT}$, while both R_1 and R_2 have **minimum** values. A proper adjustment will require one resistor (R_1 or R_2) as close to zero as possible *). This procedure is a substitute for having two matched PNP BJTs in this experiment.
Arrange resistors R_1 and R_2 for the condition $I_{REF} = I_{OUT}$ when $-V_{EE}$=0V, V_{CC}=10.0V, and V_{OUT}=0V.

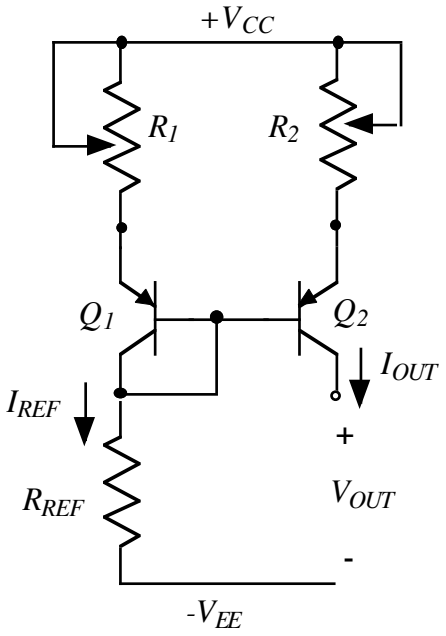


Figure 3

b) Keeping the R_1 and R_2 as set up in Sec.3.2(a), as well as $-V_{EE} = 0V$, $V_{CC} = 10V$, and $R_{REF} = 5k\Omega$, measure and plot the output current I_{OUT} of the current mirror for V_{OUT} in the range from 0V to 5V. Draw the circuit diagram of your test circuit and explain the method that you used to measure this characteristic. From the data find the small-signal output resistance of the current mirror.

c) Compare the measured output resistance with the theoretical value calculated in the Prelab, and discuss the results.

*) too large R_1 and R_2 values would lead to the cascode effect and the output resistance increasing

3.3 NPN Cascode Current Mirror

a) Construct the circuit shown in Fig. 4. As BJT transistors, use four NPN transistors from the BJT transistor array CA3046 and R_{REF} = 5kΩ. Measure the I_{REF} and I_{OUT} currents for the power supplies $-V_{EE}$ = 0V and $V_{OUT} = V_{CC}$ = 10V. Compare with theoretical values of I_{REF} and I_{OUT} using the β values from the CA3046 data sheet.

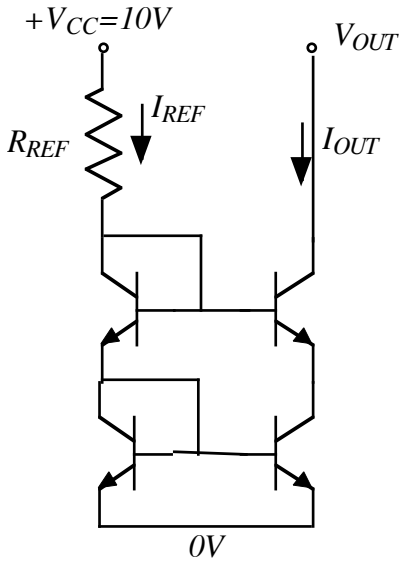


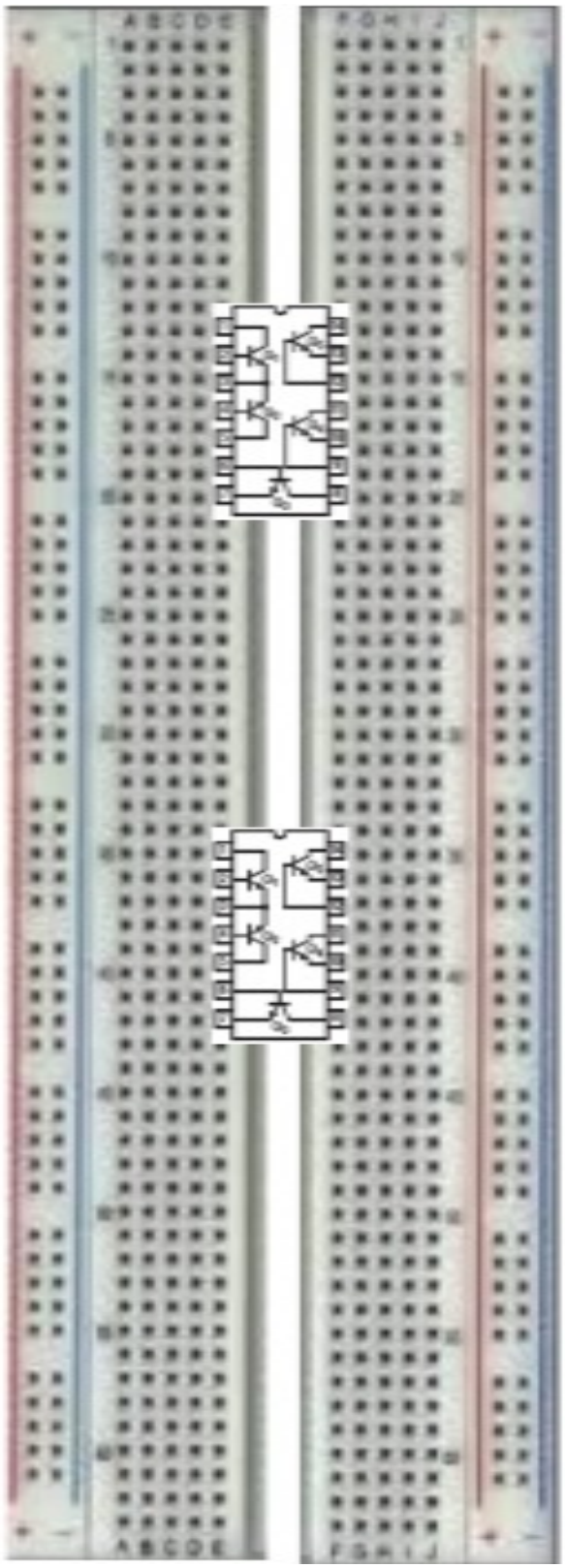
Figure 4

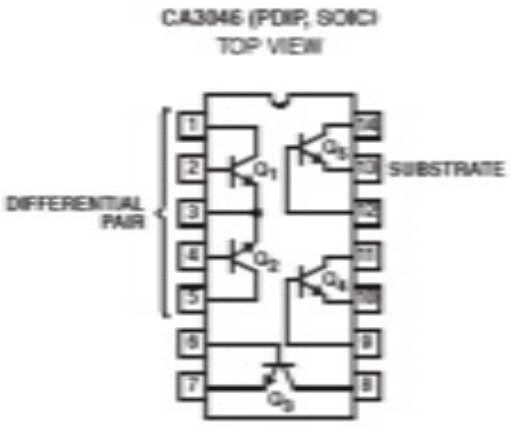
b) Using the same procedure as in Sec.3.1(c), measure the I_{OUT} vs. V_{OUT} characteristics of the current mirror within the V_{OUT} voltage range from 0 to 10V. From the plot, find the V_{MIN} and the small-signal output resistance.

c) Compare the measured output resistance and V_{MIN} with the theoretical values calculated in the Prelab, and discuss the results.

NOTE from CA3046 Data sheet

The collector of each transistor of the CA3046 is isolated from the substrate by an integral diode. The substrate (Terminal 13) must be connected to the most negative point in the external circuit to maintain isolation between transistors and to provide for normal transistor action.





It is recommended that you will use this template to draw interconnections between transistors BEFORE attempting to assemble the circuits shown in Figs. 1 to 4 on the protoboard. This drawing is very helpful in assembling and debugging your circuit.