ENSC 325 MICROELECTRONICS II Spring 2022

Experiment 4

CMOS Two-Stage Amplifier

Due: Mar. 30, 2022

• Lab reports should be delivered to Marek after the lecture (10:20AM) or to Marek's office ASB 8837 before 4:00 PM on the due day.

1.0 Objective

In this experiment, we will build a two-stage CMOS amplifier (Fig.1) and examine its properties. The amplifier will be build of individual MOS transistors available in the form of MC14007 MOS transistor arrays. Each MC14007 chip will provide three identical either n-channel or p-channel MOS transistors (Fig.2).

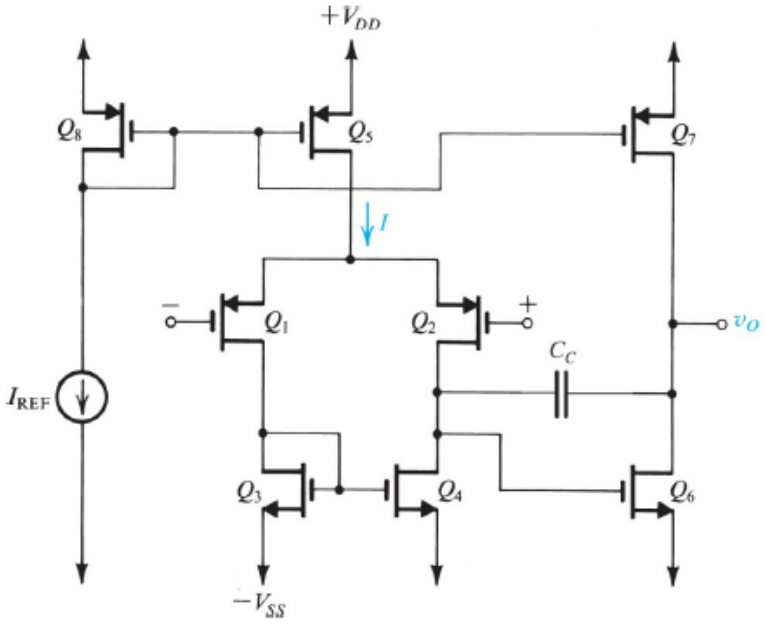

Figure 1. Two-stage CMOS op-amp with frequency compensation

2.0 Pre-lab (must be done before the experiment part)

A two-stage CMOS amplifier is shown in Fig.1. Assume that all n-channel MOS transistors and all p-channel MOS transistors have the output characteristics as shown in Fig.3 and Fig.4 (MC14007 data sheet). These characteristics show the current of the MOS transistor for the condition $|V_{DS}| = |V_{GS}|$ only. Evaluate and specify transistor model parameters (threshold voltages V_{Tp} and V_{Tn}, transconductance parameters K_n and K_p, and Early voltages) directly from these output characteristics. Report your procedure and the extracted model parameters.

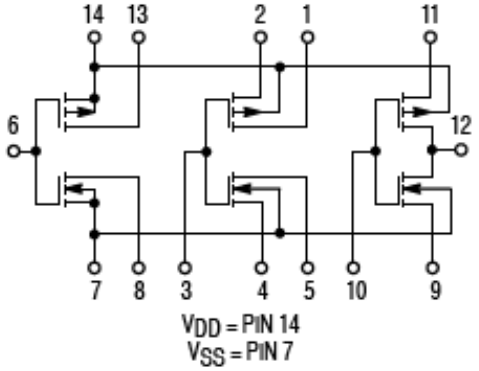

Figure 2. MC14007 Schematic diagram

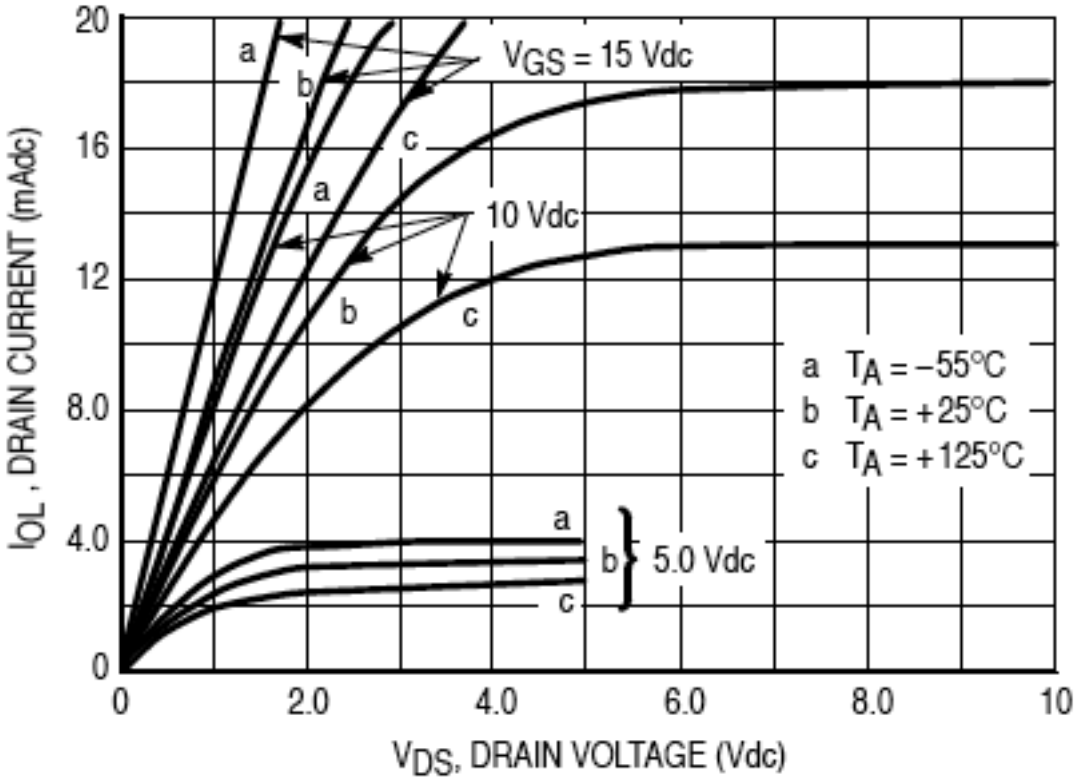

Figure 3. N-channel MOS characteristics

In the amplifier, implement the Q_6 and Q_7 as a parallel connection of a few (3) MOS transistors to increase their equivalent aspect ratio W/L (and also the bias current and transconductance). Make sure that at least one of these three parallelly-connected p-channel transistors implementing Q_7 comes from the same chip as the Q_8 and Q_5 transistors.

Calculate the expected voltage gain A_d and the pole frequencies f_{p1} and f_{p2} of the two-stage op-amp without compensation. Report your calculations of the expected values of A_d, f_{p1} and f_{p2}.

Correct calculation of CMOS op amp parameters is sufficient. Circuit simulations is not needed. If you decide to perform the circuit simulation, there are two models of MC14007 transistors included on the course web. Be aware that model LEVEL=3 does not use LAMBDA as a parameter to model channel-length modulation effect.

3.0. Procedure

- **<u>Always ground your body while handling CMOS chips.</u>**
- Build the two-stage op-amp from the MC14007 CMOS transistor arrays, without the compensating capacitor, making sure that MOS transistors that must be matched come from the same chip. The templates in Figs. 5 and 6 should be helpful to design interconnection pattern on the prototype board before the final assembly is attempted.

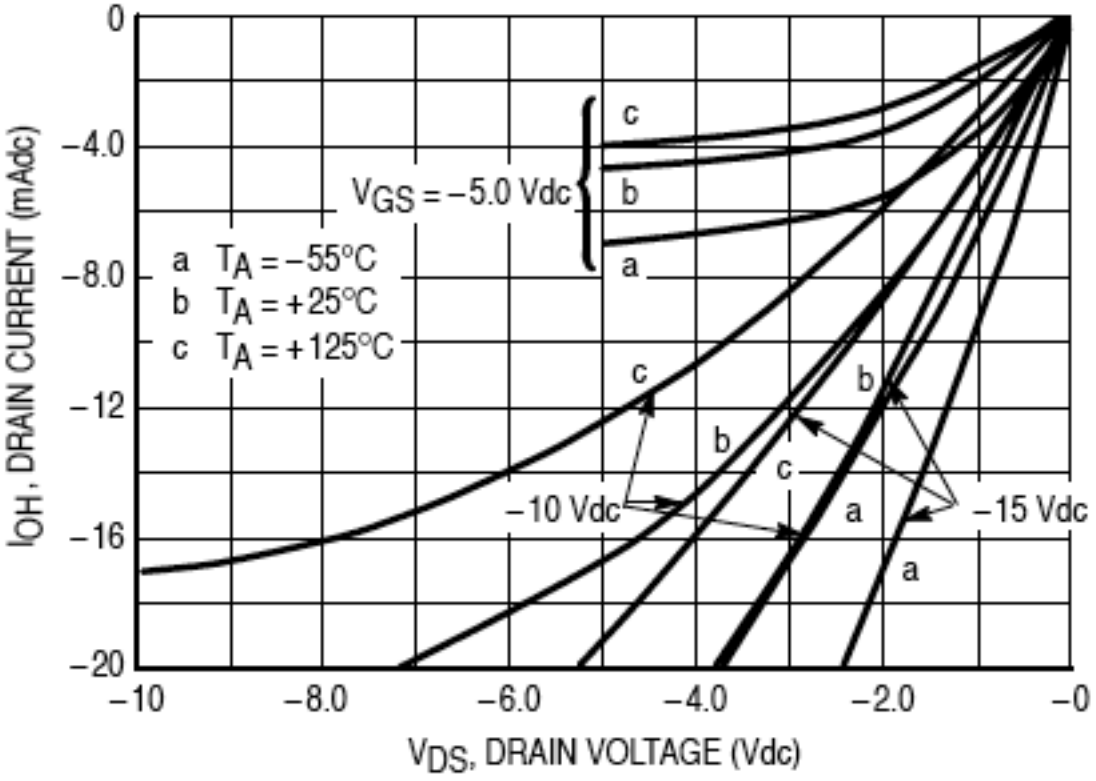

Figure 4. P-channel MOS characteristics

a) Construct the two-stage op-amp shown in Fig.1 using the power supplies *Vss* = 0V and V_{DD} = 10V. Measure the dc voltages and biasing currents. Compare them with the results of your circuit analysis. Include results and the discussion in the lab report.
b) Measure the differential-mode voltage gain vs. frequency starting from 1kHz and plot it (Bode plot - gain in dB vs. frequency using logarithmic scale). Find graphically the upper -3dB frequency. Plots should include data points.

c) Measure the common-mode voltage gain starting from 1kHz. Calculate and plot *CMRR* (*CMRR*'s Bode plot).
d) Connect the compensating capacitor C_C = 10pF. Investigate and report how the connection of the compensating capacitance changed the frequency characteristics of the op-amp.
e) Discuss the results.

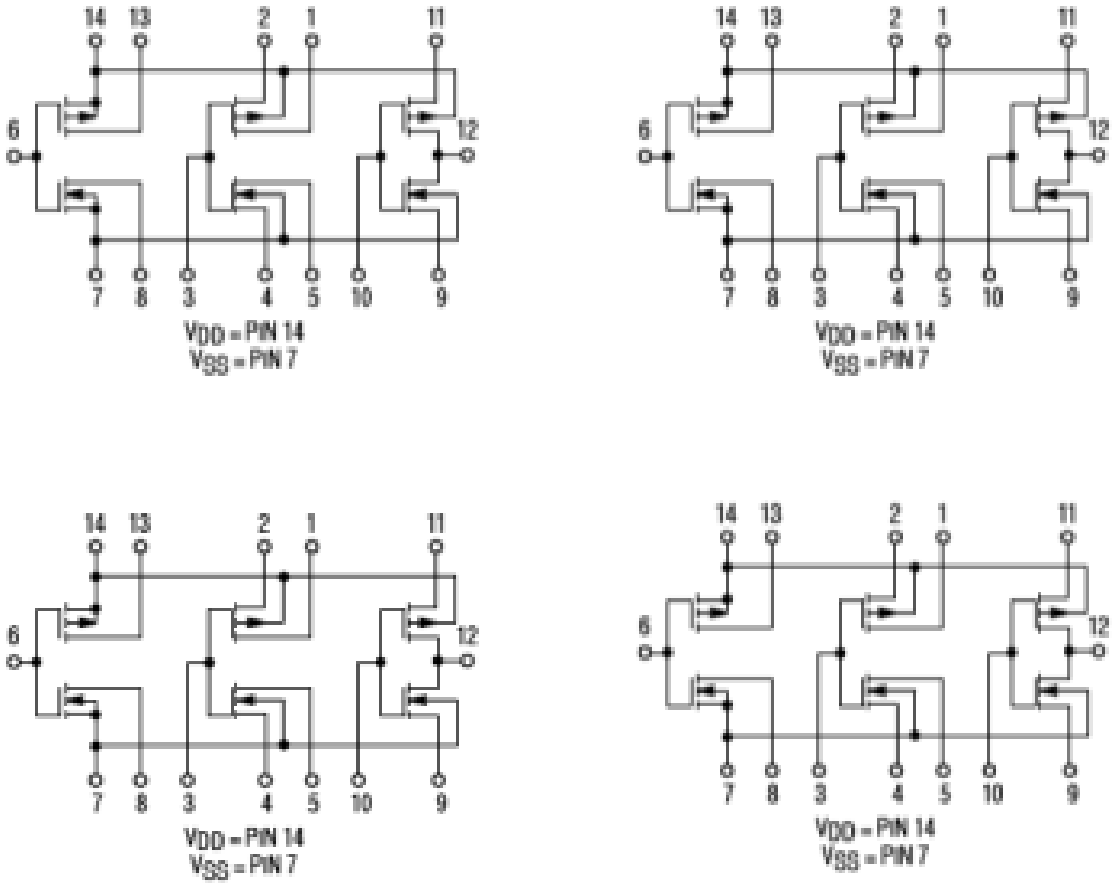

Figure 5. MC14007

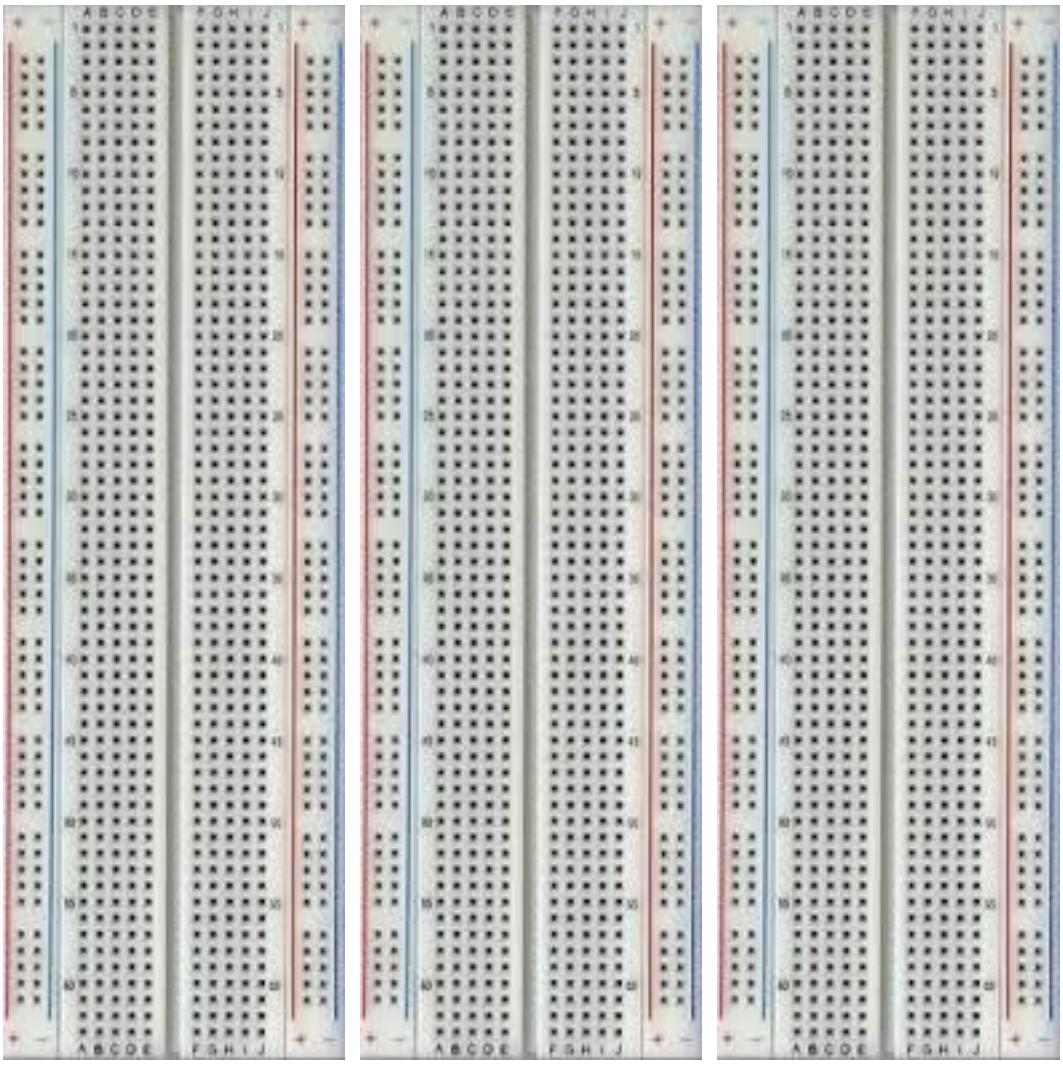

Figure 6

MOS transistor parameter extraction procedure:

$$I_D = K_N \left(V_{GS} - V_{TN}\right)^2 \left(1 + \frac{V_{DS}}{V_{AN}}\right) \qquad \text{(n-channel MOS)}$$

[A] For the n-channel MOS transistor

1) Using two values of I_D for two different V_{DS} and the same V_{GS} calculate V_A
2) Using two values of I_D for two different V_{GS} (V_{DS} does not need to be the same) find V_T
3) Having identified V_A and V_T, calculate K_N

[B] Repeat the procedure for the p-channel MOS