Microelectronics II - ENSC 325 - Spring 2022

° Textbook

ISBN 978-0-19-933913-6, 7th edition,
or 8th edition, Oxford University Press

° Oxford Learning link to 8e resources

https://learninglink.oup.com/access/sedra8e-student-resources#tag_all-chapters

° Lectures

Mondays	08:30 - 10:20, AQ 3159
Wednesdays	08:30 - 09:20, AQ 3159

° Tutorials

Wednesdays	09:30 - 10:20, AQ 3159

Lectures, tutorials and office hours will be on-line till Jan. 24, then back to normal

° Prerequisite

ENSC 225 (Microelectronics I)

° Labs

Hardware Lab - Lab 1 (after Jan. 24)
Computer Lab - circuit simulation using LTspice (or HSPICE in ESIL)

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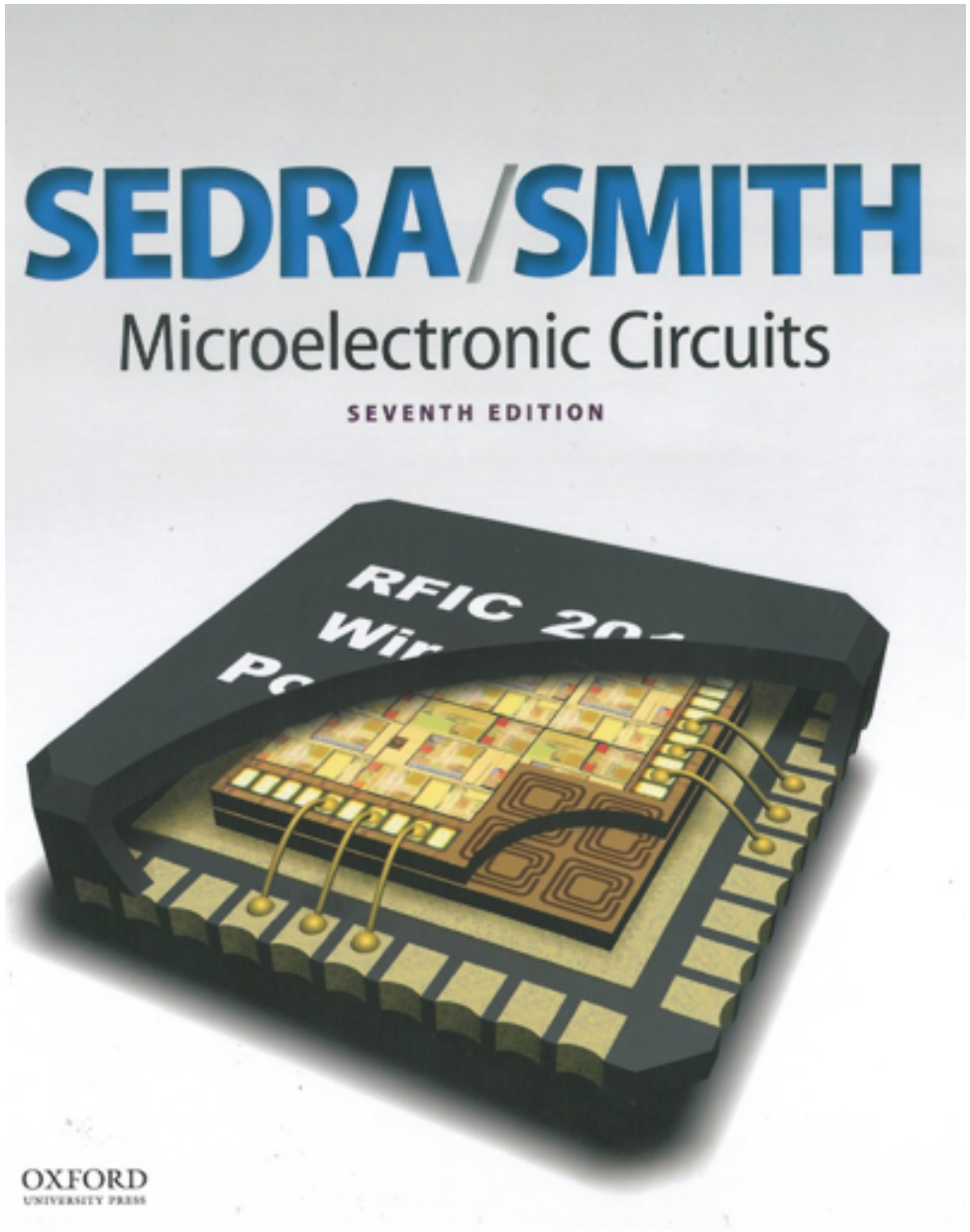

° Instructor

Marek Syrzycki, syrzycki@sfu.ca

Office hours: Wednesday, 13:00-14:00, ASB 8837

° Teaching Assistants

Nicholaus Zilinski, nzilinsk@sfu.ca

Office hours: Thursday, 13:00 - 14:00, Lab 1

Hamidreza Ghanbari, hamidreza_ghanbari@sfu.ca

Office hours: Tuesday, 10:30 - 11:30, Lab 1

Office hours on-line before Jan.24

° Course web page

www.sfu.ca/~syrzycki/325

user id: ENSC325

password protected

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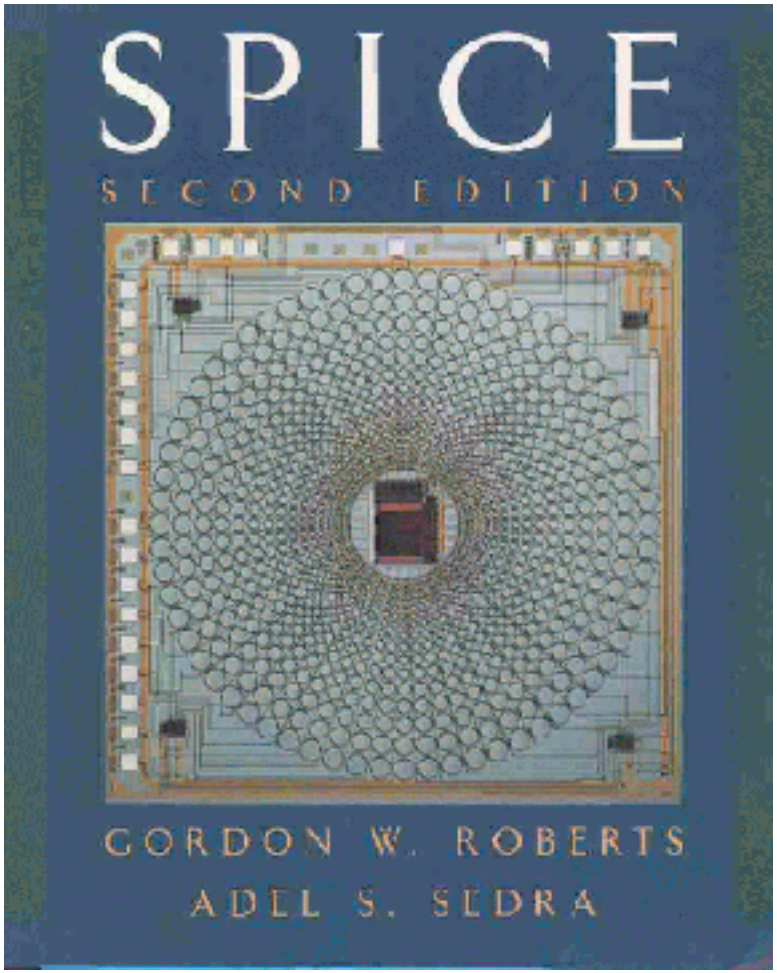

- **Supplementary textbook**

  Oxford University Press

  ISBN: 0195108426

- **Book web page**

  www.macs.ee.mcgill.ca/~roberts/ROBERTS/SPICE

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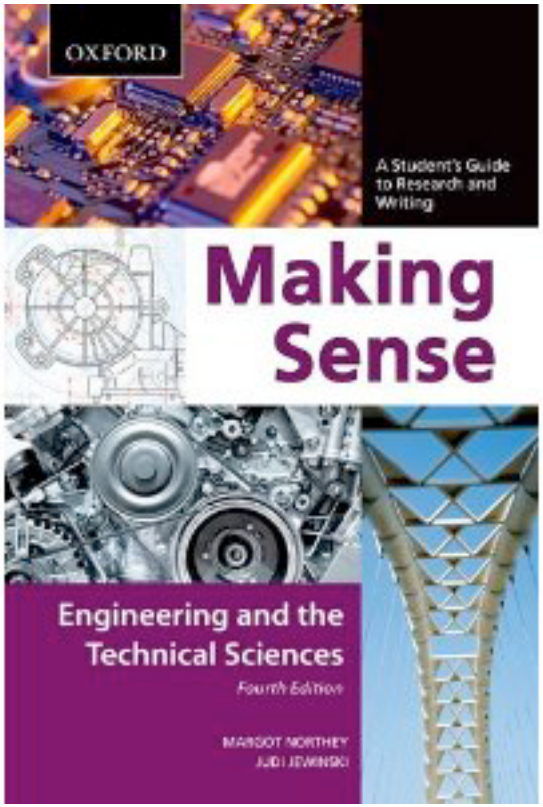


- **Supplementary textbook**

Oxford University Press, 4th Edition

ISBN: 978-0-19-544584-8

- **A note to the student**

"This book has been developed for students of the engineering and technical sciences. Its purpose is to provide a framework for first conducting research and then writing clearly and comprehensively....

...This book will show you how to refine your research and writing skills so that you can present your ideas professionally both on paper and in person."

Course grading policy

• Hardware Labs (4)	50%
• Quizes (4)	50%
• Homework assignments (4)	not graded

Taking all quizes is mandatory. No makeup quizes are planned.

Each Lab Team in the Lab 1 will have 2 students and one parts kit.

Hardware Lab - starts after Jan. 24

Four experiments

- Current mirrors
- Differential amplifiers
- BJT multistage amplifier
- CMOS two-stage operational amplifier

Parts kit

Quantity	Part	Description
5	CA 3046	General purpose NPN transistor array (5 x NPN's), Intersil, 14-PID
6	2N 3904	General purpose NPN transistor, Fairchild, TO-92
6	2N 3906	General purpose PNP transistor, Fairchild, TO-92
4	2N 7000	N-channel enhancement typo MOS FET, Fairchild, TO-92
1	LM 324	Quad 741-type op amp, 14-Plastic Dual-In-Line
6	MC14007	Dual CMOS pair plus CMOS inverter, Motorola
2	PV36ser	Trimpot, 200 ohms, 25 turns, MuRata, Digi-Key 490-2936-ND
2	PV36ser	Trimpot, 1 kiloohm, 25 turns, MuRata, Digi-Key 490-2931-ND
2	PV36ser	Trimpot, 10 kiloohm, 25 turns, MuRata, Digi-Key 490-2932-ND
2	10pF	Capacitor, disc ceramic
2	33pF	Capacitor, disc ceramic
2	100pF	Capacitor, disc ceramic
2	330pF	Capacitor, disc ceramic
2	10µF/15V	Capacitor, electrolytic

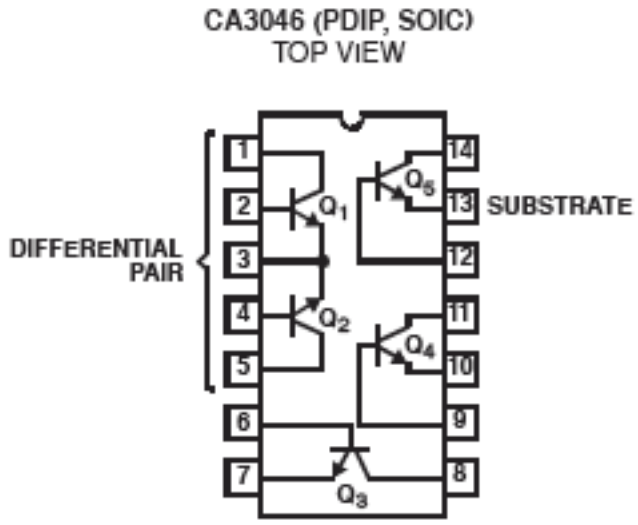
Software Lab

- LTspice software tool will be used in the ENSC 325
  - downloadable to your computers from:

https://www.analog.com/en/design-center/design-tools-and-calculators/ltspice-simulator.html

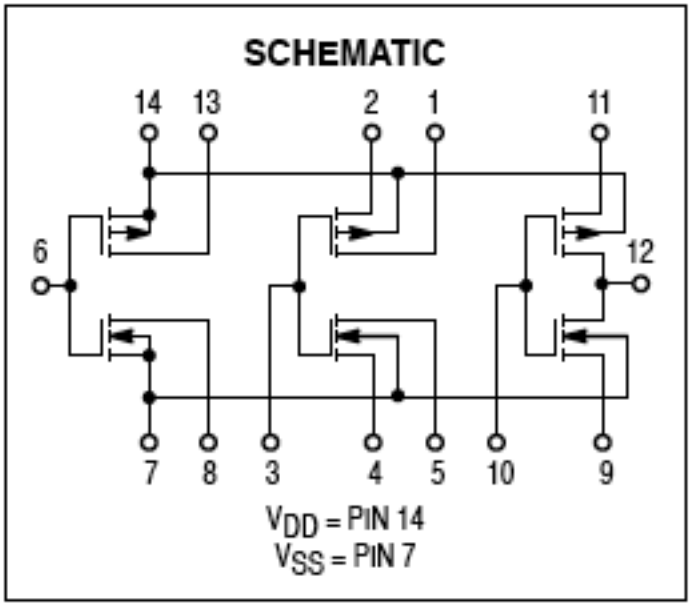
- HSPICE in ESIL is available and can be also used
- Spice circuit simulator must be used with appropriate device models and/or model libraries

npn BJT array CA3046



Differential pair plus 3 matched BJTs

CMOS transistor array MC14007



Dual complementary pair plus CMOS inverter

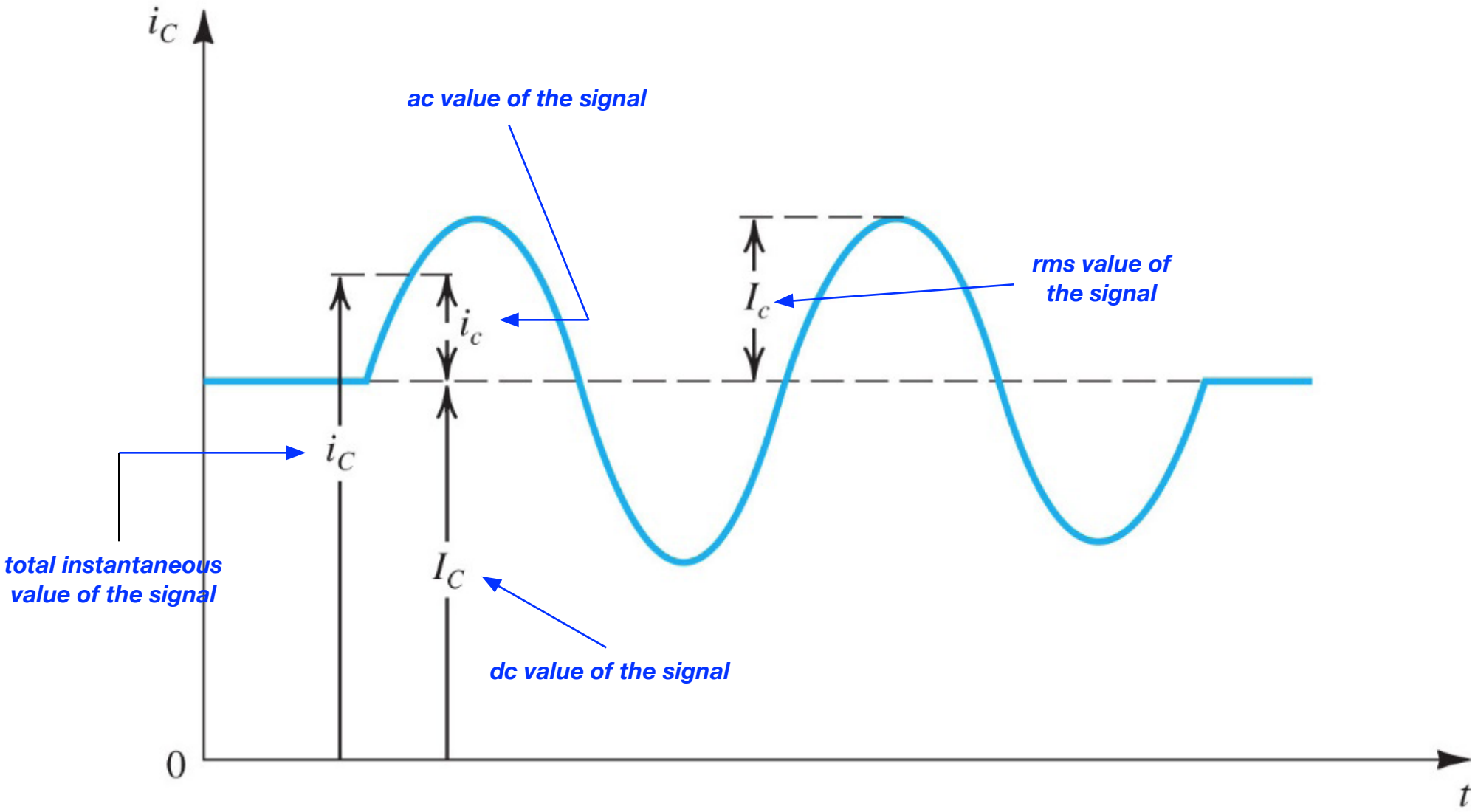
Tentative schedule of lectures

Wk	Date		L	H	Q	Lecture Topic	7th Ed.
1	Jan 10	M				Course overview. Current sinks and sources.	8.1 - 8.2
1	Jan 12	W				Simple current mirrors. Single-stage integrated amplifiers with active loads.	8.2 - 8.3
2	Jan 17	M		H1		Cascode amplifiers. Transistor pairs.	8.5, 8.7
2	Jan 19	W				Improved current mirrors.	8.6
3	Jan 24	M	L1	H1d		BJT differential amplifiers.	9.2 - 9.4
3	Jan 26	W		H2		MOS differential amplifiers.	9.1
4	Jan 31	M				Differential amplifiers with active load.	9.5
4	Feb 2	W			Q1	Frequency response of differential amplifiers.	10.7
5	Feb 7	M	L1d/L2	H2d		Multistage amplifiers.	9.6
5	Feb 9	W				Output stages of op amps.	12.1 - 12.7
6	Feb 14	M		H3		Simple operational amplifier (741 op amp) structure.	13.3
6	Feb 16	W			Q2	741 op amp analysis and parameters.	13.3
7	Feb 28	M	L2d/L3			Modern designs of BJT op amps.	13.4
7	Mar 2	W				Power devices and power IC amplifiers.	12.8 - 12.10
8	Mar 7	M		H3d		CMOS op amps – two-stage op amp.	13.1
8	Mar 9	W				CMOS op amps – two-stage op amp.	13.1
9	Mar 14	M	L3d/L4			Folded cascode op amp.	13.2
9	Mar 16	W			Q3	Feedback amplifiers	11.1 - 11.6
10	Mar 21	M		H4		Stability of feedback amplifiers.	11.7 - 11.8
10	Mar 23	W				Frequency compensation techniques.	11.9 - 11.10
11	Mar 28	M				Digital logic inverters. CMOS inverter.	14.2 - 14.3
11	Mar 30	W	L4d	H4d		CMOS static logic gates.	14.1
12	Apr 4	M				CMOS pass-transistor logic circuits. CMOS dynamic digital circuits.	15.4, 15.5
13	Apr 6	W			Q4	Latches and registers.	16.1
13	Apr 11	M				Semiconductor memories	16.2 - 16.5

Important things to remember

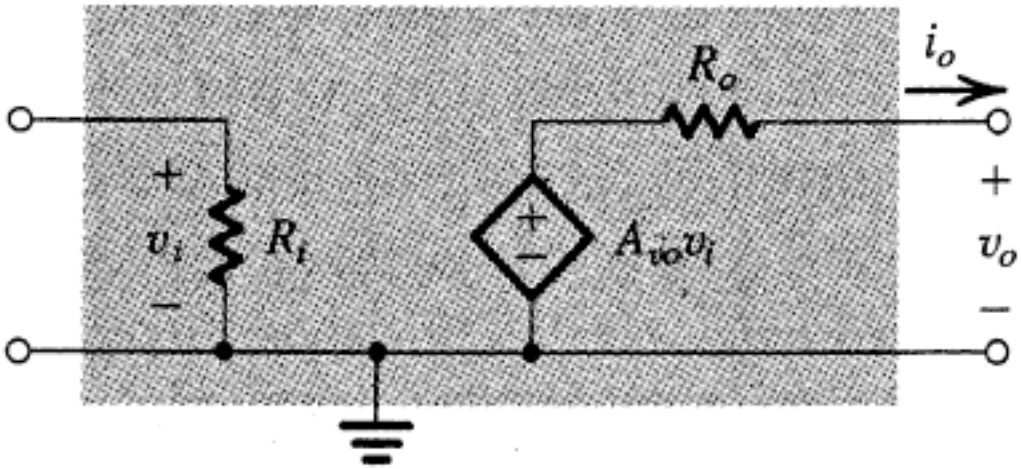
from ENSC 225

Symbol notation for signals



Source: Sedra/Smith "Microelectronic Circuits", 7th Ed, Oxford University Press

Voltage amplifier



Gain Parameter

Open-Circuit Voltage Gain

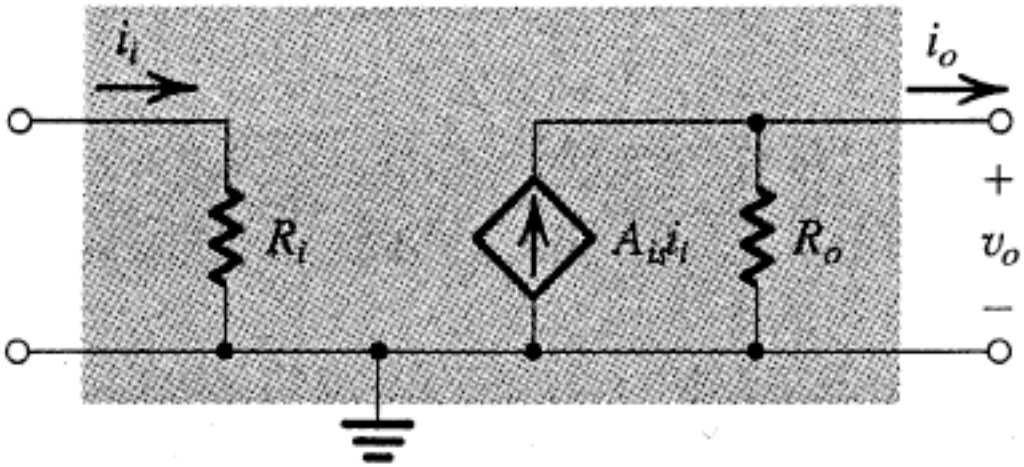
$$A_{vo} \equiv \left.\frac{v_o}{v_i}\right|_{i_o=0} \quad (\text{V/V})$$

Ideal Characteristics

$$R_i = \infty$$

$$R_o = 0$$

Current amplifier



Gain Parameter

Short-Circuit Current Gain

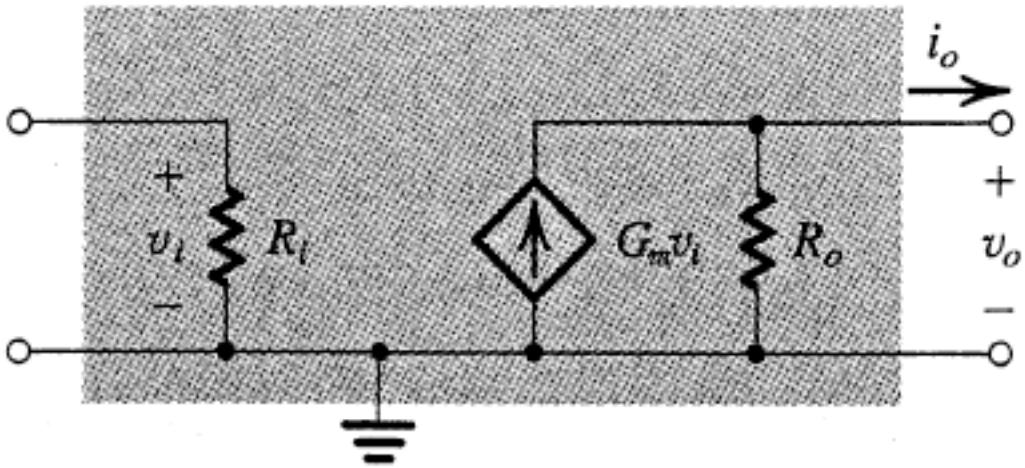
$$A_{is} \equiv \left.\frac{i_o}{i_i}\right|_{v_o=0} \quad \text{(A/A)}$$

Ideal Characteristics

$$R_i = 0$$

$$R_o = \infty$$

Transconductance amplifier



Gain Parameter

Short-Circuit Transconductance

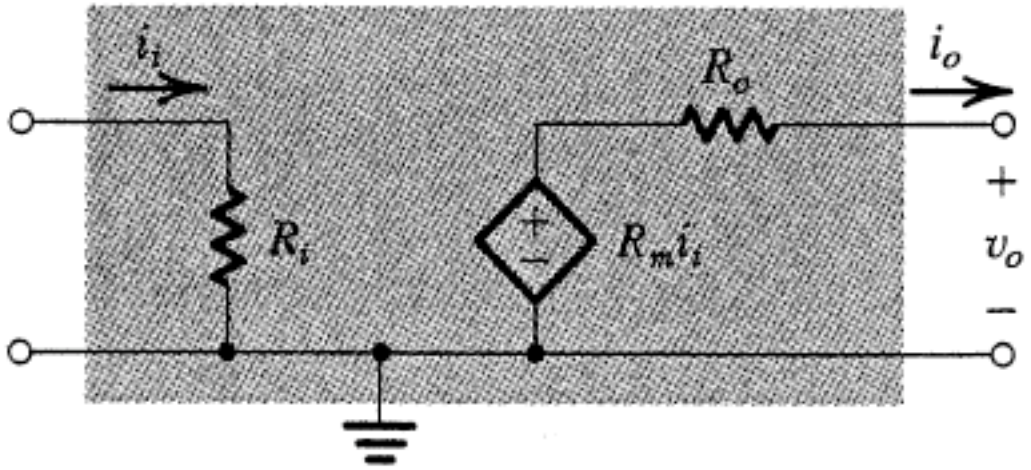
$$G_m \equiv \left.\frac{i_o}{v_i}\right|_{v_o=0} \quad \text{(A/V)}$$

Ideal Characteristics

$$R_i = \infty$$

$$R_o = \infty$$

Transresistance amplifier



Gain Parameter

Open-Circuit Transresistance

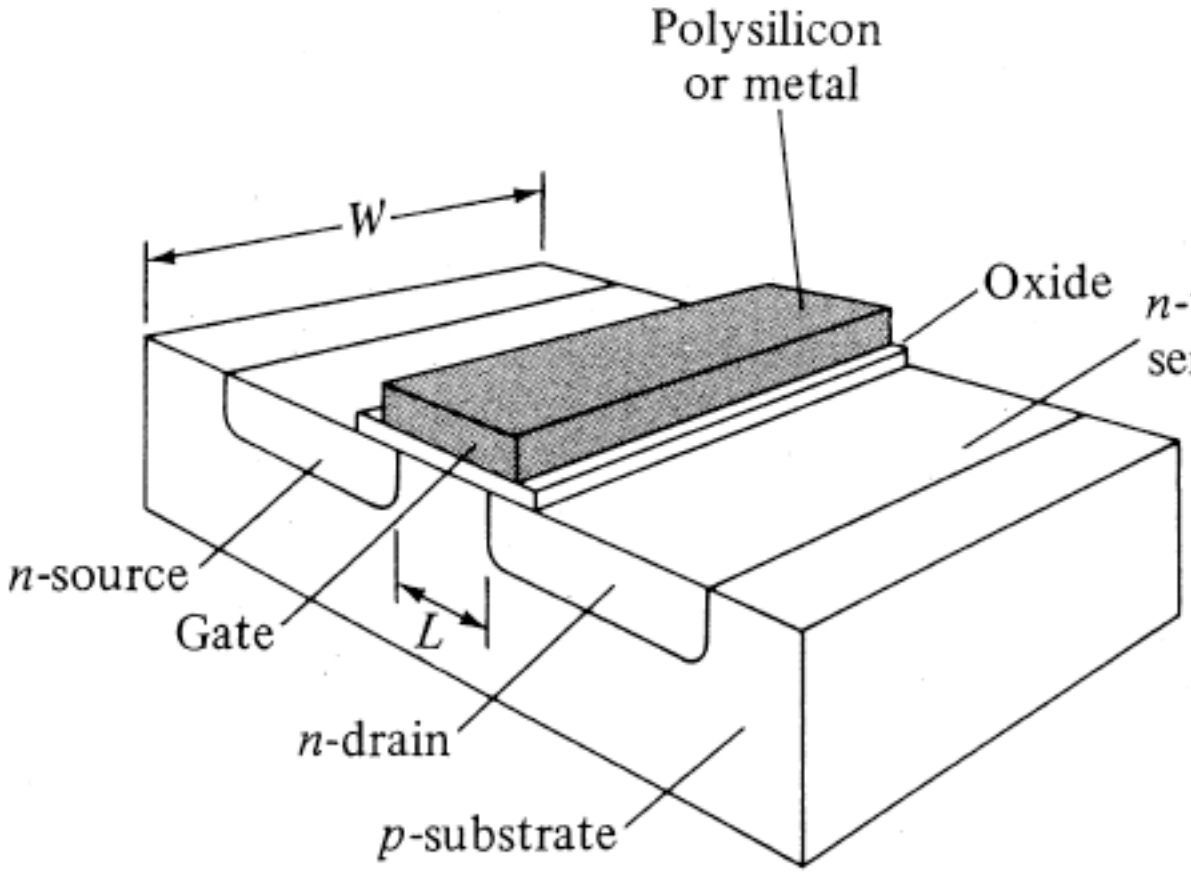
$$R_m \equiv \left.\frac{v_o}{i_i}\right|_{i_o=0} \quad \text{(V/A)}$$

Ideal Characteristics

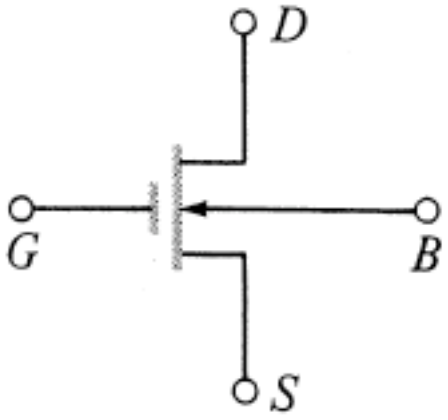
$$R_i = 0$$

$$R_o = 0$$

MOS transistor



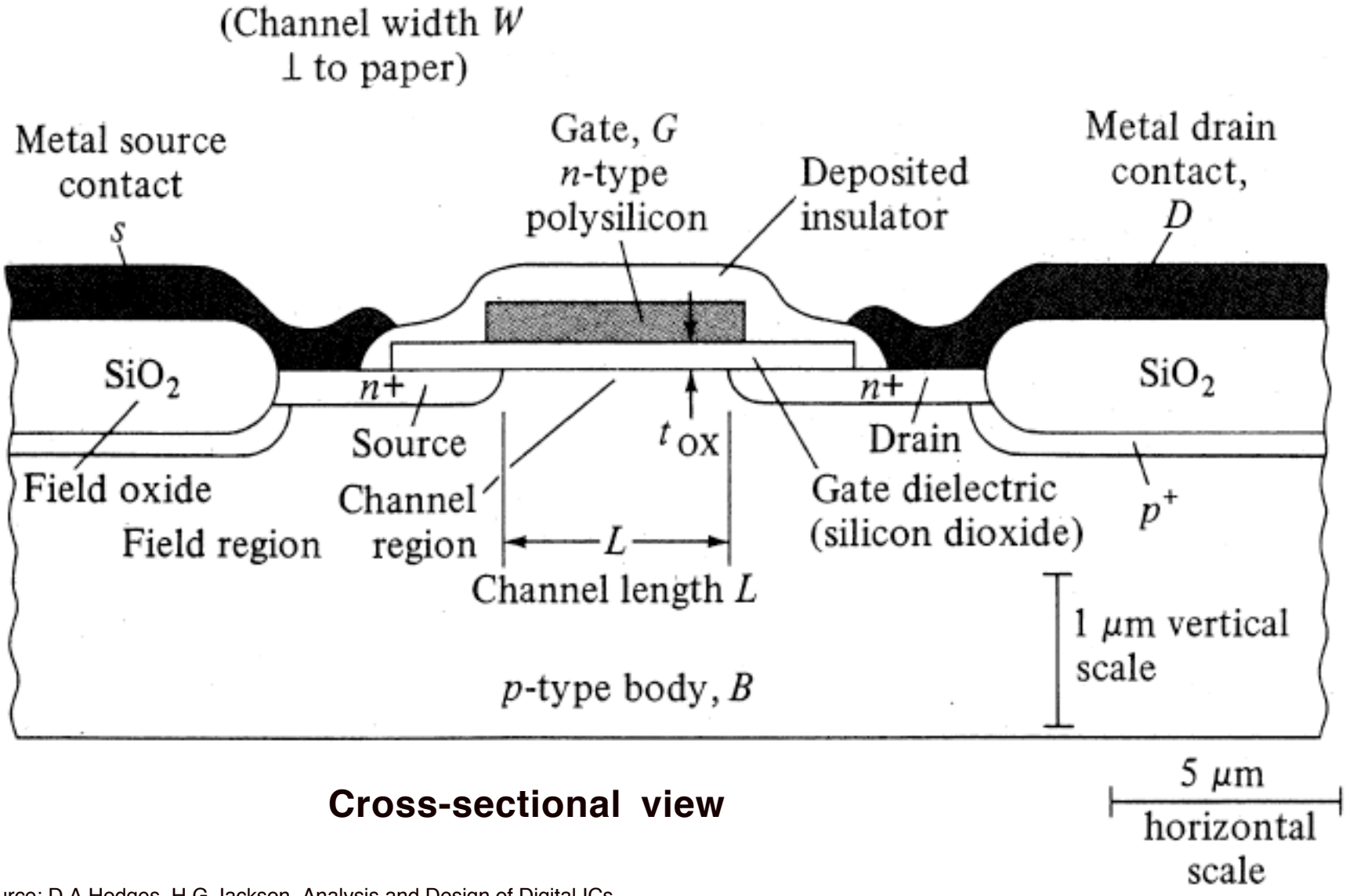
structure



schematic symbol

Source: D.A.Hodges, H.G.Jackson, Analysis and Design of Digital ICs

MOS transistor

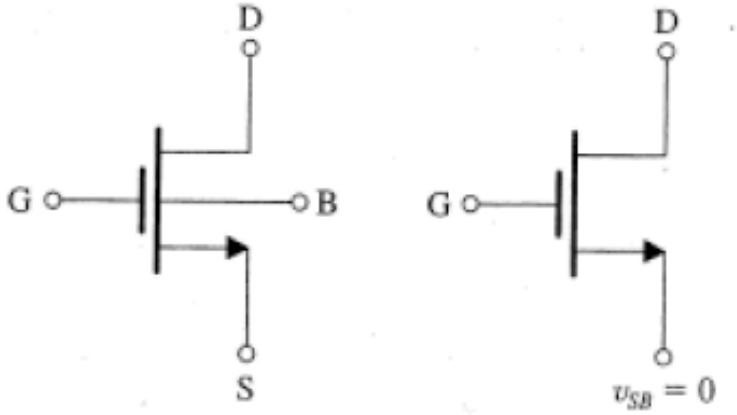


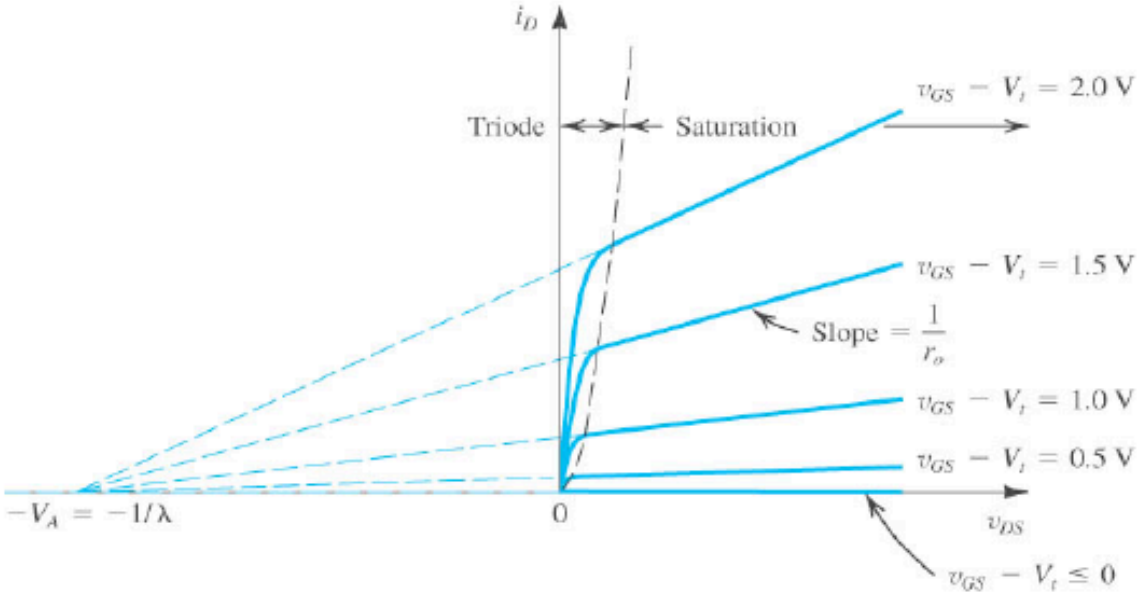
Cross-sectional view

Source: D.A.Hodges, H.G.Jackson, Analysis and Design of Digital ICs

I-V characteristics of MOS transistors

Symbol:





Operation in the *triode* region:

$$v_{GS} \ge V_t \qquad v_{DS} \le v_{GS} - V_t$$

$$i_D = \mu_n C_{ox} \frac{W}{L}\left[(v_{GS} - V_t)v_{DS} - \frac{1}{2}v_{DS}^2\right]$$

Operation in the *saturation* region:

$$v_{GS} \ge V_t \qquad v_{DS} \ge v_{GS} - V_t$$

$$i_D = \frac{1}{2}\mu_n C_{ox} \frac{W}{L}(v_{GS} - V_t)^2(1 + \lambda v_{DS})$$

Threshold voltage:

$$V_t = V_{t0} + \gamma(\sqrt{2\phi_f + |V_{SB}|} - \sqrt{2\phi_f})$$

$C_{ox} = \varepsilon_{ox}/t_{ox}$	(F/m^2)
$k_n' = \mu_n C_{ox}$	(A/V^2)
$V_A' = (V_A/L)$	(V/m)
$\lambda = (1/V_A)$	(V^{-1})
$\gamma = \sqrt{2qN_A\varepsilon_s}/C_{ox}$	$(\text{V}^{1/2})$

$\varepsilon_0 = 8.854 \times 10^{-12}$ F/m

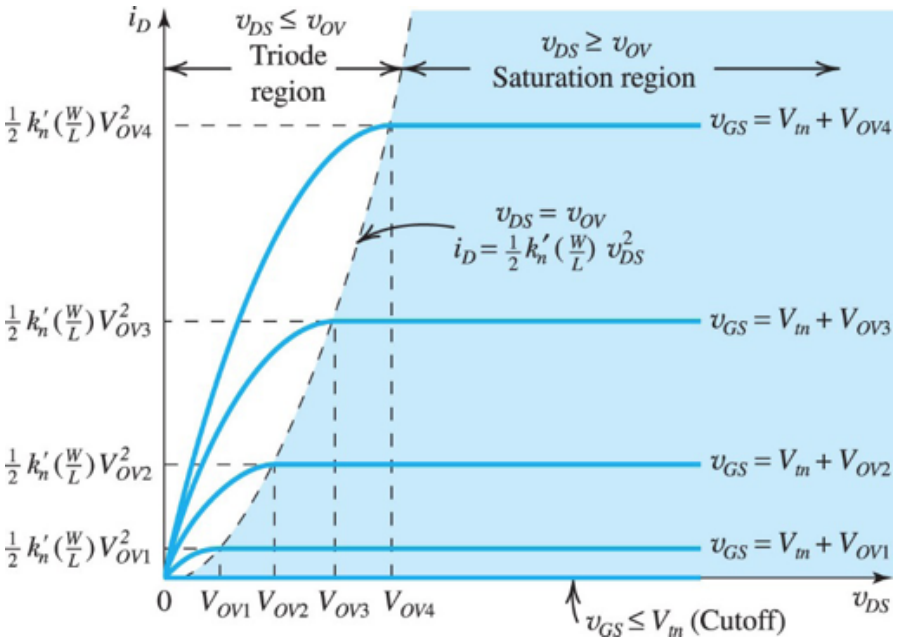
$\varepsilon_{ox} = 3.9\varepsilon_0 = 3.45 \times 10^{-11}$ F/m

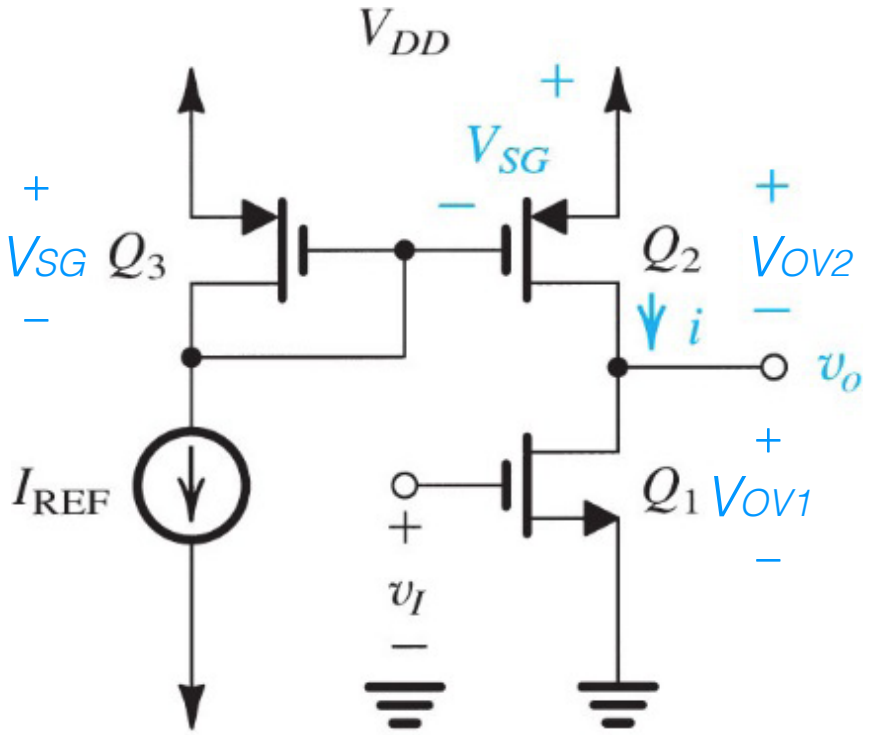
$\varepsilon_s = 11.7\varepsilon_0 = 1.04 \times 10^{-10}$ F/m

$q = 1.602 \times 10^{-19}$ C

Source: Sedra/Smith "Microelectronic Circuits", 7th Ed, Oxford University Press

MOS overdrive voltage V_{OV}





$$I_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS})$$

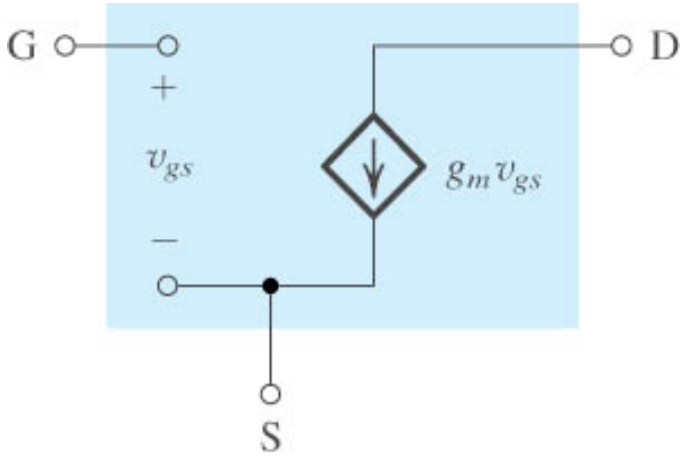
$$\lambda = 0 \longrightarrow r_o = \infty$$

$$V_{OV} = V_{GS} - V_T$$

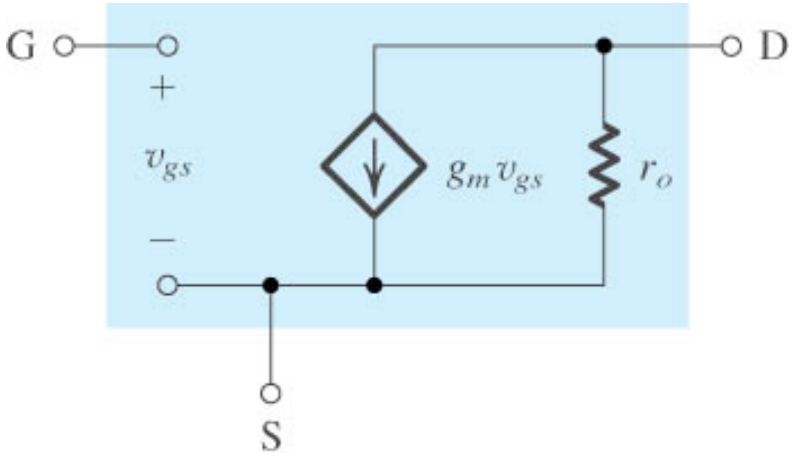
$$i_D = \frac{1}{2}k_n\left(\frac{W}{L}\right)(V_{OV})^2 \longrightarrow V_{OV} = \sqrt{\frac{2i_D}{k_n\left(\frac{W}{L}\right)}}$$

Small-signal models of MOS transistor

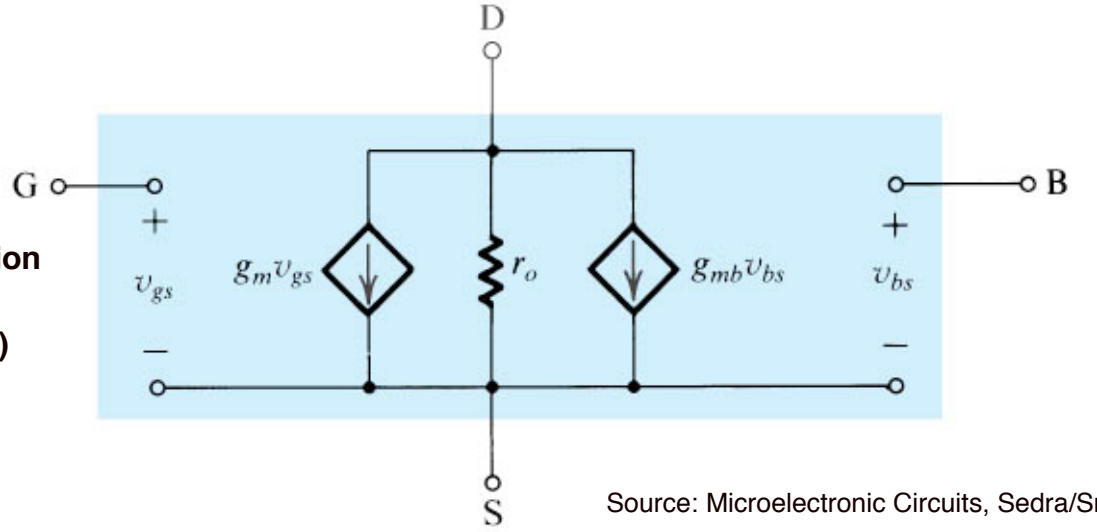
- neglecting channel-length modulation effect (output resistance $r_o = \infty$)



- including channel-length modulation effect (finite output resistance r_o)



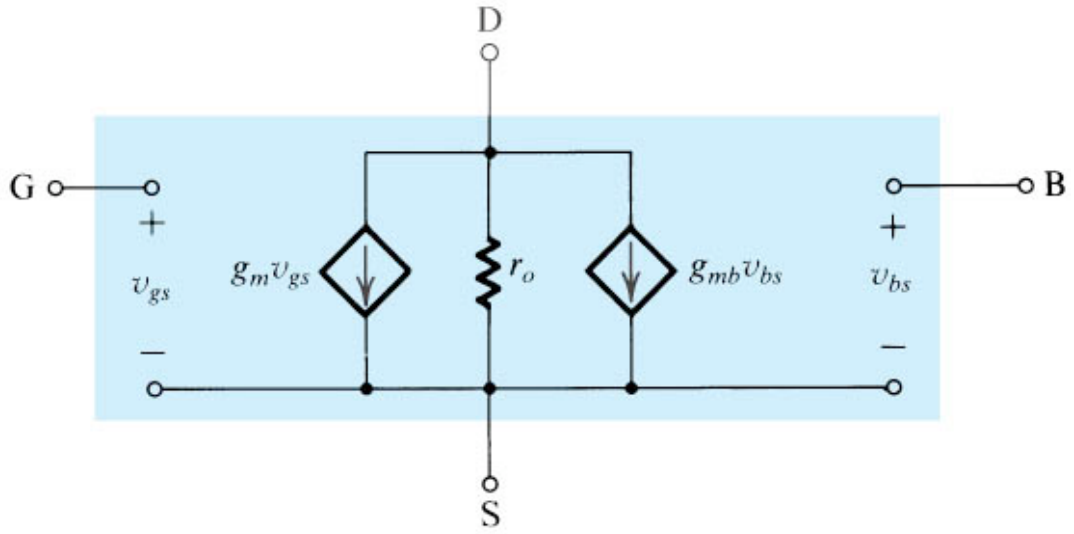
- including channel-length modulation effect and substrate (bulk) transconductance g_{mb} ($v_{bs} \neq 0$)



Source: Microelectronic Circuits, Sedra/Smith, 5th ed.

Small-signal model and parameters of MOS transistor

- **model**



- **parameters**

transconductance

$$g_m = \mu_n C_{ox} \frac{W}{L} V_{OV} = \sqrt{2\mu_n C_{ox} \frac{W}{L} I_D} = \frac{2I_D}{V_{OV}}$$

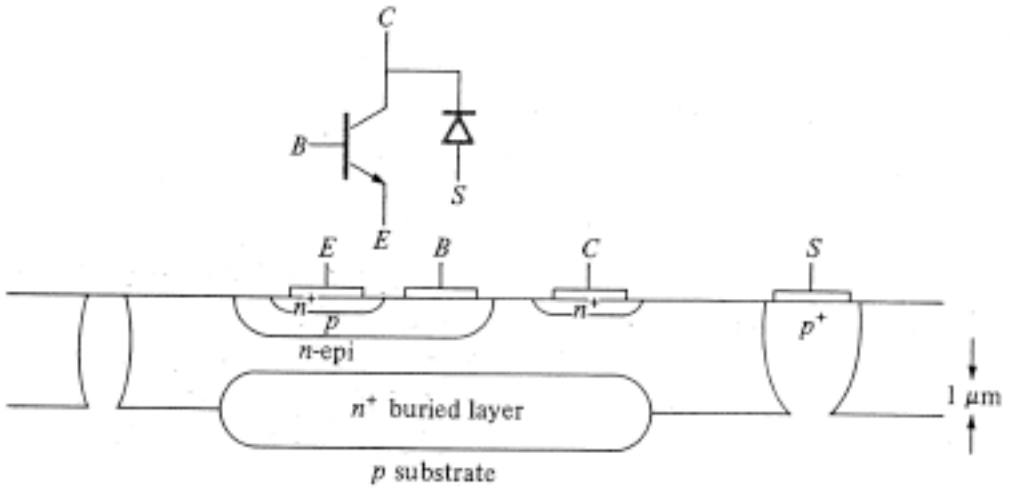
substrate (bulk) transconductance

$$g_{mb} = \chi g_m = \frac{\gamma}{2\sqrt{2\phi_f + V_{SB}}} g_m$$

output resistance

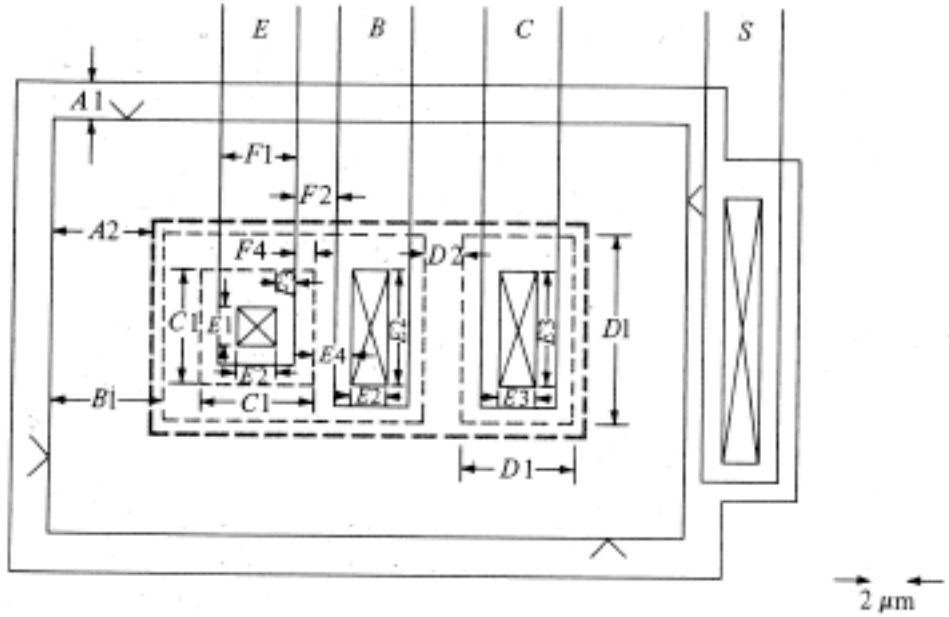
$$r_o = V_A / I_D$$

Bipolar junction transistors (BJTs)



Integrated circuit npn transistor structure

Cross-sectional view



Layout

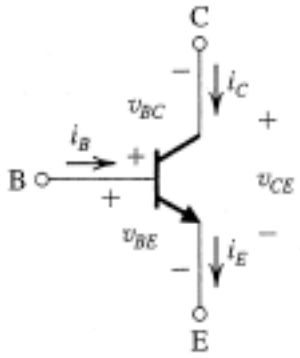
Buried-layer mask
Isolation mask
Diffusion mask
Metal mask
Contact window mask

Source: D.A.Hodges, H.G.Jackson, Analysis and Design of Digital ICs

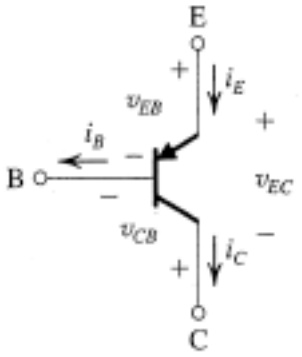
Bipolar junction transistors (BJTs)

Circuit Symbol and Directions of Current Flow

npn Transistor



pnp Transistor



$i_E = i_C + i_B$

Operation in the Active Mode (for Amplifier Application)

Conditions:

1. EBJ Forward Biased

$v_{BE} > V_{BEon}$; $V_{BEon} \equiv 0.5$ V

Typically, $v_{BE} = 0.7$ V

$v_{EB} > V_{EBon}$; $V_{EBon} \equiv 0.5$ V

Typically, $v_{EB} = 0.7$ V

2. CBJ Reversed Biased

$v_{BC} \le V_{BCon}$; $V_{BCon} \equiv 0.4$ V

$\Rightarrow v_{CE} \ge 0.3$ V

$v_{CB} \le V_{CBon}$; $V_{CBon} \cong 0.4$ V

$\Rightarrow v_{EC} \ge 0.3$ V

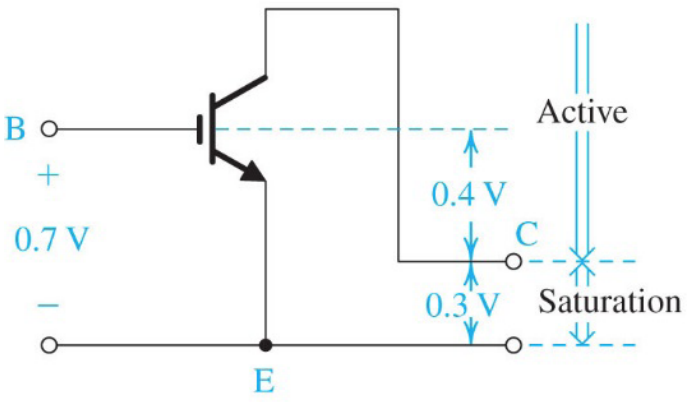
Current-Voltage Relationships

- $i_C = I_S e^{v_{BE}/V_T}$
- $i_C = I_S e^{v_{EB}/V_T}$
- $i_B = i_C/\beta \quad \Leftrightarrow \quad i_C = \beta i_B$
- $i_E = i_C/\alpha \quad \Leftrightarrow \quad i_C = \alpha i_E$
- $\beta = \dfrac{\alpha}{1-\alpha} \quad \Leftrightarrow \quad \alpha = \dfrac{\beta}{\beta+1}$

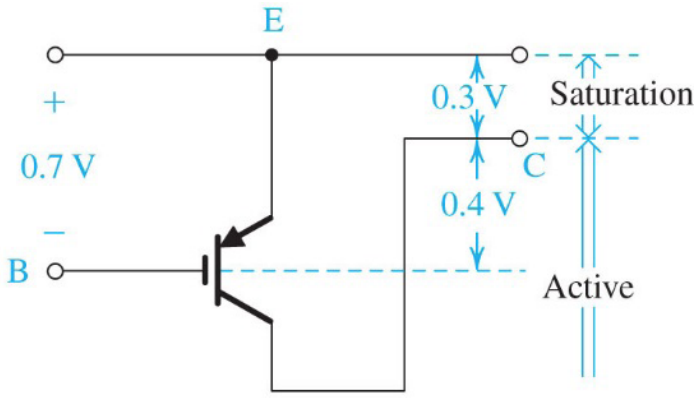
$I_S = A \cdot I_s$

A = emitter area

BJT base-emitter voltage V_{BE} [$V_{BE(ON)}$]



(a) *npn*



(b) *pnp*

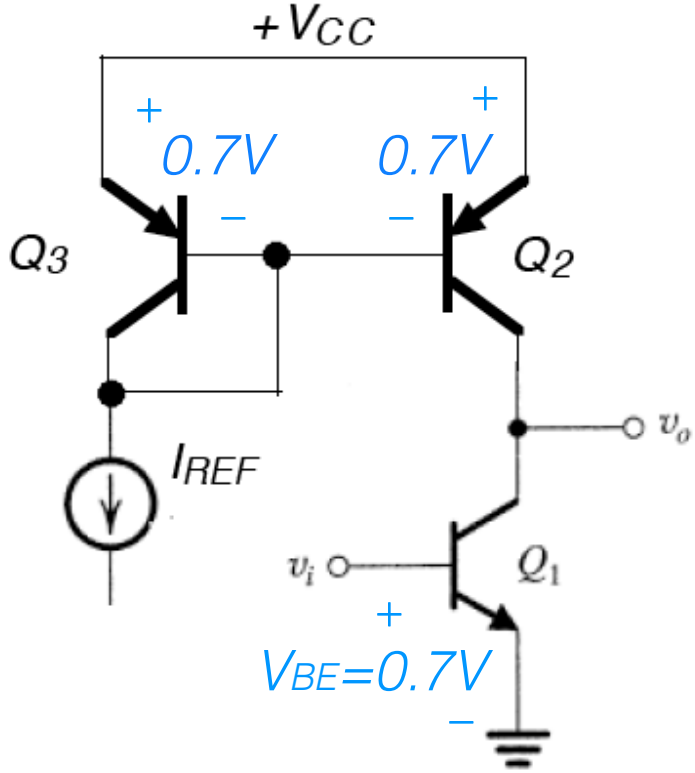
BJT biased in active region:

B-E junction forward biased → $V_{BE} = V_{BE(ON)} = 0.7V$

B-C junction reverse biased (or forward biased below 0.4V)

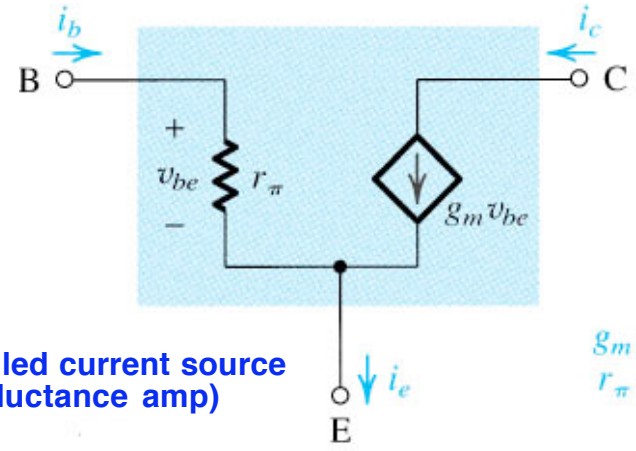
BJT biased in saturation region:

Both junction froward biased → $V_{CE} \leq 0.3V$



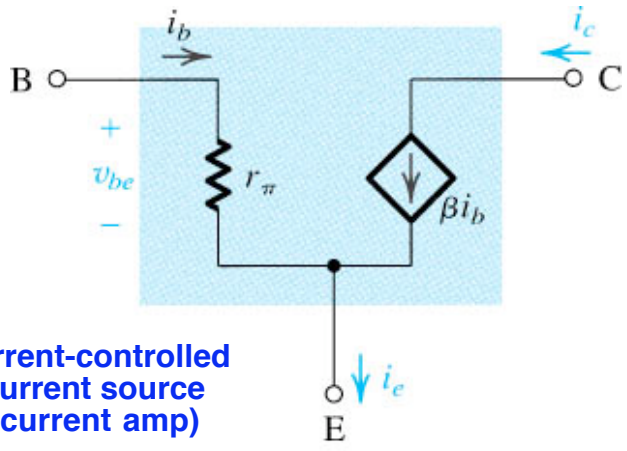
Small-signal BJT model

hybrid-π



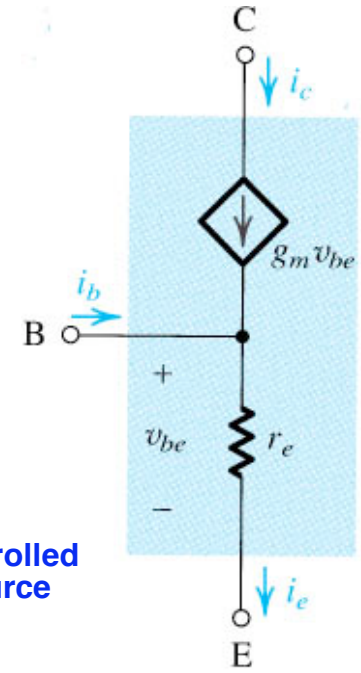
voltage-controlled current source (transconductance amp)

$$g_m = I_C/V_T$$
$$r_\pi = \beta/g_m$$



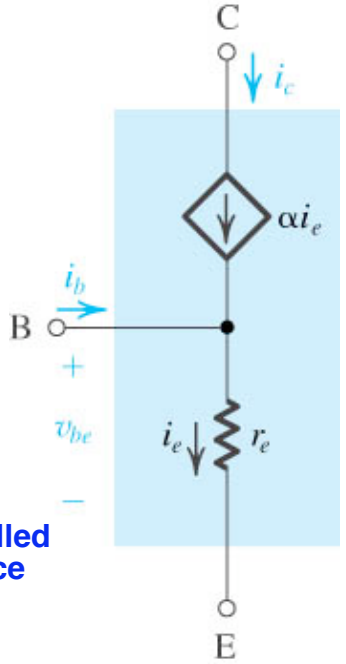
current-controlled current source (current amp)

T-model



voltage-controlled current source

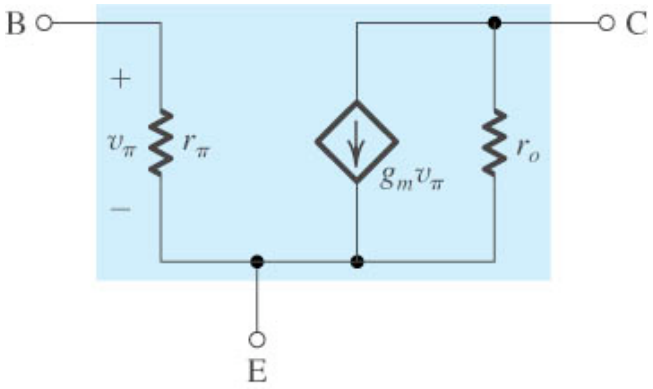
$$g_m = I_C/V_T$$
$$r_e = \frac{V_T}{I_E} = \frac{\alpha}{g_m}$$



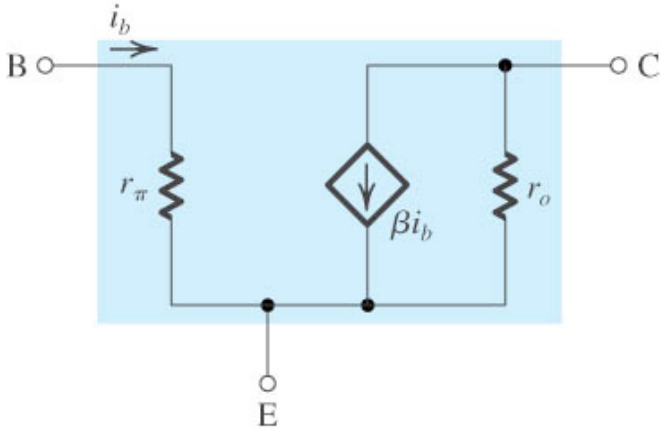
current-controlled current source

Small-signal BJT model including the output resistance

hybrid-π

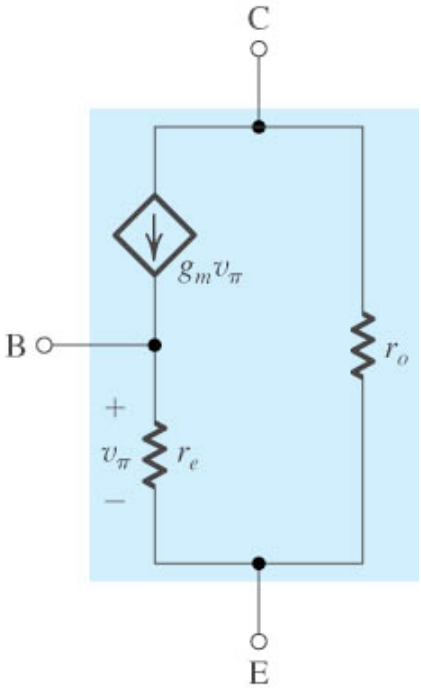


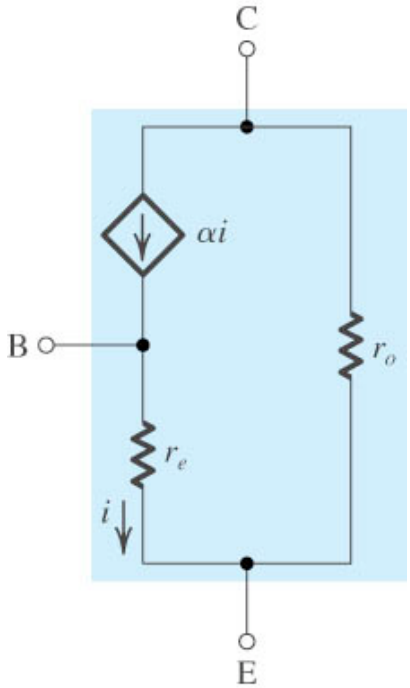
voltage-controlled current source
(transconductance amp)



current-controlled current source
(current amp)

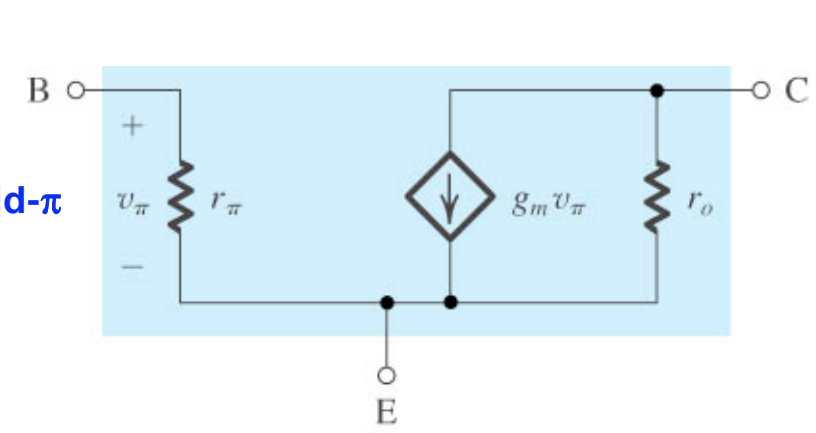
T-model

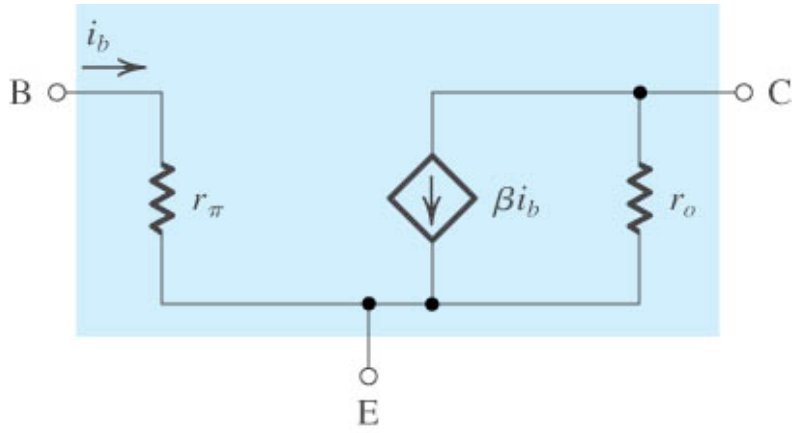




Small-signal BJT model parameters

hybrid-π





Model Parameters in Terms of DC Bias Currents

$$g_m = \frac{I_C}{V_T} \qquad r_e = \frac{V_T}{I_E} = \alpha\left(\frac{V_T}{I_C}\right) \qquad r_\pi = \frac{V_T}{I_B} = \beta\left(\frac{V_T}{I_C}\right) \qquad r_o = \frac{|V_A|}{I_C}$$

In Terms of g_m

$$r_e = \frac{\alpha}{g_m} \qquad r_\pi = \frac{\beta}{g_m}$$

In Terms of r_e

$$g_m = \frac{\alpha}{r_e} \qquad r_\pi = (\beta+1)r_e \qquad g_m + \frac{1}{r_\pi} = \frac{1}{r_e}$$

Relationships Between α and β

$$\beta = \frac{\alpha}{1-\alpha} \qquad \alpha = \frac{\beta}{\beta+1} \qquad \beta + 1 = \frac{1}{1-\alpha}$$