Zhenman Fang

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CV Contents

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Work Experience

4/2019 – present **Simon Fraser University**, *Burnaby, BC, Canada*, **Tenure-Track Assistant Professor**.
Primary Affiliation: School of Engineering Science, Computer Engineering Option
Associate Faculty Member, School of Computing Science, since 8/2019
Co-Chair, Computer Engineering Option, since 9/2021
Founder and Director, HiAccel Research Lab

2/2020 – present **Part-time Consultant**, *Burnaby, BC, Canada*.
Part-time consulting service to Canadian and US industry in topics relevant to hardware acceleration and hardware/software codesign

7/2018 – 3/2019 **Simon Fraser University**, *Burnaby, BC, Canada*, **Adjunct Professor**.
School of Engineering Science, Computer Engineering Option

9/2017 – 3/2019 **Xilinx**, *San Jose, CA, USA*, **Staff Software Engineer**.
SDx (now re-branded as AMD Vitis) System Compiler Team

7/2014 – 9/2017 **University of California, Los Angeles**, *USA*, **Postdoctoral Scholar**.
Worked in two multi-university centers: Center for Domain-Specific Computing (CDSC) and Center for Future Architectures Research (C-FAR)

4/2013 – 7/2014 **University of Minnesota, Twin Cities**, *USA*, **Research Scholar**.
Department of Computer Science and Engineering

Education and Training

7/2014 – 9/2017 **University of California, Los Angeles**, *USA*, **Postdoctoral Scholar**, *Computer Science*.
Research: Accelerator-Rich Architectures and Systems
Supervisor: Prof. Jason Cong and Prof. Glenn Reinman

4/2013 – 7/2014 **University of Minnesota, Twin Cities**, *USA*, **Visiting PhD**, *Computer Science and Engineering*.
Thesis: On Performance Optimization and Evaluation for Multicore Memory Systems
Supervisor: Prof. Pen-Chung Yew

9/2009 – 6/2014 **Fudan University, China**, **PhD**, *Computer Science*.
Thesis: On Performance Optimization and Evaluation for Multicore Memory Systems
Supervisor: Prof. Binyu Zang

9/2005 – 7/2009 **Fudan University, China and University College Dublin, Ireland**, **Joint Bachelor's Degree**.
Bachelor of Engineering, Software Engineering, Fudan University (**Outstanding Graduate**)
Bachelor of Science Honors, Computer Science, University College Dublin

Research Interests

Major theme: Customizable computing with software-defined hardware acceleration, especially on the commodity reconfigurable computing platform FPGA, including:

- **Hardware/software codesign for machine learning:** especially for accelerating early-day CNNs [J5, C9], sub-8-bit mixed-precision CNNs [J16, J10, C40, C30, C28, C23], SNNs [J8, C21], vision transformers [C36, C29, C25], and stable diffusion [C41]

- **Hardware/software codesign for big data analytics:** especially for accelerating structured queries [J18, J11, C31], vector database queries [J15, C19, C18], and common big data processing tax [C39, C38, C13, SC3]
- **Other workload characterization and acceleration:** especially for precision medicine [J2, C16, C12, C11, C7], high-performance computing [J13, C44, C37, C33], quantum chemistry [C42], and learned image processing [J17, J12, C43, C35, C34]
- **Characterization of commodity hardware platforms:** [J9, J4, J1, C20, C15, C6, SC2]
- **Next-generation computer architecture:** especially for heterogeneous and energy-efficient accelerator-rich architectures [J7, J3, C18, C15, C14, C11, C10, C5, SC4, SC2, TR1], memory systems and near data acceleration [J13, J11, C18, C11, SC4]
- **Programming, automation, and compiler support:** especially support for the above computer architectures [J19, J18, J14, J13, J6, C32, C31, C8, C4, P3, P2, TR3]
- **Reliability for hardware accelerators:** especially for learning-based hardware reliability modeling [C17, SC5], and robustness for machine learning accelerators [C27, C26, C24, C22]

Selected Awards

2024 **FPL 2024 Stamatis Vassiliadis Best Paper Award**, *34th IEEE International Conference on Field-Programmable Logic and Applications (FPL 2024), [C42] received the highest review score and best paper among all 129 FPL 2024 submissions*.

2024 **FPGA 2024 Paper with the Highest Review Score**, *32nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2024), [C33] received the highest review score among all 89 FPGA 2024 submissions, tied with two other submissions*.

2022 **FPGA 2021 Paper Highlighted in ACM TRETS Special Issue**, *29th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2021), [C20] highlighted in FPGA 2021 Special Issue in ACM Transactions on Reconfigurable Technology and Systems (TRETS)*.

2020 **Natural Sciences and Engineering Research Council of Canada (NSERC) Alliance Award**.

2019 **Canada Foundation for Innovation John R. Evans Leaders Fund (CFI JELF) Award**.

2019 **Xilinx University Program Award**.

2019 **TCAD 2019 Donald O. Pederson Best Paper Award**, *IEEE Council on Electronic Design Automation, the best paper published/accepted in the IEEE Transactions on CAD in 2017/2018*.

2018 **ISPASS 2018 Best Paper Nominee**, *2018 IEEE International Symposium on Performance Analysis of Systems and Software (ISPASS 2018), 4 papers out of 67 submissions*.

2017 **MEMSYS 2017 Best Paper Award**, *The ACM International Symposium on Memory Systems (MEMSYS 2017), 1 paper out of 42 accepted papers*.

2017 **HPCA 2017 Best Paper Nominee**, *2017 IEEE Symposium on High Performance Computer Architecture (HPCA 2017), 4 papers out of 224 submissions*.

2018 **Team Award in Xilinx Software and IP Group (10-people team in a 1000+ people group)**.

2018 **Outstanding Reviewer**, *Elsevier Journal of Parallel and Distributed Computing (JPDC)*.

2017 **Outstanding Reviewer**, *Integration, the Elsevier VLSI Journal*.

2017 **Outstanding Reviewer**, *Elsevier Microprocessors and Microsystems (MICPRO)*.

2016 **Outstanding Reviewer**, *Elsevier Journal of Parallel and Distributed Computing (JPDC)*.

2016 **Best Demo Award**, *SRC/DARPA Center for Future Architectures Research (C-FAR) 2016 Annual Review, 3rd place out of 49 demos*.

2016 **Postdoc Fellowship, UCLA Institute for Digital Research and Education (IDRE)**.

Publications

Quick Summary

75 publications: 19 journal papers, 49 conference papers (44 full papers and 5 short papers), 2 US patents and 1 China patent, 4 technique reports.

Total citations: 2,700+, h-index: 25. 1 paper with 700+ citations: [J5, TCAD 2019 Donald O. Pederson Best Paper]. **1 paper with 200+ citations:** [J12, TGRS 2023]. **5 more papers with 100+ citations:** [SC2, FCCM 2018 Short Paper], [C10, HPCA 2017 Best Paper Nominee], [C8, ACM SOCC 2016], [C7, HotCloud 2016], [C6, DAC 2016]. Based on Google Scholar [Dec 28, 2024].

Conference and journal ranking: Tier 1 conferences and journals are the top tier ones in the field, and tier 2 means very good (but not the top tier) conferences and journals. The ranking is mainly based on Conference Ranks (`http://www.conferenceranks.com/`).

Legend and author list convention: Names that are underlined in the publication list are those students, postdoc, and/or research associate whom I have supervised or co-supervised since I joined SFU. ***My name*** is highlighted in ***bold and italic***. **The author list is typically in the descending order of contribution and students are generally listed first.** An exception of this convention is for some of my work done at UCLA (before joining SFU) with my postdoc supervisor Dr. Jason Cong, where the author list is sometimes in the alphabetical order of author names; in this case, names with a following "*" denote the leading authors.

Where do I publish: After I officially joined SFU, I mainly publish in the FPGA and reconfigurable computing area, including top-tier conferences (FPGA, FCCM, FPL) and top-tier journal (TRETS). Meanwhile, I also publish in other closely relevant areas such as design automation and computer architecture, as summarized in the tables below.

Journal field, name, tier, and number of papers that I published there:

Field	Name	Full Journal Name	Tier	Number of papers that I published
FPGA and reconfigurable computing	TRETS	ACM Transactions on Reconfigurable Technology and Systems	1	full x11
Design automation	TCAD	IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems	1	full x1, best paper x1
	D&T	IEEE Design & Test	1	full x1
Computer architecture	TACO	ACM Transactions on Architecture and Code Optimization	1	full x1
Remote sensing	TGRS	IEEE Transactions on Geoscience and Remote Sensing	1	full x2
Signal processing	TIP	IEEE Transactions on Image Processing	1	full x1
Broad ECE and CS	PIEEE	Proceedings of the IEEE	1	full x1
	TETC	IEEE Transactions on Emerging Topics in Computing	1	full x1
Total journal publications (19 published)				full x19

Conference field, name, tier, and number of papers that I published there:

Field	Name	Full Conference Name	Tier	Number of papers that I published
FPGA and reconfigurable computing	FPGA	ACM International Symposium on Field-Programmable Gate Arrays	1	full x3, top papers x2
	FCCM	IEEE International Symposium on Field-Programmable Custom Computing Machines	1	full x5, short x3
	FPL	IEEE International Conference Field-Programmable Logic and Applications	1	full x7, short x1 best paper x1
	FPT	IEEE International Conference on Field-Programmable Technology	2	full x2
Design automation (sponsored by IEEE & ACM)	DAC	Design Automation Conference	1	full x2
	ICCAD	International Conference on Computer-Aided Design	1	full x3
	DATE	Design, Automation and Test in Europe Conference	1	full x2
Computer architecture	HPCA	IEEE Symposium on High Performance Computer Architecture	1	full x2, best paper nominee x1
	ISPASS	IEEE International Symposium on Performance Analysis of Systems and Software	2	full x2, best paper nominee x1
	IISWC	IEEE International Symposium on Workload Characterization	2	full x1
	LCTES	ACM Conference on Languages, Compilers, and Tools for Embedded Systems	2	full x1, short x1
	ASAP	IEEE International Conference on Application-specific Systems, Architectures and Processors	2	full x1
	MEMSYS	ACM International Symposium on Memory Systems	2	full x1, best paper x1
High performance computing and cloud computing	ICS	ACM International Conference on Supercomputing	1	full x2
	SOCC	ACM Symposium on Cloud Computing	1	full x1
	HotCloud	USENIX Workshop on Hot Topics in Cloud Computing	2	full x1
Computer vision and signal processing	ECCV	European Conference on Computer Vision	1	full x2
	ICASSP	IEEE International Conference on Acoustics, Speech, and Signal Processing	1	full x1
	DCC	IEEE Data Compression Conference	1	full x1
	PacRim	IEEE Pacific Rim Conference on Communications, Computers, and Signal Processing	N/A	full x1, top paper x1
Circuit and system design	ISQED	IEEE International Symposium on Quality Electronic Design	2	full x1
	DSD	IEEE/Euromicro Symposium on Digital Systems Design	2	full x2
Total conference publications (48 published + 1 accepted)				full x44, short x5

Journal Articles (Published: 19)

[J19] Moazin Khatti, Xingyu Tian, Ahmad Sedigh Baroughi, Akhil Raj Baranwal, Yuze Chi, Licheng Guo, Jason Cong, ***Zhenman Fang***. *PASTA: Programming and Automation Support for Scalable Task-Parallel HLS Programs on Modern Multi-Die FPGAs*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2024, Tier 1**), Volume 17, Issue 3, Sept 2024, Article No.: 42, Pages 1 - 31. Journal extension of [C32].

[J18] Alec Lu, Jahanvi Narendra Agrawal, ***Zhenman Fang***. *SQL2FPGA: Automatic Acceleration of SQL Query Processing on Modern CPU-FPGA Platforms*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2024, Tier 1**), Volume 17, Issue 3, Sept 2024, Article No.: 39, Pages 1 - 28. Journal extension of [C31].

[J17] Haisheng Fu, Feng Liang, Jie Liang, Yongqiang Wang, ***Zhenman Fang***, Guohe Zhang, Jingning Han. *Fast and High-Performance Learned Image Compression With Improved Checkerboard Context Model, Deformable Residual Module, and Knowledge Distillation*. IEEE Transactions on Image Processing (**TIP 2024, Tier 1**), vol. 33, pp. 4702-4715, Aug 2024.

[J16] Geng Yang, Jie Lei, ***Zhenman Fang***, Yunsong Li, Jiaqing Zhang, Weiying Xie. *HyBNN: Quantifying and Optimizing Hardware Efficiency of Binary Neural Networks*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2024, Tier 1**), Volume 17, Issue 2, Article No.: 25, pp 1–24. FPT 2023 Journal Track.

[J15] Kenny Liu*, Alec Lu*, Kartik Samtani, ***Zhenman Fang***, and Licheng Guo. *CHIP-KNNv2: A Configurable and High-Performance K-Nearest Neighbors Accelerator on HBM-based FPGAs*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2023, Tier 1**), Volume 16, Issue 4, Dec 2023, Article No.: 62, pp 1–26. Journal extension of [C19].
Note: Kenny and Alec co-lead this paper.

[J14] Licheng Guo, Yuze Chi, Jason Lau, Linghao Song, Xingyu Tian, Moazin Khatti, Weikang Qiao, Jie Wang, Ecenur Ustun, ***Zhenman Fang***, Zhiru Zhang, and Jason Cong. *TAPA: A Scalable Task-Parallel Dataflow Programming Framework for Modern FPGAs with Co-Optimization of HLS and Physical Design*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2023, Tier 1**), Volume 16, Issue 4, Dec 2023, Article No.: 63, pp 1–31.

[J13] Xingyu Tian, Zhifan Ye, Alec Lu, Licheng Guo, Yuze Chi, and ***Zhenman Fang***. *SASA: A Scalable and Automatic Stencil Acceleration Framework for Optimized Hybrid Spatial and Temporal Parallelism on HBM-based FPGAs*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2023, Tier 1**), Volume 16, Issue 2, Apr 2023, Article No.: 28, pp 1–33.

[J12] Jiaqing Zhang, Jie Lei, Weiying Xie, ***Zhenman Fang***, Yunsong Li, Qian Du. *SuperYOLO: Super Resolution Assisted Object Detection in Multimodal Remote Sensing Imagery*. IEEE Transactions on Geoscience and Remote Sensing (**TGRS 2023, Tier 1**), vol. 61, pp. 1-15, Mar 2023, Art no. 5605415. **This paper has been cited more than 200 times.**

[J11] Weikang Qiao, Licheng Guo, ***Zhenman Fang***, Mau-Chung Frank Chang, and Jason Cong. *TopSort: A High-Performance Two-Phase Sorting Accelerator Optimized on HBM-based FPGAs*. IEEE Transactions on Emerging Topics in Computing (**TETC 2023 Invited Paper, Tier 1**), vol. 11, no. 2, pp. 404-419, 1 April-June 2023.

[J10] Geng Yang, Jie Lei, Weiying Xie, ***Zhenman Fang***, Yunsong Li, Jiaxuan Wang, Xin Zhang. *Algorithm/Hardware Co-Design for Real-Time On-Satellite CNN based Ship Detection in SAR Imagery*. IEEE Transactions on Geoscience and Remote Sensing (**TGRS 2022, Tier 1**), Volume: 60, pp. 1-18, Mar 2022.

[J9] Alec Lu, ***Zhenman Fang***, and Lesley Shannon. *Demystifying the Soft and Hardened Memory Systems of Modern FPGAs for Software Programmers through Microbenchmarking*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2022 Special Issue on FPGA 2021 Highlights, Tier 1**), Volume 15, Issue 4, December 2022, Article No.: 43, pp 1–33. Journal extension of [C20].

[J8] Sathish Panchapakesan, ***Zhenman Fang***, and Jian Li. *SyncNN: Evaluating and Accelerating Spiking Neural Networks on FPGAs*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2022, Tier 1**), Volume 15, Issue 4, Article No.: 48, pp 1–27, December 2022. Journal extension of [C21].

[J7] Eric Matthews, Alec Lu, ***Zhenman Fang***, and Lesley Shannon. *Quick-Div: Rethinking Integer Divider Design for FPGA-based Soft-Processors*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2022, Tier 1**), Volume 15, Issue 3, Article No.: 32, pp 1–27, September 2022. Journal extension of [C14].

[J6] Yi-Hsiang Lai, Ecenur Ustun, Shaojie Xiang, ***Zhenman Fang***, Hongbo Rong, Zhiru Zhang. *Programming and Synthesis for Software-Defined FPGA Acceleration: Status and Future Prospects*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2021 Invited Paper, Tier 1**), Volume 14, Issue 4, Article No.: 17, pp 1–39, December 2021.

[J5] Chen Zhang, Guangyu Sun, ***Zhenman Fang***, Peipei Zhou, Peichen Pan, Jason Cong. *Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks*. IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (**TCAD 2019 Best Paper, Tier 1**), Volume 38, Issue 11, Pages 2072-2085, Nov. 2019. Journal extension of [C9]. **This paper has been cited more than 740 times.**

———Before Officially Joining SFU (4)———

[J4] Young-kyu Choi, Jason Cong, ***Zhenman Fang***, Yuchen Hao, Glenn Reinman, Peng Wei*. *In-depth Analysis on Microarchitectures of Modern Heterogeneous CPU-FPGA Platforms*. ACM Transactions on Reconfigurable Technology and Systems (**TRETS 2019, Tier 1**), Volume 12, Issue 1, February 2019, Article No.: 4, pp 1–20. Journal extension of [C6].

[J3] Jason Cong*, ***Zhenman Fang***, Muhuan Huang, Peng Wei, Di Wu, and Cody Hao Yu. *Customizable Computing — From Single-Chip to Datacenters*. Proceedings of the IEEE (**PIEEE 2019 Invited Paper, Tier 1**), Volume 107, Issue 1, Pages 185 - 203, Jan. 2019.

[J2] Jason Cong, ***Zhenman Fang***, Muhuang Huang*, Libo Wang, Di Wu. *CPU-FPGA Co-Optimization for Big Data Applications*. IEEE Design & Test (**D&T 2018 Invited Paper, Tier 1**), vol. 35, no. 1, pp. 16-22.

[J1] ***Zhenman Fang***, Sanyam Mehta, Pen-Chung Yew, Antonia Zhai, James Greensky, Gautham Beeraka, and Binyu Zang. *Measuring Microarchitectural Details of Multi- and Many-core Memory Systems Through Microbenchmarking*. ACM Transactions on Architecture and Code Optimization (**TACO 2015, Tier 1**), 11, 4, Article 55 (January 2015), 26 pages.

Refereed Full Conference Papers (Accepted: 1)

[C44] Xingyu Tian, Geng Yang, ***Zhenman Fang***. *FLUD: A Scalable and Configurable Systolic Array Design for LU Decomposition on FPGAs*. Accepted by the 2024 IEEE International Conference on Field-Programmable Technology (**FPT 2024, Tier 2**), Sydney, Australia, December 2024. Acceptance Rate: 27.5%, 19 out of 69.

Refereed Full Conference Papers (Published: 43)

[C43] Haisheng Fu, Jie Liang, ***Zhenman Fang***, Jingning Han, Feng Liang, Guohe Zhang. *WeConvene: Learned Image Compression with Wavelet-Domain Convolution and Entropy Model*. The 2024 European Conference on Computer Vision (**ECCV 2024, Tier 1**), Milano, Italy, Sept-Oct 2024. Lecture Notes in Computer Science, vol 15108, pp. 37–53.
Acceptance Rate: 27.9%, 2395 out of 8585.

[C42] Philip Stachura, Guanyu Li, Xin Wu, Christian Plessl, ***Zhenman Fang***. *SERI: High-Throughput Streaming Acceleration of Electron Repulsion Integral Computation in Quantum Chemistry using HBM-based FPGAs*. The 34th IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2024 Stamatis Vassiliadis Best Paper Award, Tier 1**), Turin, Italy, September 2024, pp. 60-68.
Acceptance Rate: 22.5%, 29 out of 129. Same for [C41] to [C38]

[C41] Geng Yang, Yanyue Xie, Zhong Jia Xue, Sung-En Chang, Yanyu Li, Peiyan Dong, Jie Lei, Weiying Xie, Yanzhi Wang, Xue Lin, ***Zhenman Fang***. *SDA: Low-Bit Stable Diffusion Acceleration on Edge FPGAs*. The 34th IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2024, Tier 1**), Turin, Italy, September 2024, pp. 264-273.

[C40] Geng Yang, Jie Lei, ***Zhenman Fang***, Jiaqing Zhang, Junrong Zhang, Weiying Xie and Yunsong Li. *SA4: A Comprehensive Analysis and Optimization of Systolic Array Architecture for 4-bit Convolutions*. The 34th IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2024, Tier 1**), Turin, Italy, September 2024, pp. 204-212.

[C39] Kenny Liu, Alec Lu, ***Zhenman Fang***. *BitBlender: Scalable Bloom Filter Acceleration on FPGAs with Dynamic Scheduling*. The 34th IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2024, Tier 1**), Turin, Italy, September 2024, pp. 325-331.

[C38] Abdul Wadood, Alec Lu, Ken Zhang, ***Zhenman Fang***. *FORC: A High-Throughput Streaming FPGA Accelerator for Optimized Row Columnar File Decoders in Big Data Engines*. The 34th IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2024, Tier 1**), Turin, Italy, September 2024, pp. 318-324.

[C37] Junzhe Liang, Manoj Bheemasandra Rajashekar, Xingyu Tian, ***Zhenman Fang***. *HiTC: High-Performance Triangle Counting on HBM-Equipped FPGAs using HLS*. The 2024 IEEE Pacific Rim Conference on Communications, Computers and Signal Processing (**PacRim 2024**), Victoria, BC, Aug 2024, pp. 1-6. **This paper received the highest review score among all submissions in the Computers track of PacRim 2024.**

[C36] Zhengang Li, Alec Lu, Yanyue Xie, Zhenglun Kong, Mengshu Sun, Hao Tang, Zhong Jia Xue, Peiyan Dong, Caiwen Ding, Yanzhi Wang, Xue Lin, ***Zhenman Fang***. *QUASAR-ViT: Hardware-Oriented Quantization-Aware Architecture Search for Vision Transformers*. The 38th ACM International Conference on Supercomputing (**ICS 2024, Tier 1**), Kyoto, Japan, Jun 2024, pp. 324–337.

[C35] Haisheng Fu, Feng Liang, Jie Liang, ***Zhenman Fang***, Guohe Zhang, Jingning Han. *Efficient Learned Image Compression with Selective Kernel Residual Module and Channel-wise Causal Context Model*. The 2024 IEEE International Conference on Acoustics, Speech, and Signal Processing (**ICASSP 2024, Tier 1**), Seoul, Korea, April 2024, pp. 4040-4044.

[C34] Haisheng Fu, Feng Liang, Jie Liang, ***Zhenman Fang***, Guohe Zhang, Jingning Han. *Learned Image Compression with Dual-Branch Encoder and Conditional Information Coding*. The 2024 IEEE Data Compression Conference (**DCC 2024, Tier 1**), Snowbird, Utah, March 2024, pp. 173-182.

[C33] Manoj Bheemasandra Rajashekar, Xingyu Tian, ***Zhenman Fang***. *HiSpMV: Hybrid Row Distribution and Vector Buffering for Imbalanced SpMV Acceleration on FPGAs*. The 32nd ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2024, Tier 1**), Monterey, CA, Mar 2024, pp. 154-164. **This paper received the highest review score among all FPGA 2024 submissions, tied with two other papers.**
Acceptance Rate: 23.6%, 21 out of 89.

[C32] Moazin Khatti, Xingyu Tian, Yuze Chi, Licheng Guo, Jason Cong, ***Zhenman Fang***. *PASTA: Programming and Automation Support for Scalable Task-Parallel HLS Programs on Modern Multi-Die FPGAs*. The 31st IEEE International Symposium On Field-Programmable Custom Computing Machines (**FCCM 2023, Tier 1**), Marina Del Rey, CA, May 2023, pp. 12-22.
Acceptance Rate: 21.4%, 15 out of 70.

[C31] Alec Lu, ***Zhenman Fang***. *SQL2FPGA: Automatic Acceleration of SQL Query Processing on Modern CPU-FPGA Platforms*. The 31st IEEE International Symposium On Field-Programmable Custom Computing Machines (**FCCM 2023, Tier 1**), Marina Del Rey, CA, May 2023, 184-194.
Acceptance Rate: 21.4%, 15 out of 70.

[C30] Sung-En Chang*, Geng Yuan*, Alec Lu*, Mengshu Sun, Yanyu Li, Xiaolong Ma, Zhengang Li, YanyueXie, Minghai Qin, Xue Lin, ***Zhenman Fang*** and Yanzhi Wang. *ESRU: Extremely Low-Bit and Hardware-Efficient Stochastic Rounding Unit Design for Low-Bit DNN Training*. IEEE/ACM Design, Automation and Test in Europe Conference (**DATE 2023, Tier 1**), Antwerp, Belgium, Apr 2023, pp. 1-6.
Acceptance Rate: 25%. Note: Sung-En, Geng, and Alec co-lead this paper.

[C29] Peiyan Dong, Mengshu Sun, Alec Lu, Yanyue Xie, Kenneth Liu, Zhenglun Kong, Xin Meng, Zhengang Li, Xue Lin, ***Zhenman Fang***, and Yanzhi Wang. *HeatViT: Hardware-Efficient Adaptive Token Pruning for Vision Transformers*. The 29th IEEE International Symposium on High-Performance Computer Architecture **(HPCA 2023, Tier 1**), Montreal, QC, Canada, Feb-Mar 2023, pp. 442-455.
Acceptance Rate: 25%, 91 out of 360.

[C28] Geng Yuan, Sung-En Chang, Qing Jin, Alec Lu, Yanyu Li, Yushu Wu, Zhenglun Kong, Yanyue Xie, Peiyan Dong, Minghai Qin, Xiaolong Ma, Xulong Tang, ***Zhenman Fang***, and Yanzhi Wang. *You Already Have It: A Generator-Free Low-Precision DNN Training Framework using Stochastic Rounding*. The European Conference on Computer Vision (**ECCV 2022, Tier 1**), Tel Aviv, Israel, Oct 2022. Lecture Notes in Computer Science, vol 13672, pp. 34–51.
Acceptance Rate: 28%, 1,645 out of 5,804.

[C27] Behnam Ghavami, Mani Sadati, Mohammad Shahidzadeh, ***Zhenman Fang***, Lesley Shannon. *Blind Data Adversarial Bit-flip Attack against Deep Neural Networks*. The 25th IEEE/Euromicro Conference on Digital Systems Design (**DSD 2022, Tier 2**), Gran Canaria, Spain, Aug-Sept 2022, pp. 899-904.

[C26] Behnam Ghavami, Mahdi Sajedi, Mohsen Raji, ***Zhenman Fang***, Lesley Shannon. *A Majority-based Approximate Adder for FPGAs*. The 25th IEEE/Euromicro Conference on Digital Systems Design (**DSD 2022, Tier 2**), Gran Canaria, Spain, Aug-Sept 2022, pp. 53-59.

[C25] Zhengang Li, Mengshu Sun, Alec Lu, Haoyu Ma, Geng Yuan, Yanyue Xie, Hao Tang, Yanyu Li, Miriam Leeser, Zhangyang Wang, Xue Lin, ***Zhenman Fang***. *Auto-ViT-Acc: FPGA-Aware Automatic Acceleration Framework for Vision Transformer with Mixed-Scheme Quantization*. The 32nd IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2022, Tier 1**), Belfast, UK, Aug-Sept 2022, pp. 109-116.
Acceptance Rate: 25.6%, 33 out of 129.

[C24] Behnam Ghavami, Sayed Hamid Reza Mousavi, ***Zhenman Fang***, Lesley Shannon. *Stealthy Attack on Algorithmic-Protected DNNs via Smart Bit Flipping*. The 23nd IEEE International Symposium on Quality Electronic Design (**ISQED 2022, Tier 2**), Virtual Conference, Apr 2022, pp. 358-364.

[C23] Mengshu Sun*, Zhengang Li*, Alec Lu*, Yanyu Li, Sung-En Chang, Xiaolong Ma, Xue Lin, ***Zhenman Fang***. *FILM-QNN: Efficient FPGA Acceleration of Deep Neural Networks with Intra-Layer, Mixed-Precision Quantization*. The 30th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2022, Tier 1**), Virtual Conference, Feb/Mar 2022, pp. 134–145.
Acceptance Rate: 20.8%, 15 out of 72. Note: Mengshu, Zhengang, and Alec co-lead this paper.

[C22] Behnam Ghavami, Mani Sadati, ***Zhenman Fang***, Lesley Shannon. *FitAct: Error Resilient Deep Neural Networks via Fine-Grained Post-Trainable Activation Functions*. IEEE/ACM Design, Automation and Test in Europe Conference (**DATE 2022, Tier 1**), Virtual Conference, Mar 2022, pp. 1239-1244.
Acceptance Rate: 25%.

[C21] Sathish Panchapakesan, ***Zhenman Fang***, and Jian Li. *SyncNN: Evaluating and Accelerating Spiking Neural Networks on FPGAs*. The 31st IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2021, Tier 1**), Virtual Conference, Sept 2021, pp. 286-293.
Acceptance Rate: 22.2%, 32 out of 144.

[C20] Alec Lu, ***Zhenman Fang***, Weihua Liu, and Lesley Shannon. *Demystifying the Memory System of Modern Datacenter FPGAs for Software Programmers through Microbenchmarking*. The 29th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (**FPGA 2021, Tier 1**), Virtual Conference, Mar 2021, pp. 105–115. **This paper is one of the top papers highlighted in the FPGA 2021 Special Issue in ACM TRETS.**
Acceptance Rate: 19.8%, 22 out of 111.

[C19] Alec Lu, ***Zhenman Fang***, Nazanin Farahpour, and Lesley Shannon. *CHIP-KNN: A Configurable and High-Performance K-Nearest Neighbors Accelerator on Cloud FPGAs*. The 2020 IEEE International Conference on Field-Programmable Technology (**FPT 2020, Tier 2**), Virtual Conference, Dec 2020, pp. 139-147.
Acceptance Rate: 24.7%, 21 out of 85.

[C18] Nazanin Farahpour, Yuchen Hao, ***Zhenman Fang***, and Glenn Reinman. *Reconfigurable Accelerator Compute Hierarchy: A Case Study Using Content-Based Image Retrieval*. The 2020 IEEE International Symposium on Workload Characterization (**IISWC 2020, Tier 2**), Virtual Conference, Oct 2020, pp. 276-287.
Acceptance Rate: 37.1%, 26 out of 70.

[C17] Seyed Milad Ebrahimipour, Behnam Ghavami, Hamdi Mousavi, Mohsen Raji, ***Zhenman Fang*** and Lesley Shannon. *Aadam: A Fast, Accurate, and Versatile Aging-Aware Cell Library Delay Model using Feed-Forward Neural Network*. The 2020 IEEE/ACM International Conference On Computer Aided Design (**ICCAD 2020, Tier 1**), Virtual Conference, Nov 2020, pp. 1-9.
Acceptance Rate: 27.0%, 127 out of 470.

[C16] Michael Lo, ***Zhenman Fang***, Jie Wang, Peipei Zhou, Mau-Chung Frank Chang and Jason Cong. *Algorithm-Hardware Co-design for BQSR Acceleration in Genome Analysis ToolKit*. The 28th IEEE International Symposium On Field-Programmable Custom Computing Machines (**FCCM 2020, Tier 1**), Fayetteville, AR, USA, May 2020, pp. 157-166.
Acceptance Rate: 20.7%, 19 out of 92.

[C15] ***Zhenman Fang***, Farnoosh Javadi, Jason Cong, Glenn Reinman. *Understanding Performance Gains of Accelerator-Rich Architectures*. The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors (**ASAP 2019 invited paper, Tier 2**), New York NY, Jul 2019, pp. 239-246.

[C14] Eric Matthews, Alec Lu, ***Zhenman Fang***, and Lesley Shannon. *Rethinking Integer Divider Design for FPGA-based Soft-Processors*. The 27th IEEE International Symposium on Field-Programmable Custom Computing Machines (**FCCM 2019, Tier 1**), San Diego CA, Apr 2019, pp. 289-291.
Acceptance Rate: 25.8%, 31 out of 120.

———Before Officially Joining SFU (13)———

[C13] Weikang Qiao, Jieqiong Du, ***Zhenman Fang***, Jason Cong, and Mau-Chung Frank Chang. *High-Throughput Lossless Compression on Tightly-Coupled CPU-FPGA Platforms*. The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines (**FCCM 2018, Tier 1**), Boulder CO, May 2018, pp. 37-44.
Acceptance Rate: 20.8%, 22 out of 106.

[C12] Peipei Zhou, Zhenyuan Ruan, ***Zhenman Fang***, Jason Cong, Megan Shand, and David Roazen. *Doppio: I/O-Aware Performance Analysis, Modeling and Optimization for In-Memory Computing Framework*. The 2018 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS 2018 Best Paper Nominee, Tier 2**), Belfast, Northern Ireland, UK, Apr 2018, pp. 22-32.
Acceptance Rate: 31.3%, 21 out of 67. Best paper nominee rate: 6.0%, 4 out of 67.

[C11] Jason Cong, ***Zhenman Fang****, Michael Gill, Farnoosh Javadi*, Glenn Reinman. *AIM: Accelerating Computational Genomics through Scalable and Noninvasive Accelerator-Interposed Memory*. The ACM International Symposium on Memory Systems (**MEMSYS 2017 Best Paper Award, Tier 2**), Alexandria, VA, Oct 2017, pp. 3-14.
Acceptance Rate: N/A. Best paper award rate: $< 2.4\%$, 1 out of 42 accepted papers.
Note: Dr. Fang and Farnoosh Javadi (whom Dr. Fang mentored back when he was a postdoc at UCLA) made equal contribution to co-lead this paper.

[C10] Jason Cong, ***Zhenman Fang****, Yuchen Hao*, Glenn Reinman. *Supporting Address Translation for Accelerator-Centric Architectures*. The 23rd IEEE Symposium on High Performance Computer Architecture (**HPCA 2017 Best Paper Nominee, Tier 1**), Austin TX, Feb 2017, pp. 37-48. **This paper has been cited more than 120 times.**
Acceptance Rate: 22.3%, 50 out of 224. Best paper nominee rate: 1.8%, 4 out of 224.
Note: Dr. Fang and Yuchen Hao (whom Dr. Fang mentored back when he was a postdoc at UCLA) made equal contribution to co-lead this paper.

[C9] Chen Zhang, ***Zhenman Fang***, Peipei Zhou, Peichen Pan, Jason Cong. *Caffeine: Towards Uniformed Representation and Acceleration for Deep Convolutional Neural Networks*. The 2016 IEEE/ACM International Conference on Computer-Aided Design (**ICCAD 2016, Tier 1**), Austin TX, Nov 2016, pp. 1-8.
Acceptance Rate: 23.7%, 97 out of 409.

[C8] Muhuan Huang, Di Wu, Cody Hao Yu, ***Zhenman Fang***, Matteo Interlandi, Tyson Condie, Jason Cong. *Programming and Runtime Support to Blaze FPGA Accelerator Deployment at Datacenter Scale*. The ACM Symposium on Cloud Computing (**ACM SOCC 2016, Tier 1**), Santa Clara, CA, Oct 2016, pp. 456-469. **This paper has been cited more than 110 times.**
Acceptance Rate: 25.2%, 38 out of 151.

[C7] Yu-Ting Chen, Jason Cong, ***Zhenman Fang***, Jie Lei, Peng Wei*. *When Apache Spark Meets FPGAs: A Case Study for Next-Generation DNA Sequencing Acceleration*. The 8th USENIX Workshop on Hot Topics in Cloud Computing (**HotCloud 2016, Tier 2**), Denver CO, Jun 2016, pp. 64-70. **This paper has been cited more than 100 times.**
Acceptance Rate: 30.9%, 21 out of 68.

[C6] Young-kyu Choi, Jason Cong, ***Zhenman Fang***, Yuchen Hao, Glenn Reinman, Peng Wei*. *A Quantitative Analysis on Microarchitectures of Modern CPU-FPGA Platforms*. The 53rd ACM/IEEE Design Automation Conference (**DAC 2016, Tier 1**), Austin TX, Jun 2016, pp. 1-6.
Acceptance Rate: 22.6%, 152 out of 674.
This paper has been cited more than 190 times.

[C5] Jason Cong, ***Zhenman Fang****, Michael Gill, Glenn Reinman. *PARADE: A Cycle-Accurate Full-System Simulation Platform for Accelerator-Rich Architectural Design and Exploration*. 2015 IEEE/ACM International Conference on Computer-Aided Design (**ICCAD 2015, Tier 1**), Austin TX, Nov 2015, pp. 380-387.
Acceptance Rate: 24.6%, 94 out of 382.

[C4] Sanyam Mehta, ***Zhenman Fang***, Antonia Zhai, Pen-Chung Yew. *Multi-Stage Coordinated Prefetching for Present-day Processors*. Proceedings of the 28th ACM International Conference on Supercomputing (**ICS 2014, Tier 1**), Munich, Germany, Jun 2014, pp. 73-82.
Acceptance Rate: 21.3%, 34 out of 160.

[C3] ***Zhenman Fang***, Qinghao Min, Keyong Zhou, Yi Lu, Yibin Hu, Weihua Zhang, Haibo Chen, Jian Li, Binyu Zang. *Transformer: A Functional-Driven Cycle-Accurate Multicore Simulator*. The 49th ACM/IEEE Design Automation Conference (**DAC 2012, Tier 1**), San Francisco CA, Jun 2012, pp. 106-114.
Acceptance Rate: 22.7%, 168 out of 741.

[C2] ***Zhenman Fang***, Jiaxin Li, Weihua Zhang, Yi Li, Haibo Chen, Binyu Zang. *Improving Dynamic Prediction Accuracy Through Multi-Level Phase Analysis*. Proceedings of the 2012 ACM SIGPLAN/SIGBED Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES 2012, Tier 2**), Beijing, China, Jun 2012, pp. 89-98.
Acceptance Rate: 22.7%, 15 out of 66.

[C1] ***Zhenman Fang***, Donglei Yang, Weihua Zhang, Haibo Chen, Binyu Zang. *A Comprehensive Analysis and Parallelization of an Image Retrieval Algorithm*. The 2011 IEEE International Symposium on Performance Analysis of Systems and Software (**ISPASS 2011, Tier 2**), Austin TX, Apr 2011, pp. 154-164.
Acceptance Rate: 37.5%, 24 out of 64.

Refereed Short Conference Papers (Published: 5)

[SC5] Behnam Ghavami, Milad Ebrahimi, ***Zhenman Fang***, Lesley Shannon. *MAPLE: A Machine Learning based Aging-Aware FPGA Architecture Exploration Framework*. The 31st IEEE International Conference on Field-Programmable Logic and Applications (**FPL 2021 short paper, Tier 1**), Virtual Conference, Sept 2021, pp. 369-373.
Acceptance Rate: 37.5%, 54 out of 144.

[SC4] Nazanin Farahpour, ***Zhenman Fang***, and Glenn Reinman. *FPGA-based Near Data Processing Platform Selection Using Fast Performance Modeling*. The 21st ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (**LCTES 2020 short WiP paper, Tier 2**), Virtual Conference, June 2020, pp. 151-155.

[SC3] Mau-Chung Frank Chang, Jason Cong, ***Zhenman Fang***, and Weikang Qiao*. *An FPGA-based BWT Accelerator for Bzip2 Data Compression*. The 27th IEEE International Symposium on Field-Programmable Custom Computing Machines (**FCCM 2019 short paper, Tier 1**), San Diego CA, Apr 2019, pp. 96-99.
Acceptance Rate: 17.9%, 7 out of 39.

———Before Officially Joining SFU (2)———

[SC2] Jason Cong, ***Zhenman Fang****, Michael Lo, Hanrui Wang, Jingxian Xu and Shaochong Zhang. *Understanding Performance Differences of FPGAs and GPUs*. The 26th IEEE International Symposium on Field-Programmable Custom Computing Machines (**FCCM 2018 short paper, Tier 1**), Boulder CO, May 2018, pp. 172-175. **This paper has been cited more than 170 times.**
Acceptance Rate: 14.6%, 7 out of 48.

[SC1] Peipei Zhou, HyunSeok Park, ***Zhenman Fang***, Jason Cong, Andre DeHon. *Energy Efficiency of Fully Pipelining: A Case Study for Matrix Multiplication*. The 24th IEEE International Symposium on Field-Programmable Custom Computing Machines (**FCCM 2016 short paper, Tier 1**), Washington DC, May 2016, pp. 172-175.
Acceptance Rate: 24.1%, 32 out of 133.

Patents (Granted: 3)

[P3] ***Zhenman Fang***, James L Hwang, Alfred Huang, Michael Gill, Tom Shui. *Heterogeneous instantiation of high-level language callable library for hardware core*. **US patent**: 10762265 B1. Filed date: Nov 13, 2018. Publication date: Sept 1, 2020.
Note: This work was done back when Dr. Fang was at Xilinx.

[P2] ***Zhenman Fang***, James L Hwang, Samuel A Skalicky, Tom Shui, Michael Gill, Welson Sun, Alfred Huang, Jorge E Carrillo, Chen Pan. *Automatic creation of high-level language callable library for a hardware core*. **US patent**: 10755013 B1. Filed date: Nov 13, 2018. Publication date: Aug 25, 2020.
Note: This work was done back when Dr. Fang was at Xilinx.

——Before Officially Joining SFU (1)——

[P1] Weihua Zhang, ***Zhenman Fang***, Donglei Yang, Binyu Zang. *Image/video feature extraction parallel algorithm based on multi-core system structure*. **China patent**: CN102495725 A. Filed date: Nov 15, 2011. Publication date: Jun 13, 2012.

Technical Reports (Published: 4)

[TR4] Kiarash Saremi, Hossein Pedram, Behnam Ghavami, Mohsen Raji, ***Zhenman Fang***, and Lesley Shannon. *SeaPlace: Process Variation Aware Placement for Reliable Combinational Circuits against SETs and METs*. arXiv:2112.04136 [cs.AR], 2021. 14 pages

———Before Officially Joining SFU (3)———

[TR3] Jason Cong, ***Zhenman Fang***, Yuchen Hao, Peng Wei*, Cody Hao Yu, Chen Zhang, Peipei Zhou. *Best-Effort FPGA Programming: A Few Steps Can Go a Long Way*. arXiv:1807.01340 [cs.AR] 2018. 13 pages.

[TR2] Jason Cong, ***Zhenman Fang***, Hassan Kianinejad*, Peng Wei. *Revisiting FPGA Acceleration of Molecular Dynamics Simulation with Dynamic Data Flow Behavior in High-Level Synthesis*. arXiv:1611.04474 [physics.comp-ph] 2016. 8 pages.

[TR1] Yu-Ting Chen*, Jason Cong, ***Zhenman Fang***, Bingjun Xiao, Peipei Zhou. *ARAPrototyper: Enabling Rapid Prototyping and Evaluation for the Accelerator-Rich Architecture*. arXiv:1610.09761 [cs.AR] 2016. 14 pages.

Open Source Software

Summary: Led and contributed to the release of 16 open source software projects. Detailed project description and link can be found here: http://www.sfu.ca/~zhenman/software.html

[SW16] [@SFU] SERI: Streaming Acceleration for Electron Repulsion Integral Computation on FPGA

[SW15] [@SFU] BitBlender: Scalable Bloom Filter Accelerator on FPGA

[SW14] [@SFU] FORC: FPGA Accelerator for Apache ORC File Decoder
Our FORC work is considered for adoption by Huawei Canada.

[SW13] [@SFU] HiSpMV: A High-Performance SpMV Accelerator on FPGA for Imbalanced Matrices

[SW12] [@SFU] PASTA: Scalable Task-Parallel HLS Programming Framework on FPGA

[SW11] [@SFU] SQL2FPGA: Spark SQL to FPGA Compiler
Our SQL2FPGA work has received great interests from multiple companies such as AMD/Xilinx, Huawei Canada, and Microsoft.

[SW10] [@SFU] SASA: Scalable and Automatic Stencil Acceleration on FPGA

[SW9] [@SFU] SyncNN: Novel Synchronous Spiking Neural Network Acceleration on FPGA

[SW8] [@SFU] Rodinia-HLS: FPGA Version of Rodinia Benchmarks in HLS C/C++
Our Rodinia-HLS benchmarks have been adopted in the AMD/Xilinx Vitis quality of results (QoR) regression tests.

[SW7] [@SFU] Microbenchmarks to Characterize Modern FPGA Memory Systems

[SW6] [@SFU] CHIP-KNN: A Configurable and High-Performance KNN Accelerator on FPGA

[SW5] [@UCLA] PARADE: Full-System Accelerator-Rich Architecture Simulator

[SW4] [@UCLA] Blaze: Deploying Accelerators at Datacenter Scale

[SW3] [@UCLA] Microbenchmarks to Characterize Modern CPU-FPGA Platforms

[SW2] [@UCLA] High-Throughput Deflate Compression Accelerator on FPGA

[SW1] [@UMN] Microbenchmarks to Characterize Multi-/Many-core Memory Systems

Invited Talks

Summary: More than 30 invited talks by universities and companies in USA, Canada, Switzerland, Italy, China mainland, Hong Kong and Taiwan.

[TK12] *Software-Programmable Accelerator-Centric Systems (4)*

- ByteDance, San Jose, CA, USA (Mar 2024)
- City University of Hong Kong, Virtual (Nov 2023)
- AMD/Xilinx, San Jose, CA, USA (Jul 2023)
- Futurewei, Santa Clara, CA, USA (Jul 2023)

[TK11] *Hardware/Software Codesign for Big Data Acceleration on FPGAs (1)*

- Huawei Big Data Meetup II Workshop 2023, Virtual (Nov 2023)

[TK10] *PASTA: Programming and Automation Support for Scalable Task-Parallel HLS Programs on Modern Multi-Die FPGAs (1)*

- SFU-Huawei Joint Lab Workshop 2023, Virtual (Oct 2023)

[TK9] *Hardware/Software Codesign to Accelerate Vision Transformers on FPGAs (1)*

- Invited talk at the 8th Energy Efficient Training and Inference of Transformer Based Models (EMC2) Workshop, Co-located with the 37th AAAI Conference on Artificial Intelligence (AAAI 2023), Virtual (Feb 2023)

[TK8] *Intelligent Computing Memory Systems for Data-Intensive Applications (1)*
- SFU-Huawei Joint Lab Workshop 2022, Virtual (Nov 2022)

[TK7] *Accelerating Big Data Analytics with Hardware/Software Co-design (2)*
- Huawei 13th Strategy & Technology Workshop (STW 2022), Virtual (Sept 2022)
- Huawei 2012 Labs Global Software Technology Summit - Canadian Research Institute, Virtual (Mar 2022)

[TK6] *Accelerating Next-Generation Sequencing on FPGA-Enabled Cluster (1)*
- British Columbia Genome Sciences Center, Vancouver, BC, Canada (Apr 2020)

[TK5] *Customizable Computing with Specialized Hardware Acceleration (1)*
- Huawei Big Data Workshop, Toronto, ON, Canada (Oct 2019)

[TK4] *Understanding Performance Gains of Accelerator-Rich Architectures (1)*
- Invited talk at the 30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019), New York, NY, USA (Jul 2019)

[TK3] *Towards Accelerator-Rich Architectures and Systems (13)*
- Politecnico di Milano, Milan, Italy (Oct 2019)
- Huawei Research, Burnaby, BC, Canada (Apr 2019)
- Alibaba Group Holding, Sunnyvale, CA, USA (Dec 2018)
- University of California, Merced, CA, USA (Nov 2017)
- Simon Fraser University, Burnaby, BC, Canada (Oct 2017)
- University of Southern California, Los Angeles, CA, USA (Sept 2017)
- Xilinx, San Jose, CA, USA (May 2017)
- Peking University, Beijing, China (May 2017)
- EPFL, Lausanne, Switzerland (Mar 2017)
- University of California, Santa Cruz, CA, USA (Feb 2017)
- University of Pittsburgh, Pittsburgh, PA, USA (Feb 2017)
- Drexel University, Philadelphia, PA, USA (Feb 2017)
- University of California, Los Angeles, CA, USA (Feb 2017)

[TK2] *Accelerating Next-Generation DNA Sequencing (1)*
- UCLA Institute for Digital Research and Education (IDRE), CA, USA (Apr 2017)

[TK1] *Initial Experiences with Deploying FPGA Accelerators in Datacenters (5)*
- National Chiao Tung University, Taiwan (Oct 2016)
- Peking University, Beijing, China (Oct 2016)
- Tsinghua University, Beijing, China (Oct 2016)
- Huawei Technologies Co., Ltd., Beijing, China (Oct 2016)
- Institute of Computing Technology, Chinese Academy of Sciences, Beijing, China (Oct 2016)

Teaching Experience

Summary: Created one new cross-listed course on ENSC 453/894 (5 offerings), completely redesigned core course ENSC 254 (2 offerings), and kept enhancing core course ENSC 251 (7 offerings). Organized a couple of full-day conference tutorials.

ENSC 453/894: Programming for Heterogeneous Computing Systems (4 credits)

- New course I created, undergraduate/graduate cross-listed, open to CS as well
- Focus on multicore CPU programming with OpenMP, FPGA programming with high-level synthesis C/C++, and GPU programming with CUDA, which is first-of-its-kind
- ENSC 453/894 (4 credits) course offering summary:

Semester	Enrollment	#TAs	Instructor Support	Course Difficulty	Response Rate
Fall 2024	57 Undergrad + 7 Grad	2	4.2	0.5	91%
Fall 2023	33 Undergrad + 4 Grad	1	4.2	0.3	86%
Fall 2022	16 Undergrad + 16 Grad	1	4.4	0.5	81%

Semester	Enrollment	#TAs	Overall Quality	Course Difficulty	Response Rate
Summer 2021	9 Undergrad + 4 Grad	1	4.11	1.44	100%
Summer 2020	15 Undergrad + 9 Grad	1	4.08	2.17	88.9%

- **Note:** Before Fall 2022, the course overall quality score is taken from the question of "Overall, the quality of my learning experience in this course was... Scale used: 1=Very Poor, 2=Poor, 3=Fair, 4=Good, 5=Very Good". The course difficulty score is taken from the question of "How easy was the course? Scale used: 1=Very Hard, 2=Hard, 3=Medium, 4=Easy, 5=Very Easy". Both are taken from SFU student surveys.
  Starting from Fall 2022, SFU no longer provides the above scores in the student evaluation. Instead, the instructor support score is taken from the question of "I think Zhenman Fang ... tried to support student learning (i.e., used a variety of learning activities, invested in my success, invited and responded to student feedback). It is scored as: Almost never = 1, Rarely = 2, Sometimes/Somewhat = 3, Often = 4, Almost always = 5." The course difficulty score is taken from the question of "How challenging you find a course is related to how much effort you have to put in to be successful. It is scored as: Not challenging = -1, The right level of challenge for me = 0, Too challenging = 1."

ENSC 254: Introduction to Computer Organization (4 credits)

- 2nd year undergraduate core course (i.e., all students have to take this course), focus on fundamentals of computer organization
- Completely redesigned the course (was ARM based, over-focused on assembly programming) to focus on the latest RISC-V based processor design and cache memory hierarchy design
- ENSC 254 (4 credits) course offering summary:

Semester	Enrollment	#TAs	Instructor Support	Course Difficulty	Response Rate
Summer 2024	176	6	4.0	0.3	88%
Summer 2023	144	4	4.3	0.1	78%

ENSC 251: Software Design and Analysis for Engineers (4 credits)

- 2nd year undergraduate core course, focus on object-oriented programming with C++
- This course is offered twice ever year, all students have to take this course

- ENSC 251 (4 credits) course offering summary:

Semester	Enrollment	#TAs	Instructor Support	Course Difficulty	Response Rate
Fall 2022	98	3	4.4	0.1	89%

Semester	Enrollment	#TAs	Overall Quality	Course Difficulty	Response Rate
Summer 2022	59	3	3.91	2.87	78%
Fall 2021	84	4	3.52*	2.57	76.2%
Summer 2021	51	2	4.06	2.56	70.6%
Fall 2020	88	2	3.81	2.52	92%
Fall 2019	111	3	4.06	2.47	88.3%
Summer 2019	44	2	3.89	2.50	88.6%

- **Note:** Fall 2021 was the first semester resuming the in-person teaching after more than a year of online teaching due to COVID-19. It was the first ever in-person semester for this cohort of students enrolled in ENSC 251, who started at SFU in Fall 2020 in the midst of COVID-19. Plus, there were limited lab space due to ASB (Applied Science Building) renovation: I had to accommodate 40-student lab sessions with a 10-person room using hybrid lab sessions, which students were not very happy with. These factors led to a fluctuation in the overall quality score in the student evaluation for Fall 2021.

Full-Day Conference Tutorial: Rapid Exploration of Accelerator-rich Architectures: Automation from Concept to Prototyping

- In the 49th Annual IEEE/ACM International Symposium on Microarchitecture (**MICRO 2016**), Taipei, Taiwan, Oct 2016. Organized with David Brooks, Jason Cong, Yakun Sophia Shao, and Sam Xi.
- In the 42nd ACM/IEEE International Symposium on Computer Architecture (**ISCA 2015**), Portland OR, Jun 2015. Organized with David Brooks, Yu-Ting Chen, Jason Cong, Brandon Reagen, Glenn Reinman, Yakun Sophia Shao, Gu-Yeon Wei and Sam Xi.

Student Supervision

Quick Summary

Student awards for whom I have supervised at SFU:

Student Awards	**Number**
FPL 2024 Stamatis Vassiliadis Best Paper Award	1
FPGA 2024 Paper with the Highest Review Score	1
PacRim 2024 Paper with the Highest Review Score in Computers Track	1
FPGA 2021 Paper Highlighted in ACM TRETS Special Issue	1
MASc Thesis Defended with Distinction (Passed as Is)	2
NSERC Canada Graduate Scholarships - Master's (CGS-M)	1
British Columbia Graduate Scholarship	2
Mitacs Globalink Graduate Fellowship	1
SFU Graduate Dean's Entrance Scholarship	1
SFU Graduate Travel and Research Award	5
Mitacs Globalink Research Internship (Undergraduate)	6
NSERC Undergraduate Student Research Award	2
SFU VPR Undergraduate Student Research Award	1
Total	25

Students whom I have supervised at SFU, plus 2 students co-supervised from UCLA, and 1 student co-supervised from Xidian University, China:

Students	Postdoc	PhD	MASc	MEng	BASc	Total	Minority
Completed	0	3 (1+2)	4 (3+1)	2	13	22 (19+3)	22
Current	1	4	7	0	0	12	11

Students whom I have served in the supervisory/exam committee:

Students Committee	PhD@SFU	MASc@SFU	PhD outside SFU	Total
Completed	9	13	2	24
Current	1	0	0	1

Current Students and Postdoc (12)

Postdoc at SFU (1)

- Haisheng Fu, 11/2023 – present
  Co-supervised with Prof. Jie Liang, Prof. Liang is the primary supervisor
  PhD from Xi'an Jiaotong University, China, 2023, Visiting PhD at SFU, 11/2021 - 10/2023
  Publication (4): [J17, TIP 2024][C43, ECCV 2024][C35, ICASSP 2024][C34, DCC 2024]

PhD students at SFU (4)

- Xingyu Tian, 9/2019 – present, transferred from MASc to PhD since 5/2021
  Thesis topic: Software-defined hardware acceleration for high-performance computing
  Publication (7): [C44, FPT 2024][C37, PacRim 2024][C33, FPGA 2024][C32, FCCM 2023][J19, TRETS 2024][J14, TRETS 2023][J13, TRETS 2023]
  Award: PacRim 2024 Paper [C37] with the Highest Review Score in Computers Track
  Award: FPGA 2024 Paper [C33] with the Highest Review Score
  Award: SFU Graduate Travel and Research Award, Fall 2024
  Intern: Huawei Big Data Team, Canada, 12/2024 - present
- Philip Stachura, 9/2023 - present, transferred from MASc to PhD since 9/2024
  Publication: [C42, FPL 2024]
  Award: FPL 2024 Stamatis Vassiliadis Best Paper Award, Paper [C42]
  Award: NSERC Canada Graduate Scholarships - Master's (CGS-M), 2024-2025
  Award: British Columbia Graduate Scholarship, 2024
  Award: SFU Graduate Travel and Research Award, Fall 2024
- Ahmad Sedigh Baroughi, 9/2023 – present
  Publication: [J19, TRETS 2024]
- Qilin Hu (female), Visiting PhD from Hunan University, China, 11/2023 – present

MASc students (thesis-based) at SFU (7)

- Kenny Liu, 5/2021 - present
  BASc/MASc combined program, officially started MASc portion from 5/2022
  Publication: [C39, FPL 2024][C29, HPCA 2023][J15, TRETS 2023]
  Award: NSERC USRA (Undergraduate Student Research Awards), Summer 2021
  Award: SFU Graduate Travel and Research Award, Fall 2024
- Manoj BR, 9/2022 - present
  Publication: [C37, PacRim 2024][C33, FPGA 2024]
  Award: PacRim 2024 Paper [C37] with the Highest Review Score in Computers Track
  Award: FPGA 2024 Paper [C33] with the Highest Review Score
  Award: Mitacs Globalink Graduate Fellowship, 2022
  Intern: d-Matrix, Canada, 5/2024 - present

- Abdul Wadood, 9/2022 - present
  Publication: [C38, FPL 2024]
  Award: SFU Graduate Travel and Research Award, Fall 2024
  Intern: Huawei Big Data Team, Canada, 12/2022 - present
- William (Zhong Jia) Xue, 9/2022 - present
  BASc/MASc combined program, officially started MASc portion from 1/2023
  Publication: [C41, FPL 2024][C36, ICS 2024]
  Award: British Columbia Graduate Scholarship, 2023
  Award: NSERC USRA (Undergraduate Student Research Awards), Fall 2022
- Dilshan Sampath, 9/2022 - present
- Akhil Raj Barnawal, 9/2023 - present
  Publication: [J19, TRETS 2024]
- Haikai Zhao, 5/2024 - present

Alumni (22)

PhD students at SFU (1)

- Alec Lu, 9/2018 – 2/2024, transferred from MASc to PhD since 1/2020
  Co-supervised with Prof. Lesley Shannon, I am the primary supervisor
  Thesis: Towards Software-Defined FPGA Acceleration for Big Data Analytics
  Publication (17): [C39, FPL 2024][C38, FPL 2024][C36, ICS 2024][C31, FCCM 2023][C30, DATE 2023][C29, HPCA 2023][C28, ECCV 2022][C25, FPL 2022][C23, FPGA 2022] [C20, FPGA 2021][C19, FPT 2020][C14, FCCM 2019][J18, TRETS 2024][J15, TRETS 2023][J13, TRETS 2023][J9, TRETS 2022] [J7, TRETS 2022]
  Award: FPGA 2021 Paper [C20] Highlighted in ACM TRETS Special Issue
  Award: SFU Graduate Travel and Research Award, Summer 2023
  Intern: Meta, Redmond, WA, USA, 6/2022 - 10/2022
  Intern: Huawei Big Data Team, Canada, 12/2022 - 4/2023
  First position: ASIC Engineer, Meta (Facebook), Sunnyvale, CA, USA

MASc students (thesis-based) at SFU (3)

- Junzhe Liang (female), 9/2021 - 4/2024
  Thesis: HiTC: High-Performance Triangle Counting on HBM-Equipped FPGAs using HLS
  Publication: [C37, PacRim 2024]
  Award: PacRim 2024 Paper [C37] with the Highest Review Score in Computers Track
  First position: PhD Student, Xi'an Jiaotong University, China
- Moazin Khatti, 9/2021 - 11/2023
  Thesis: Programming and Automation Support for Scalable Task-Parallel HLS Programs on Modern Multi-Die FPGAs. **Thesis defended with distinction** (passed as is)
  Publication: [C32, FCCM 2023][J19, TRETS 2024][J14, TRETS 2023]
  Intern: d-Matrix, Canada, 5/2023 - 11/2023
  First position: Backend Compiler Engineer, d-Matrix, Toronto, ON, Canada
- Sathish Panchapakesan, 9/2019 – 12/2021
  Thesis: Evaluation and Acceleration of Spiking Neural Networks using FPGAs.
  Thesis defended with distinction (passed as is)
  Publication: [C21, FPL 2021][J8, TRETS 2022]
  Intern: Research Engineer Intern, Huawei Canada, 7/2021 - 1/2022
  First position: ML System Software Engineer, Qualcomm, Toronto, ON, Canada

MEng students (course-based) at SFU (2)

- Kartik Samtani, 1/2021 – 12/2023
  Publication: [J15, TRETS 2023]
  Award: SFU Graduate Dean's Entrance Scholarship (GDES), 2021-2022
  Intern: Huawei Big Data Team, Canada, 12/2022 - 4/2023
  First position: Staff Engineer, ASIC Digital Design, Synopsys, Missisauga, ON, Canada
- Weihua Liu, 9/2019 – 12/2023
  Publication: [C20, FPGA 2021]
  Award: FPGA 2021 Paper [C20] Highlighted in ACM TRETS Special Issue
  First position: Software Testing Engineer, Fortinet, Burnaby, BC, Canada

PhD students at Xidian University, China (1)

- Geng Yang (female), 7/2023 – 12/2024
  Note: Geng Yang were supposed to visit my group at SFU for one year starting from Jul 2023, but were delayed due to visa issues. I have remotely co-supervised her.
  Publication (4): [C44, FPT 2024][C41, FPL 2024][C40, FPL 2024][J16, TRETS 2024]
  First position: Assistant Researcher, Ant Research, Beijing, China

PhD student at UCLA (1)

- Nazanin Farahpour (female), 10/2018 – 3/2020
  Co-supervised with Prof. Glenn Reinman at UCLA, Prof. Reinman is the primary supervisor
  Thesis: Modeling and Optimization of Accelerator-Rich Architectures for Near Data Processing
  Publication: [C19, FPT 2020][C18, IISWC 2020][SC4, LCTES 2020 short WiP paper]
  First position: Senior Software Engineer, Pinterest, Bay Area, CA, USA

MASc student (thesis-based) at UCLA (1)

- Michael Lo, 10/2019 – 3/2020
  Co-supervised with Prof. Jason Cong and Prof. Mau-Chung Frank Chang at UCLA, Prof. Chang is the primary supervisor
  Project: Algorithm-Hardware Co-design for BQSR Acceleration in Genome Analysis ToolKit
  Publication: [C16, FCCM 2020]
  First position: PhD student at UCLA

Undergraduate Research Interns (Coop) at SFU (13)

- Guanyu Li, 7/2023 - 8/2024, **Publication:** [C42, FPL 2024]
  SFU VPR (Vice President of Research) USRA (Undergraduate Student Research Awards)
  Award: FPL 2024 Stamatis Vassiliadis Best Paper Award, Paper [C42]
  First position: MEng student at University of Toronto, Canada
- Aamod B K, 5/2024 - 8/2024
  Mitacs Globalink Research Internship, International Institute of Information Technology, Bangalore, India
- Xinyu Luo, 7/2023 - 10/2023
  Mitacs Globalink Research Internship, Southeast University, China
  First position: PhD student, City University of Hong Kong
- Jahanvi Narendra Agrawal (female), 7/2023 - 10/2023, **publication:** [J18, TRETS 2024]
  Mitacs Globalink Research Internship, International Institute of Information Technology, Bangalore, India
  First position: Engineer, Qualcomm, Bengaluru, Karnataka, India

- William Xue, 9/2022 - 12/2022
  NSERC USRA (Undergraduate Student Research Awards), SFU
  First position: Continue accelerated MASc in my group
- Yibin Wang, 6/2022 - 9/2022
  Mitacs Globalink Research Internship, Xidian University, China
  First position: MASc student at UCLA, USA
- Chin ho Wan, SFU ENSC Honorarium Coop, 9/2021 - 12/2021
  First position: Firmware Verification Specialist, Fortinet, Burnaby, BC, Canada
- Zhifan Ye, 7/2021 - 12/2021, **publication:** [J13, TRETS 2023]
  Mitacs Globalink Research Internship, University of Science and Technology of China
  First position: PhD student at Georgia Institute of Technology, USA
- Yuxing Zhao (female), 7/2021 - 10/2021
  Mitacs Globalink Research Internship, Southwest Jiaotong University, China
  First position: MASc student at Tongji University, China
- Kenny Liu, 5/2021 - 8/2021
  NSERC USRA (Undergraduate Student Research Awards), SFU
  First position: Continue accelerated MASc in my group
- Richard Song, SFU ENSC Honorarium Coop, 5/2021 – 8/2021
  First position: MEng student at University of Toronto, Canada
- Francis Chui, SFU ENSC Honorarium Coop, 9/2020 – 12/2020
- Ziniu Chen, SFU ENSC Honorarium Coop, 5/2020 – 7/2020
  First position: MASc student at Hong Kong University of Science and Technology

Graduate Supervisory/Exam Committee Member (25)

PhD student committee member at SFU (10)

- Committee Member, Soroush Oraki, Prof. Jie Liang's student, 8/2022 - present
- Supervisor, Binglin Li, Prof. Jie Liang's student, 8/2019 - 12/2022, defended 12/2022
- Supervisor, Eric Matthews, Prof. Lesley Shannon's student, 11/2018 - 8/2021, defended 8/2021, **publication:** [J7, TRETS 2022[[C14, FCCM 2019]
- Supervisor, Naveen Vedula (CS), Prof. Arrvindh Shriraman's student, 1/2020 - 8/2021, defended 8/2021
- Internal Examiner, Maryamsadat Rasoulidanesh, Prof. Shahram Payandeh's student, defended 8/2021
- Internal Examiner, Amirali Sharifian (CS), Prof. Arrvindh Shriraman's student, defended 7/2020
- Chair, Nastaran Hajinazar (CS), Prof. Arrvindh Shriraman's student, defended 6/2021
- Chair, Mohammad Akbari, Prof. Jie Liang's student, defended 7/2020
- Chair, Saad Mahboob, Prof. Rodney Vaughan's student, defended 12/2019
- Chair, Careesa Liu, Prof. Ryan D'Arcy's student, defended 11/2019

MASc student (thesis-based) committee member at SFU (13)

- Committee Member, Cyrus Chan, Prof. Jie Liang's student, 8/2020 - 12/2023, defended 12/2023
- Committee Member, Ehsan Mahoor, Prof. Jie Liang's student, 9/2019 - 4/2023, defended 4/2023
- Supervisor, Yuhui Gao, Prof. Lesley Shannon's student, 9/2019 - 12/2022, defended 12/2022

- Supervisor, Graham Holland, Prof. Lesley Shannon's student, 4/2019 - 12/2019, defended 12/2019
- Examiner, Fateme Shokouhinia (CS), Prof. Alaa Alameldeen's student, defended 11/2024
- Examiner, Mahmoud Abumandour (CS), Prof. Alaa Alameldeen's student, defended 8/2024
- Examiner, Yonas Kelemework (CS), Prof. Alaa Alameldeen's student, defended 8/2023
- Examiner, Parker Tian (CS), Prof. Alaa Alameldeen's student, defended 8/2023
- Examiner, Milad Hakimi (CS), Prof. Arrvindh Shriraman's student, defended 6/2022
- Examiner, Parmida Vahdatniya (CS), Prof. Arrvindh Shriraman's student, defended 4/2022
- Examiner, Ali Sedaghati (CS), Prof. Arrvindh Shriraman's student, defended 3/2022
- Internal Examiner, Srishti Yadav, Prof. Shahram Payandeh's student, defended 2/2021
- Chair, Ana Gonzalez Rios, Prof. Ljiljana Trajkovic's student, defended 8/2022

PhD student committee member outside SFU (2)

- Committee Member, Sung-En Chang, Prof. Yanzhi Wang's student, Northeastern University, US, 1/2021 - 11/2024, defended 11/2024, **publication (4):** [C41, FPL 2024][C30, DATE 2023][C28, ECCV 2022][C23, FPGA 2022]
- Committee Member, Zhengang Li, Prof. Yanzhi Wang's student, Northeastern University, US, 1/2021 - 6/2024, defended 6/2024, **publication (5):** [C36, ICS 2024][C30, DATE 2023][C29, HPCA 2023][C25, FPL 2022][C23, FPGA 2022]

Professional Services

Summary: Very active services at SFU (e.g., Computer Option Co-Chair since 2021), conference organizing/program committee (e.g., Program Chair of IEEE RAW 2024 and RAW 2025, Program Co-Chair of IEEE PacRim 2024, General Chair of IEEE ASAP 2025, Organizing Chair of ROAD4NN 2020-2023), journal editing/review (e.g., Guest Editor of ACM TRETS 2024, ACM TODAES 2021 and Springer JSPS 2019), and grant review.

Number of committee services (excluding regular journal reviewers) that I participated:

Number of committee services per year	**2019**	**2020**	**2021**	**2022**	**2023**	**2024**
University services at SFU		6	5	4	7	7
Conference organizing committee	1	3	2	3	3	5
Conference technical program committee	3	5	7	7	6	6
Conference external review committee			2	1	2	
Journal guest editor	1		1			1
Grant reviewer		1	2	3	4	1
Total	**5**	**15**	**19**	**18**	**22**	**20**

University Services at SFU

High School Outreach

- Host for Science Coops in My Lab: Jasmine Guliam (Female) from McNair Secondary, Mar 2024; and Jared Fenster from Terry Fox Secondary, Apr 2024

University-Level Services

- Open Science Principles Drafting Committee Member, SFU, 2023-2024
- White Paper Reviewer, Westcoast Women in Engineering, Science and Technology (WWEST), SFU, 2020

Faculty of Applied Science (FAS) Services

- Invited Faculty Member, SFU Burnaby FAS Conversion Event for Grade 12 Students, Faculty of Applied Science (FAS), SFU, 2020

School of Computing Science Services

- Tenure and Promotion Committee (External) Member, School of Computing Science, SFU, 2022-2023

School of Engineering Science Services

- **Computer Option Co-Chair**, School of Engineering Science, SFU, 2021-present
- Research Space Committee Member, School of Engineering Science, SFU, 2022-present
- Tenure and Promotion Committee Member, School of Engineering Science, SFU, 2023-2024
- Undergraduate Curriculum Committee Member, School of Engineering Science, SFU, 2023-2024
- Computer Engineering Faculty Search Committee Member, School of Engineering Science, SFU, 2023-2024
- School Director Search Committee Member, School of Engineering Science, SFU, 2021-2022
- Graduate Program Committee Member, School of Engineering Science, SFU, 2020-2021
- Tenure and Promotion Committee Member, School of Engineering Science, SFU, 2020-2021
- Strategic Vision Committee Member, School of Engineering Science, SFU, 2020-2021
- Computer Engineering Faculty Search Committee Member, School of Engineering Science, SFU, 2020

Conference and Workshop Organizing Committee Member

- **General Chair**, The 36th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2025)
- **Program Chair**, 32nd IEEE Reconfigurable Architectures Workshop (RAW 2025), co-located with 39th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2025)
- **Program Chair**, 31st IEEE Reconfigurable Architectures Workshop (RAW 2024), co-located with 38th IEEE International Parallel and Distributed Processing Symposium (IPDPS 2024)
- **Program Co-Chair**, 18th IEEE Biennial Pacific Rim Conference on Communications, Computers and Signal Processings (PacRim 2024)
- Poster Chair, 2024 IEEE International Symposium on Workload Characterization (IISWC 2024)
- Publicity Chair, 20th Applied Reconfigurable Computing (ARC 2024)
- **Organizing Chair**, Workshop on Research Open Automatic Design for Neural Networks (ROAD4NN 2020-2023), co-located with ACM/IEEE Design Automation Conference (DAC 2020-2023)
- Demo Night Co-Chair, The 31th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2023)
- Organizing Committee Member, 1st Languages, Architectures, and Tools for Heterogeneous Computing Workshop (LATHC 2023), co-located with IEEE/ACM International Symposium on Code Generation and Optimization 2023 (CGO 2023)
- Publicity Chair, The 32nd IEEE International Conference on Field-Programmable Logic and Applications (FPL 2022)
- Workshop Chair and Travel Awards Chair, The 30th IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM 2022)
- Special Session Chair, The 32th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2021)

- Finance and Publicity Co-Chair, 2020 IEEE International Symposium on Workload Characterization (IISWC 2020)
- Travel Grant Committee Member, The 28th ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA 2020)
- Publicity Chair (and Publication Chair), The 30th IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP 2019)
- Organizing Chair, International Workshop on Reconfigurable Acceleration in Datacenters (ReconfigAccel 2018), In Conjunction with the 32nd ACM International Conference on Supercomputing (ICS 2018)
- Sponsor Co-Chair, The 32nd ACM International Conference on Supercomputing (ICS 2018)
- Registration & Travel Awards Chair, The 23rd IEEE Symposium on High Performance Computer Architecture (HPCA 2017)
- Poster Session Chair, Center for Domain-Specific Computing 2014 Annual Review, 2015 Semi-Annual Review, 2015 Annual Review, and 2017 Semi-Annual Review

Conference Technical Program Committee Member

- ACM/SIGDA International Symposium on Field-Programmable Gate Arrays (FPGA), 2020-2025
- IEEE International Symposium on Field-Programmable Custom Computing Machines (FCCM), 2022-2025
- IEEE International Conference on Field-Programmable Logic and Applications (FPL), 2022-2024
- IEEE International Conference on Field Programmable Technology (FPT), 2021-2024
- ACM/IEEE Design Automation Conference (DAC), 2021-2024
- IEEE/ACM Design Automation and Test in Europe (DATE), 2018-2022, 2024-2025
- IEEE International Symposium on High Performance Computer Architecture (HPCA), 2023
- IEEE/ACM International Symposium on Microarchitecture (MICRO), 2022
- IEEE International Conference on Computer Design (ICCD), 2017, 2021
- IEEE International Parallel and Distributed Processing Symposium (IPDPS), 2021
- IEEE International Conference on Application-specific Systems, Architectures and Processors (ASAP), 2019-2021
- ACM SIGPLAN/SIGBED International Conference on Languages, Compilers, and Tools for Embedded Systems (LCTES), 2020
- Annual Conference of Advanced Computer Architecture (ACA), 2020
- International Symposium on Advanced Parallel Processing Technologies (APPT), 2019
- IEEE International Symposium on Workload Characterization (IISWC), 2017

Conference External Review Committee Member

- ACM/IEEE International Symposium on Computer Architecture (ISCA), 2021-2023, 2025
- IEEE/ACM International Symposium on Microarchitecture (MICRO), 2021, 2023

Journal Editing

- **TRETS Co-Guest Editor**, ACM Transactions on Reconfigurable Technology and Systems (TRETS) Special Issue on RAW 2024 (31st IEEE Reconfigurable Architectures Workshop), 2024.
- **TODAES Co-Guest Editor**, ACM Transactions on Design Automation of Electronic Systems (TODAES) Special Issue on High-Level Synthesis for FPGA: Next-Generation Technologies and Applications, 2021.

- **JSPS Co-Guest Editor**, Springer Journal of Signal Processing Systems (JSPS) Special Issue on ASAP 2019 (Application-specific Systems, Architectures and Processors), 2019.

Journal Reviewer

- **Note:** journals are first sorted by publisher, and then sorted by impact factor
- IEEE Transactions on Parallel and Distributed System (TPDS) Special Section on "Parallel and Distributed Computing Techniques for AI, ML and DL", 2020, Program Committee Member
- IEEE Transactions on Parallel and Distributed Systems (TPDS), 2017
- IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), 2016-2019
- IEEE Transactions on Circuits and Systems II (TCAS-II), 2018, 2022
- IEEE Access, 2016, 2018-2021
- IEEE Transactions on Computers (TC), 2016-2017, 2019-2021
- IEEE Micro, 2018, 2020-2021
- IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems (TCAD), 2018-2024
- IEEE Transactions on Very Large Scale Integration Systems (VLSI), 2017
- IEEE Computer Architecture letters (CAL), 2016-2017
- IEEE Transactions on Artificial Intelligence (TAI), 2023
- IEEE Transactions on Multi-Scale Computing Systems (TMSCS), 2018
- ACM Computing Surveys (CUSR), 2020
- ACM Transactions on Reconfigurable Technology and Systems (TRETS), 2019, 2022-2024
- ACM Transactions on Cyber-Physical Systems (TCPS), 2020
- ACM Journal on Emerging Technologies in Computing Systems (JETC), 2016-2017
- ACM Transactions on Embedded Computing Systems (TECS), 2019
- ACM Transactions on Architecture and Code Optimization (TACO), 2016-2017, 2020
- ACM Transactions on Programming Languages and Systems (TOPLAS), 2016-2017
- Elsevier Journal of Simulation Modelling Practice and Theory (SIMPAT), 2019
- Elsevier Journal of Parallel and Distributed Computing (JPDC), 2016-2018
- Elsevier Microprocessors and Microsystems (MICPRO), 2017-2019
- Integration, the Elsevier VLSI Journal (INTEGRATION), 2016-2019
- Elsevier Journal of Parallel Computing (ParCo), 2015
- Concurrency and Computation: Practice and Experience (CPE), 2019
- Journal of Universal Computer Science (J.UCS), 2017

Grant Reviewer

- NSERC (Natural Sciences and Engineering Research Council of Canada) Discovery Grant Review, 2018, 2020-2023
- NSERC (Natural Sciences and Engineering Research Council of Canada) Idea to Innovation Grant Review, 2023
- Swiss National Science Foundation Grant Review, 2023-2024
- Israel Science Foundation Personal Research Grants Review, 2022-2023
- Mitacs (Mathematics of Information Technology and Complex Systems, Canada) Accelerate Grant Review, 2022
- US Department of Energy Office of Science Microelectronics Research Proposal Review, 2021