Silicon Wafers: Basic unit

- Silicon Wafers Basic processing unit
- 150, 200, 300 mm disk, 0.5 mm thick
- Newest ones 300 mm (12 inches)
- Typical process 25 - 1000 wafers/run
- Each wafer: 100 - 1000's of microchips (die)
- Wafer cost $10 - $100's
- 200 mm wafer weight 0.040 Kg
- Typical processing costs $1200/wafer (200 mm)
- Typical processed wafer value $11,000
  (all products, modest yield)
- Value/Mass of processed wafer $275,000/Kg

Production of Silicon Wafers

- Silicon starts as beach sand quartzite

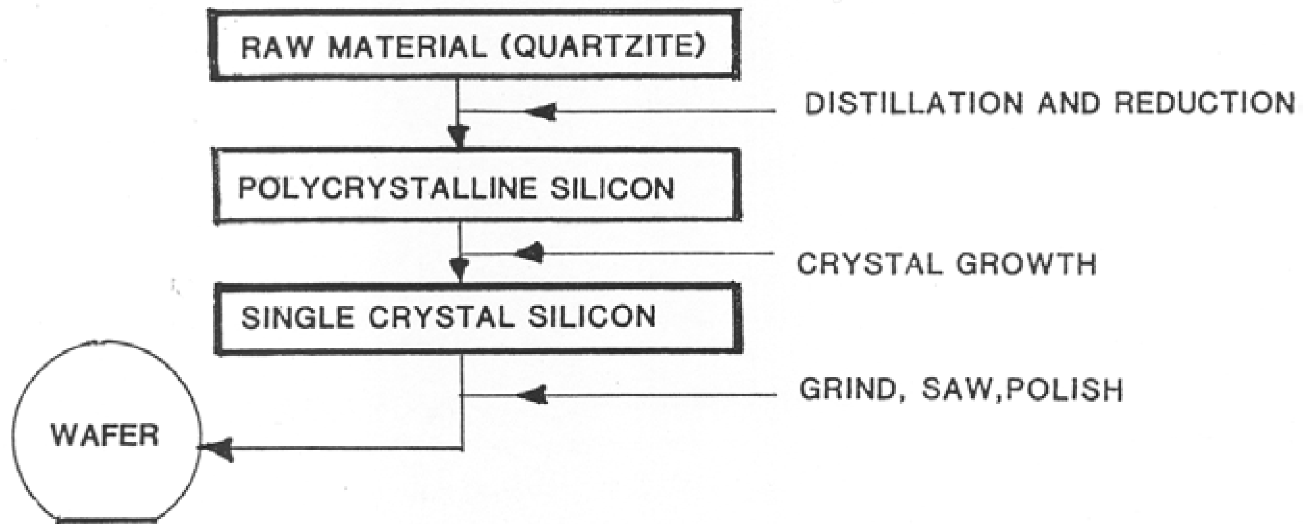


Fig. 4 Process sequence from starting material to polished wafer.

Conversion of Raw Sand into Metallurgical Grade Silicon

Step 1: Metallurgical Grade Silicon (MSG): 98% pure

- Start with white beach sand (quartzite or SiO_2)
- Use electric arc to melt in mixture of coal coke, wood at 2000°C
- Carbon removes impurities: molten Si drawn from bottom

- Takes considerable power: 12-14 KWh/Kg of Si

Step 2: Metallurgical Grade Silicon Chemical Purification

- Convert MSG powder to trichlorosilane ($SiHCl_3$)
  by reacting with anhydrous hydrogen chloride at 300°C
- Chlorine reacts with impurities to give $AlCl_3$,
- trichlorosilane ($SiHCl_3$) boils at 31.8°C

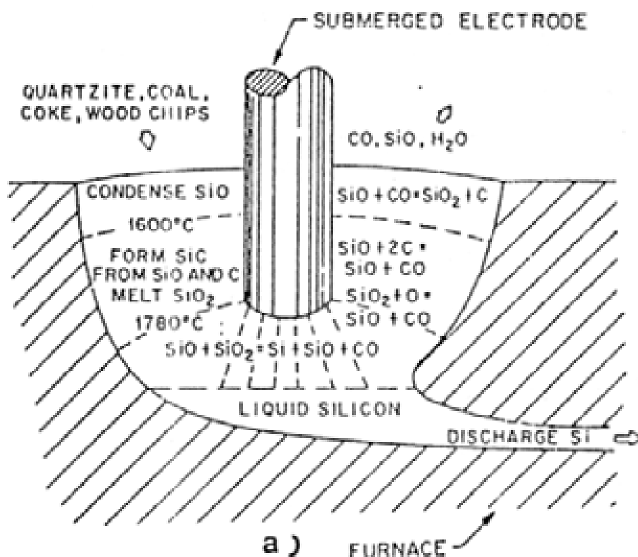


Fig. 5 (a) Schematic of submerged-electrode arc furnace for production of MGS[5].

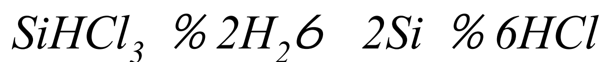
Metallurgical Grade Silicon into Polycrystalline Silicon

Step 3: Distill Trichlorosilane

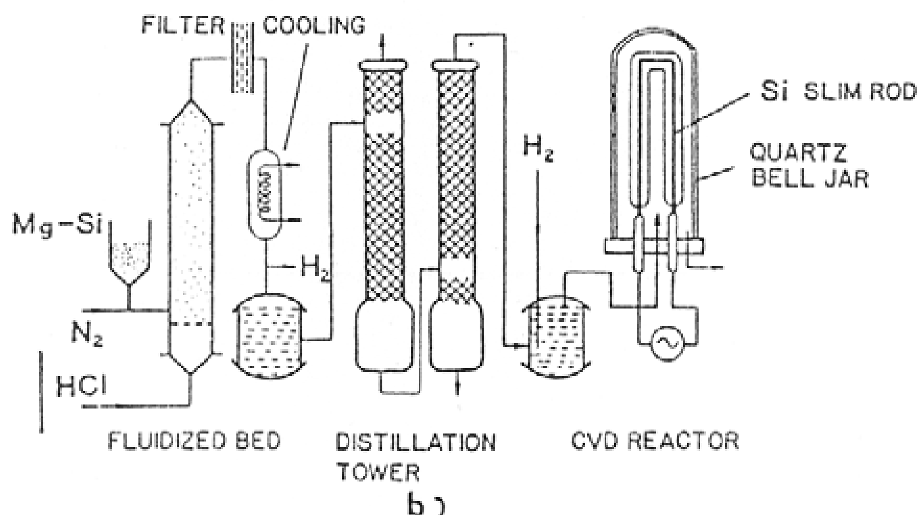
- Impurities reduce to parts per billion atoms (ppba) or $10^{13}/cm^3$
- Reduced by 10^8 from original values

Step 4: Silicon Chemical Vapour Deposition

- gaseous trichlorosilane ($SiHCl_3$) reacted with Hydrogen



- Si deposits out on rods with large crystals: Polycyrstalline
- Result Electronic Grade Silicon (EGS)
- Called the Siemens process
- Total production 3 million Kg 1985



(b) Schematic of fluidized bed, distillation tower, and CVD reactor developed by Siemens[9]

Czochralski Crystal Growth methods

- Czochralski (CZ) basic Silicon crystal growth method
- Melt Poly Si EGS at 1430ºC in quartz crucible
- Rotate crucible
- bring counter rotating seed crystal to melt
- Slowly draw seed from melt
- atoms of melt freeze out aligned with crystal planes of seed

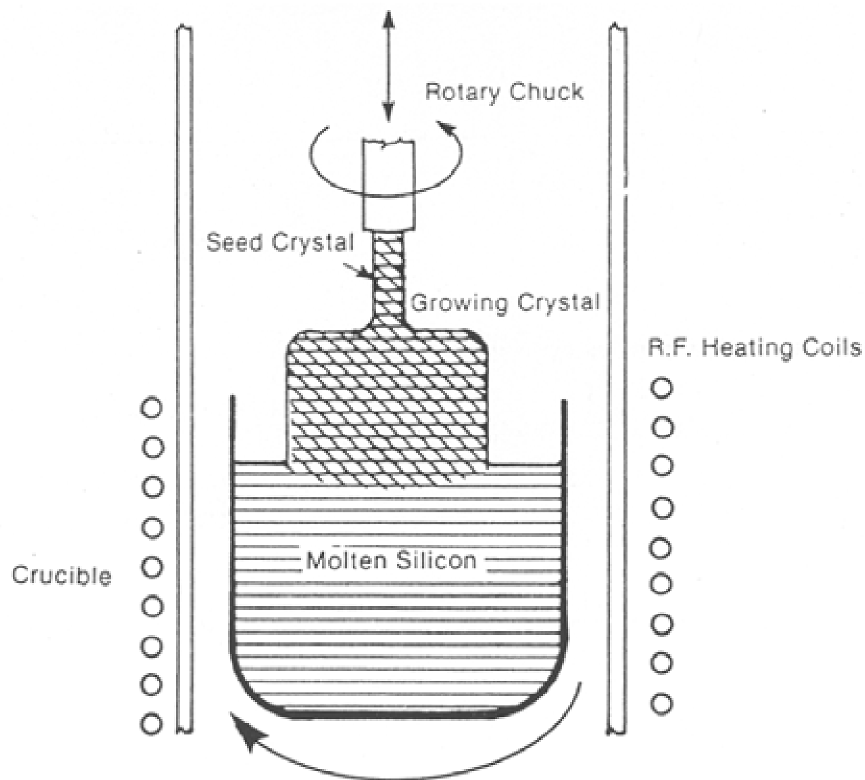


Figure 3.7 Czochralski crystal-growing system.

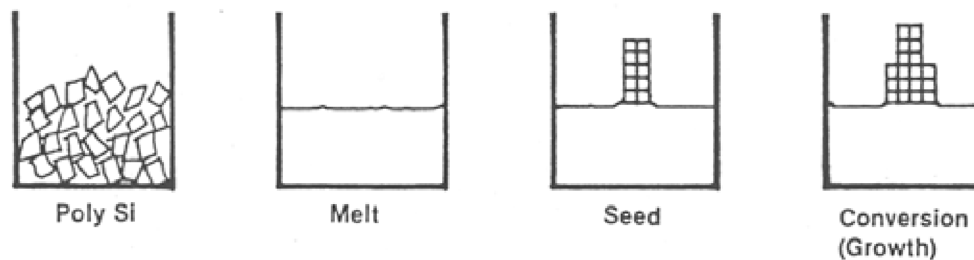


Figure 3.8 Crystal growth from a seed.

Czochralski Crystal Growth

- As seed drawn from melt initially grow narrow neck
- Dislocations (incorrect crystal alignment stopped at neck)
- as slow rate of pull (withdrawal) crystal diameter grows to max
- Maintain constant rotate/pull rate for uniformity eg 20 cm/hr

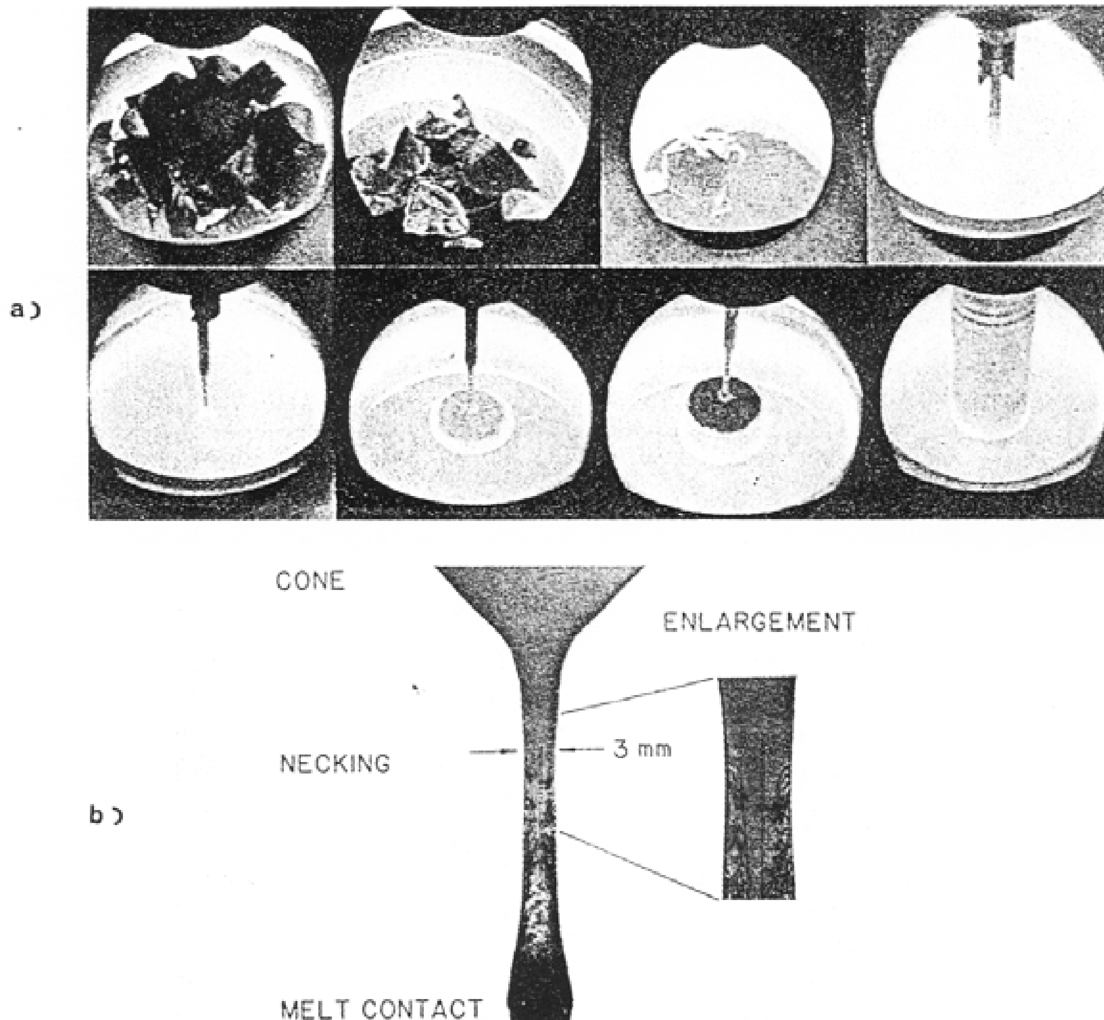


Fig. 8 (a) Illustration of several process steps during CZ crystal growth. Courtesy of Dynamit-Noble-Grace. (b) X-ray topograph of seed necking and conical part of crystal. Dislocations generated at the end of the seed crystal that contacted the molten zone grow out to the side surface of the neck and do not propagate into the main crystal[9]. Reprinted with permission of Academic Press.

Finished Czochralski Crystals

- Crystals up to 150 and 200 mm now possible
- Most recent advance: Magnetic Convection suppression

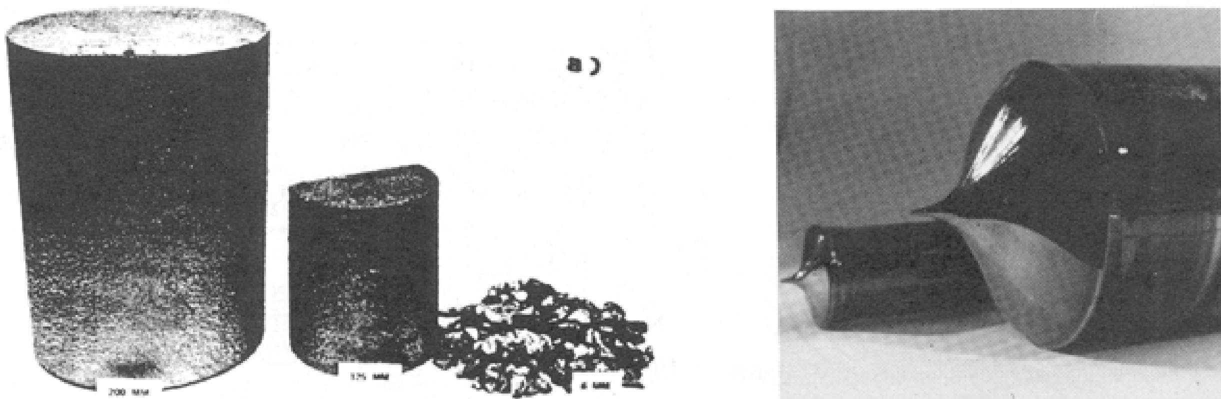


Fig. 6 (a) EGS in polysilicon form[5]. Reprinted with permission of the publisher, the Electrochemical Society. (b) 150 mm single-crystal CZ silicon ingot. Reprinted with permission of the Monsanto Eletronics Materials Company.

Movement of Impurities from Melt to Crystal

- To put dopants in wafer place impurity in melt
- Equilibrium concentration (solubility) different in solid, N_s than in liquid N_l (note solubilities often symbolized as C_s, C_l)
- Segregation ratio fraction of liquid dopant in solid

$$k = \frac{N_s}{N_l}$$

- Thus as crystal pulled melt dopant concentration changes with X, fraction of melt left

$$N_s = kN_{l0}(1 - X)^{[k-1]}$$

- Thus dopant concentration changes along length of crystal
- Thus impurities & dopants differ in each wafer

Table 1-1 Segregation coefficients for common impurities in silicon

Impurity		Segregation coefficient k†
Aluminum	(Al)	0.002
Antimony	(Sb)	0.3
Arsenic	(As)	0.3
Boron	(B)	0.72–0.8
Carbon	(C)	0.07
Copper	(Cu)	4×10^{-4}
Gallium	(Ga)	0.007–0.008
Gold	(Au)	2.2×10^{-5}
Indium	(In)	4×10^{-4}
Iron	(Fe)	8×10^{-6}
Oxygen	(O)	1.25
Phosphorus	(P)	0.35

†Where multiple values are given, literature values vary.

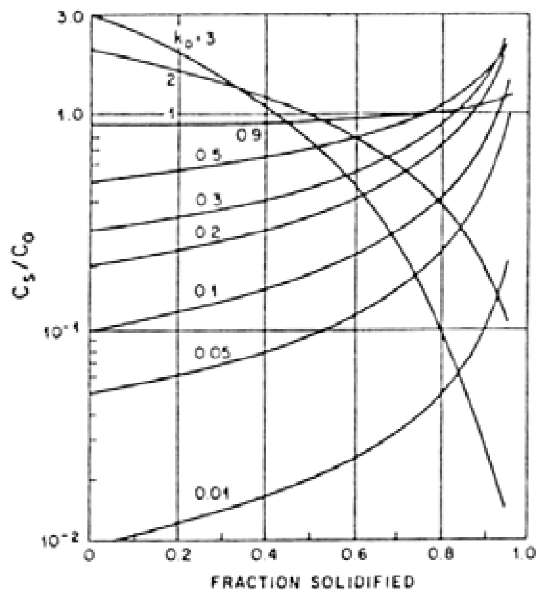


Fig. 10 Curves fron growth from the melt, showing the doping concentration in a solid as a function of ther fraction solidified. From W.G. Pfann, *Zone Melting*, 2nd Ed. 1966. Copyright © John Wiley and Sons. Reprinted with permission of John Wiley and Sons.

Float Zone Crystallization

- Float Zone (FZ) produces smaller wafers
- Start with polycrystalline Si rod
- Touch rod to seed crystal
- Heat with moving Radio Frequency (RF) coil
- Melts road near coil
- Move melt front from crystal to end and back
- leaves single crystal rod behind

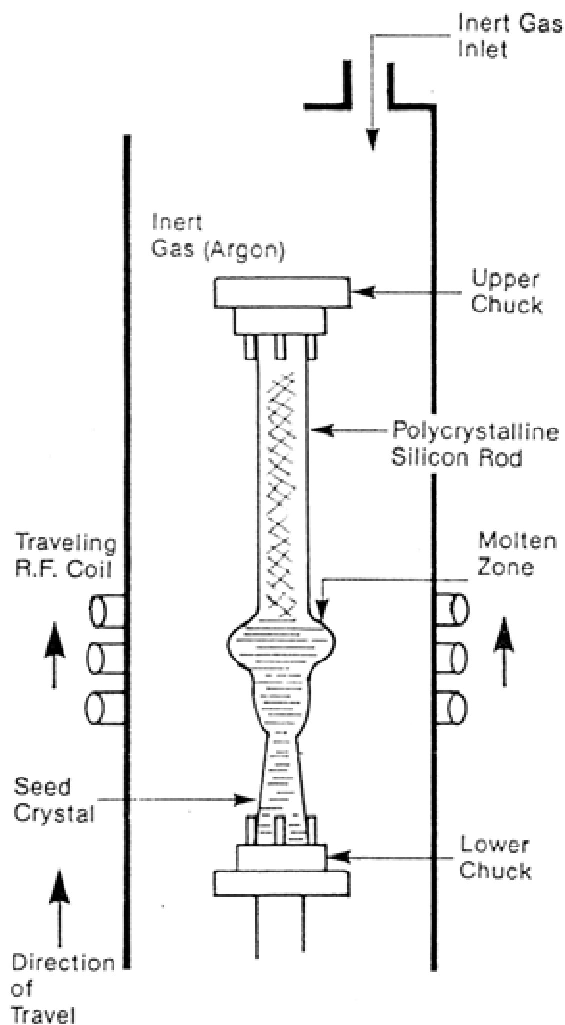


Figure 3.10 Float-zone crystal-growing system.

Comparison of CZ and FZ wafers

- FZ better impurity, but smaller size

PARAMETER	CZ	FLOAT ZONE
Large Crystal	Yes	Difficult
Cost	Lower	
Dislocations	$0 - 10^4/cm^2$	$10^3 - 10^5/cm^2$
Resistivity	Up to 100 ohm-cm	2000 ohm-cm Max.
Radial Resistivity	5 - 10%	5 - 10%
Oxygen Content	$10^{16} - 10^{18}$ atoms/cm^3	0 - Very Low

Figure 3.11 Comparison of CZ and float crystal-growing methods.

Table 2. COMPARISON of MATERIAL PROPERTIES and REQUIREMENTS for VLSI

Property	Czochralski	Float zone	Requirements for VLSI
Resistivity (phosphorus) n-type (ohm-cm)	1–50	1–300 and up	5–50 and up
Resistivity (antimony) n-type (ohm-cm)	0.005–10	–	0.001–0.02
Resistivity (boron) p-type (ohm-cm)	0.005–50	1–300	5–50 and up
Resistivity gradient (four-point probe) (%)	5–10	20	< 1
Minority carrier lifetime (μs)	30–300	50–500	300–1000
Oxygen (ppma)	5–25	Not detected	Uniform and controlled
Carbon (ppma)	1–5	0.1–1	< 0.1
Dislocation (before processing)(per cm^2)	$\leqslant 500$	$\leqslant 500$	$\leqslant 1$
Diameter (mm)	Up to 200	Up to 100	Up to 150
Slice bow (μm)	$\leqslant 25$	$\leqslant 25$	< 5
Slice taper (μm)	$\leqslant 15$	$\leqslant 15$	< 5
Surface flatness (μm)	$\leqslant 5$	$\leqslant 5$	< 1
Heavy-metal impurities (ppba)	$\leqslant 1$	$\leqslant 0.01$	< 0.001

Current common Si Wafer Sizes

- Since 1994 common sizes:
- 200 mm (8 inch) state of art fabrication
- 150 mm (6 inch) most 2nd level to front line fabs
- 125 mm (5 inch) Bastard size (only a few facilities)
- 100 mm (4 inch) Smallest production wafers: research
- 75 mm (3 inch) Obsolete size: still used in research
  (special order: more expensive than 4 inch)
- 300 mm (12 inch) now in some production
- Basically need to rebuild entire fab to change wafer size

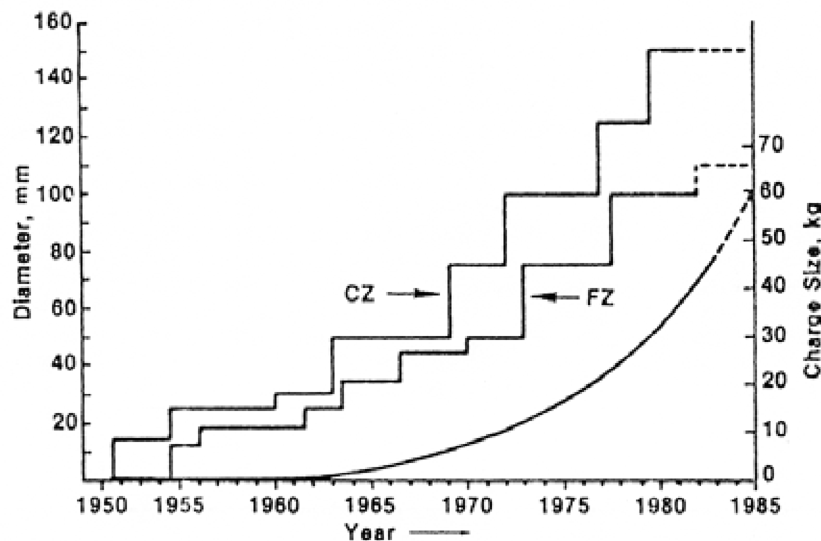


Fig. 7 The increase with time of CZ silicon crystal diameter and charge sizes[47]. Reprinted with permission of Semiconductor International.