# Silicon Etching (Ruska Ch. 6)

- Poly Crystalline Silicon widely used as a conductor•
- Called Poly Si:
- Modest resistance conductor
- Usually highly doped silicon
- Gate conductor in self aligned process
- Gate creates the position of the source/drain
- Poly Silicon etches similar to single crystal Si
- Changes depend on crystal size and doping

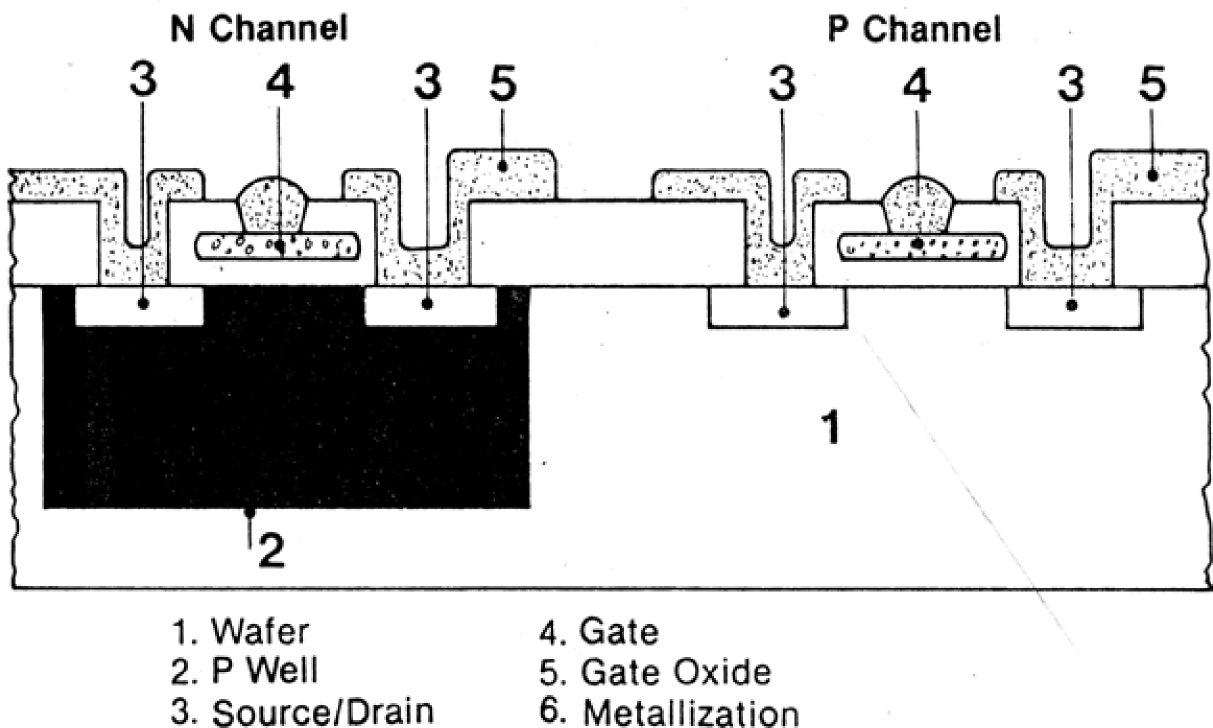
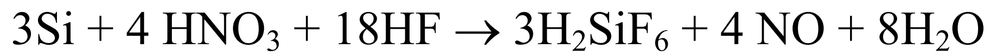



**Figure 13.5** CMOS transistor polysilicon gate electrode. (*From Ref. 4.*)

## Etching Silicon

- Typical etch: HF and $HNO_3$ (nitric acid) combination
- Oxidation/reduction reaction
- Nitric oxidizes the silicon
- HF removes the oxide formed



$$3Si + 4\,HNO_3 + 18HF \rightarrow 3H_2SiF_6 + 4\,NO + 8H_2O$$

- Ratio of HF/Nitric set etch rate

# Typical Isotropic Silicon Etches

- Typically dilute with Acetic acid $CH_3COOH$
- Reduces the etch rate

## 2A. Isotropic Silicon Etches

Table 16

| | Formula | Comments |
|---|---|---|
| 1 | HF, $HNO_3$ | See diagram |
| 2 | HF, $HNO_3$, $H_2O$ or $CH_3COOH$ | Various combinations give different etch rates |
| 3 | 900 ml $HNO_3$, 95 ml HF, 5 ml $CH_3COOH$, 14g $NaClO_2$ | 15 um/min |
| 4 | 745 ml $HNO_3$, 105 ml HF, 75 ml $CH_3COOH$, 75 ml $HClO_4$ | 170 A/sec |
| 5 | 50 ml HF, 50 ml $CH_3COOH$, 200 mg $KMnO_4$ (fresh) | Epi Etching 0.2 um/min |
| 6 | 108 ml HF, 350g $NH_4F$ per L $H_2O$ | Epi Etching<br>n type 0.2-0.6 ohm-cm; 0.43 A/min<br>p type 0.4 ohm-cm; 0.45 A/min<br>p type 15 ohm-cm; 0.23 A/min |

# Diluted HF/Nitric/Acetic

- Etch rates depend on dilution

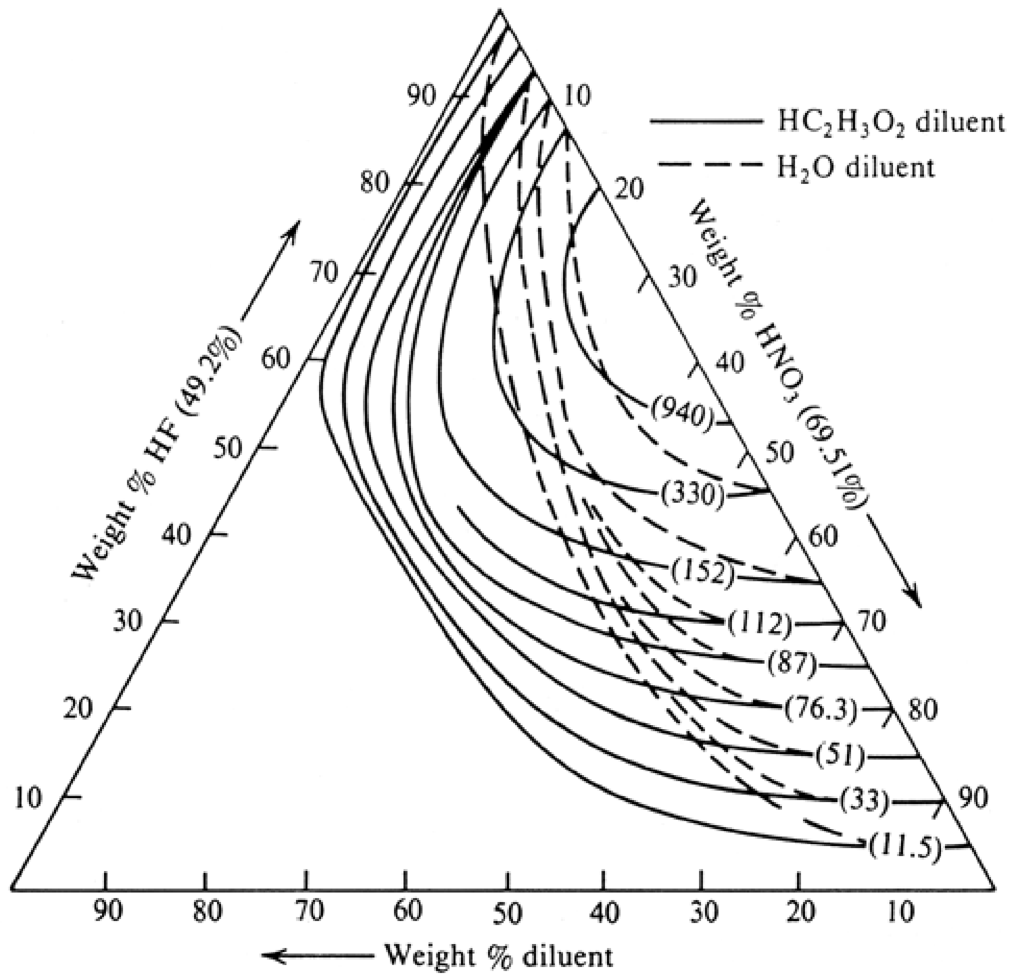



**Figure 6-8** Etch rates for single-crystal silicon as a function of HF, $HNO_3$, and diluent concentrations. These etch rates are for dual-sided etching and must be divided by 2 to obtain the etch rate on a single surface. (*Reference 8. Reprinted by permission of the publisher, The Electrochemical Society, Inc.*)

# Common PolySilicon Etches

- Similar to single crystal
- Must control etch rate

**POLYSILICON ETCHES**
**Table 7**

| | Formula | Comments |
|---|---|---|
| 1 | Shipley remover 1112A | See Shipley data sheet |
| 2 | 70.4% $HNO_3$, 28% $H_2O$, 1.4% HF | 21$^oC$ |
| 3 | 100 ml $HNO_3$, 40 ml $H_20$, 28 ml HF | 8000 A/min |
| 4 | 33 ml $CH_3COOH$, 26 ml $HN0_3$ 1 ml HF | 1500 A/min |
| 5 | 6 ml $H_20_2$, 10 ml $NH_4F$, 1 ml HF | 2000 A/min |
| 6 | 80% $HN0_3$, 20% $HBF_4$ 1.0 g1l $NH_4BF_4$ | 20$^oC$ |
| 7 | IM solutions Tetramethylammonium Hydroxide | 25-45$^oC$ |

# Anisotropic Etching of Silicon

- Etching that proceeds along crystalline planes
- typically <111> plane slowest
- <100> fastest (ratio 30:1 to 100:1)
- Used extensively in micromachining & power transistors
- <100> wafers get "V" groves
- <110> wafers get vertical side walls

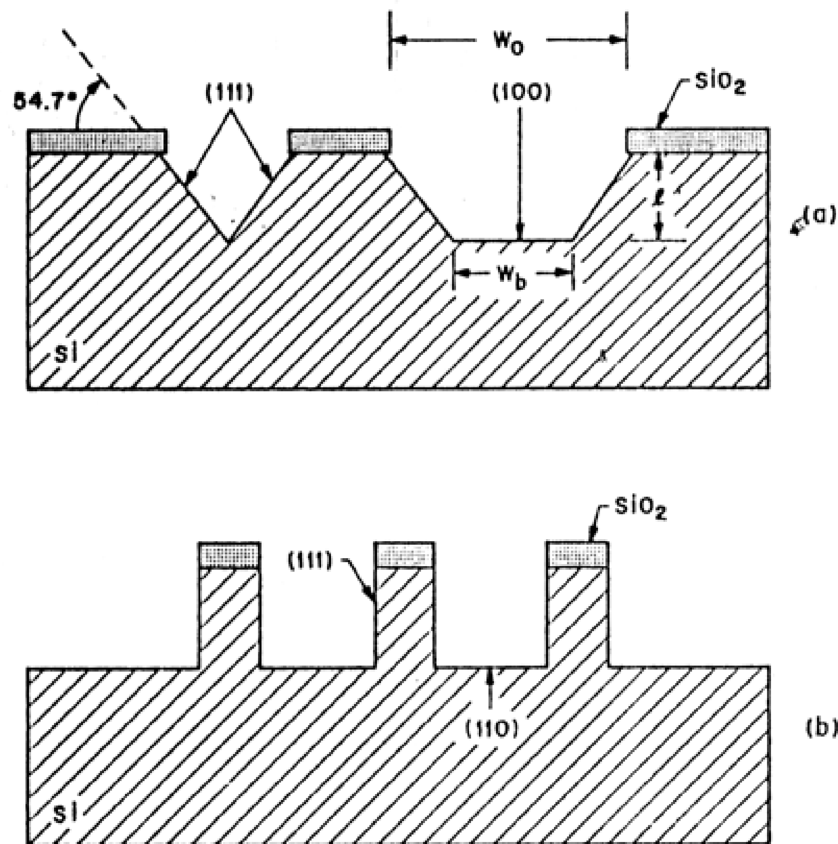



**Fig. 14** Orientation-dependent Si etching (a) etch pattern profiles on <100>-Si, (b) profiles on <110>-Si[22]. (© 1978 IEEE).

# Typical Anisotropic Etchants of Silicon

- EDP (Ethylenediamine Pyrocatecol & water) most common
- Advantages: attacks silicon, not oxide or aluminum
- Disadvantage: poisonous
- Potassium Hydroxide (KOH)
- Advantages: good crystal plane selectivity silicon
- Advantages: attacks aluminum

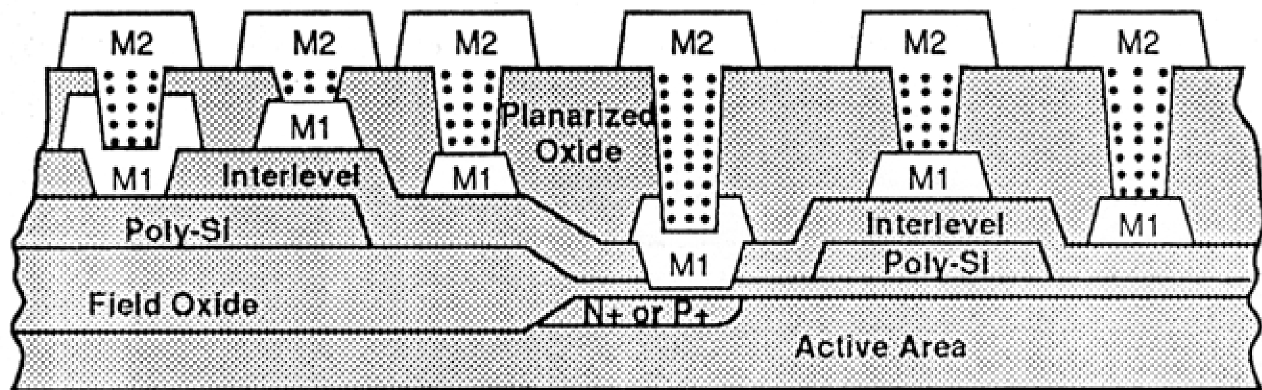
**Table 6-2 Some formulations for crystallographically selective etching of silicon**

| Ingredients | Composition | Temperature (°C) | Relative rate 100 | Relative rate 110 | Relative rate 111 | Absolute rate† | Reference |
|---|---|---|---|---|---|---|---|
| KOH in water/ isopropanol | 19 wt. % KOH | 80 | — | *400* | 1 | 0.59 μm $sec^{-1}$ | 9 |
| $N_2H_4$/water | 100 g/50 mliters | 100 | *10* | 1 | — | 0.3 | 10 |
| Ethylenediamine/ Pyrocatecol/ water | 17 mliters<br>3 g<br>8 mliters | 110 | *50* | 30 | 3 | 50 | 11 |

† Etch rate for fastest-etching orientation, i.e., the one italicized under relative rate.

## Aluminum Multilayer Structures

- Aluminum most common conductor in CMOS
- Conductive and easy to deposit
- Easy to etch
- Problem is to make multilevel structures
- Must make contact between Al layers
- Aluminum grows a protective insulating oxide

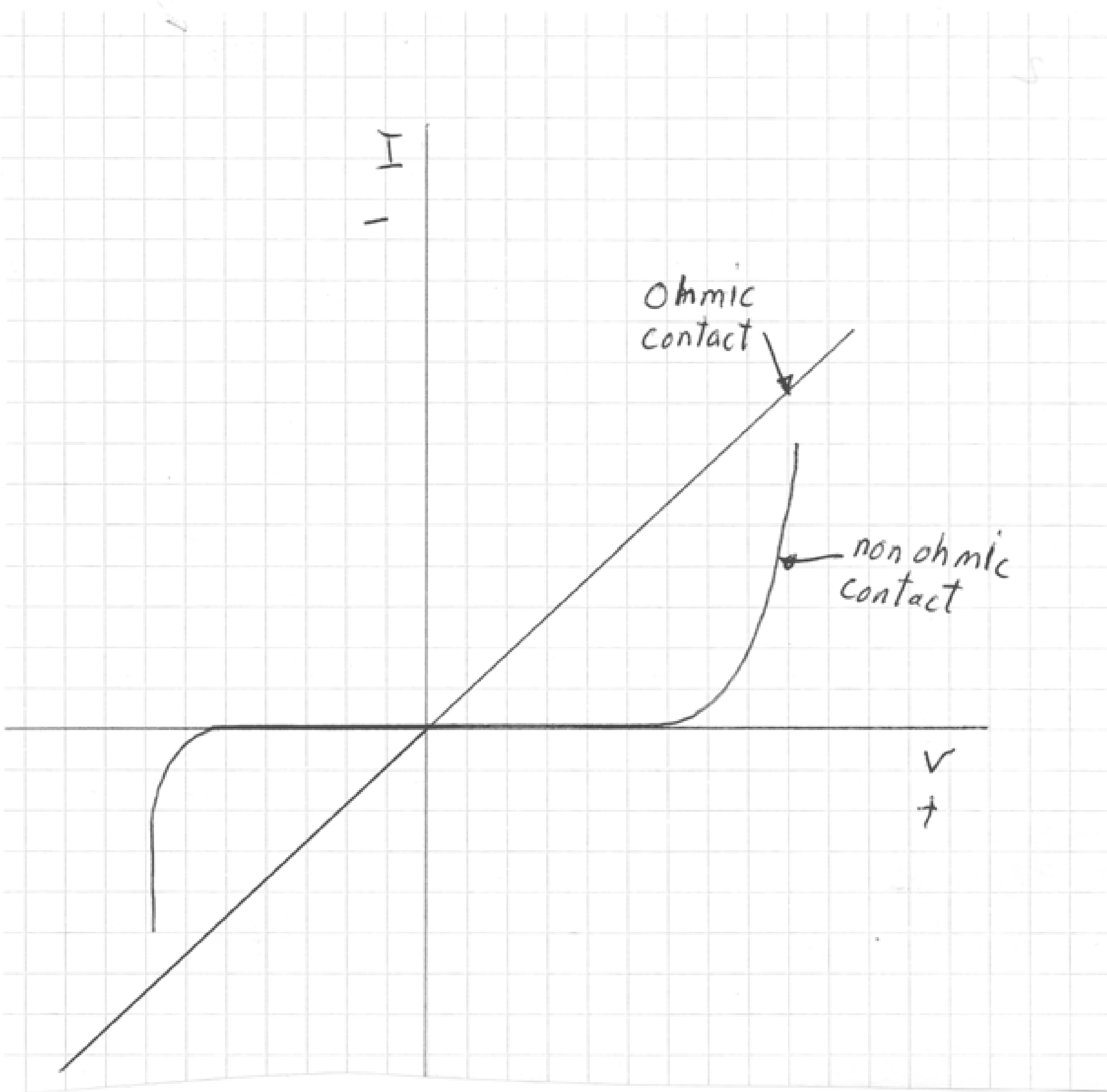



:: Via Plugs    M1 = First Metal    M2 = Second Metal

**Figure 13.2** Cross section of typical planarized two-level metal VLSI structure showing range of via depths after planarization. (*Courtesy of Solid State Technology.*)

## Ohmic Contacts

- Aluminum oxide can create diode like contacts
- Want a pure Ohmic contact (linear resistance)
- Get this by sinter in dry nitrogen at end
- Typical 450$^{o}$C for 30 minutes
- Removes the oxide, creates ohmic contact



## Aluminum Alloys

- Pure aluminum has reliability problems
- Sinter & high temperature creates difficulties
- Add Copper and Silicon
- Makes it much harder to etch

**Table 1. PROPERTIES OF ALUMINUM AND ALUMINUM ALLOY THIN FILMS**

| Name | Symbol | Melting Point (°C) | Al /Si Eutectic (°C) | Density (g/cm$^3$) | Resistivity (μΩ–cm) |
|---|---|---|---|---|---|
| Aluminum | Al | 660 | 577 | 2.70 | 2.7 |
| Aluminum/ 4% Copper | Al 4%Cu | 650 | ~577 | 2.95 | 3.0 |
| Aluminum/ 2% Silicon | Al 2%Si | 640 | ~577 | 2.69 | 2.9 |
| Aluminum/ 4% Copper 2% Silicon | Al 4%Cu 2%Si | | ~577 | 2.93 | 3.2 |

## Aluminum Spike Through

- When Aluminum heated penetrates silicon
- Si moves in Al, Al into Si
- Get spikes which can short junctions
- Suppressed by adding 1-2% Si to Al

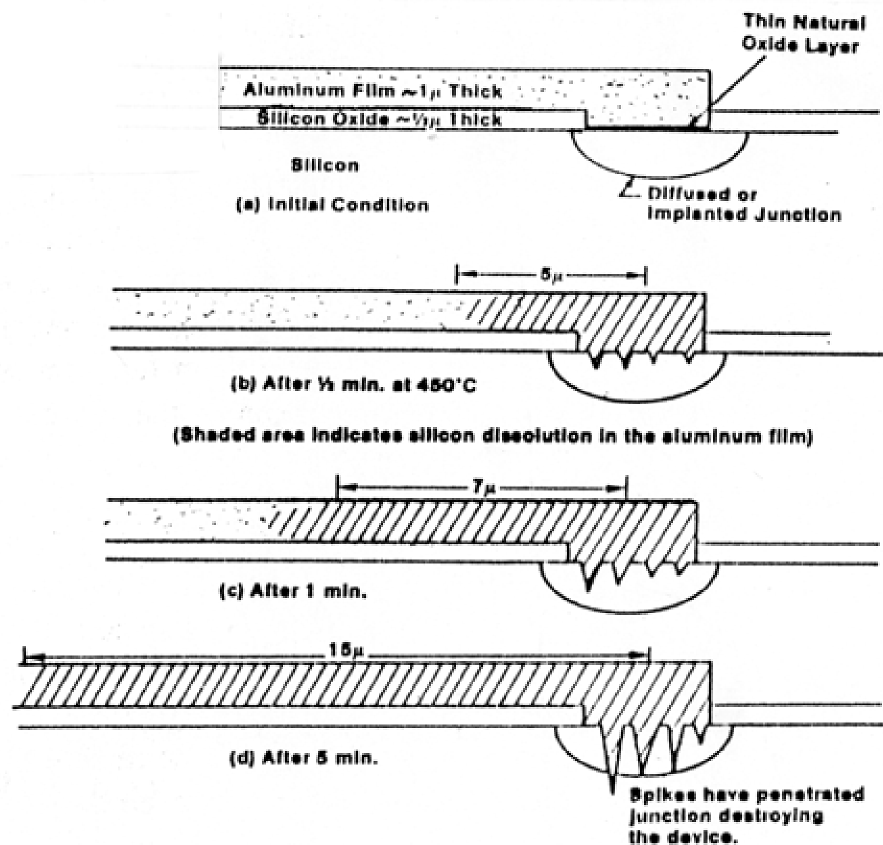



**Fig. 2** Junction spiking and silicon migration during contact sintering.

## Phase diagram

- Silicon 1.5% Aluminum Eutectic
- Lowest melting point alloy

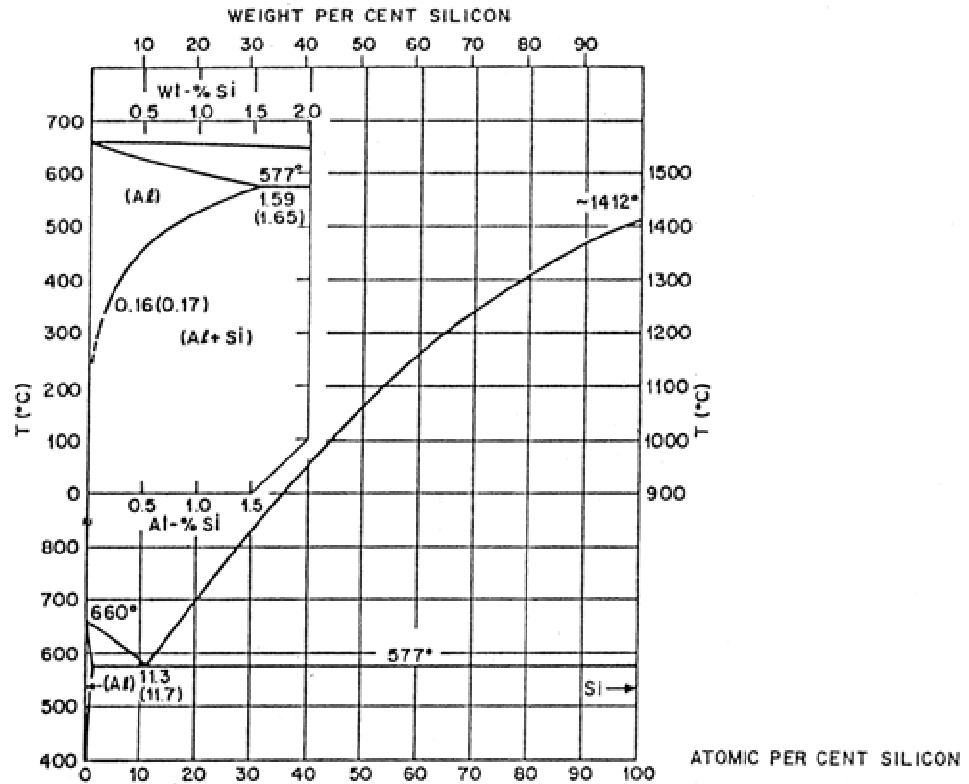
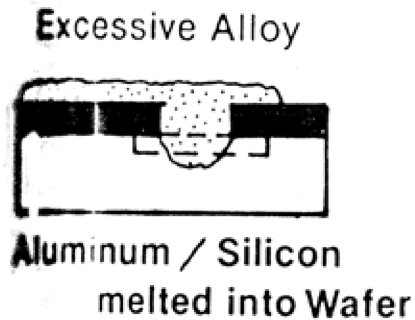
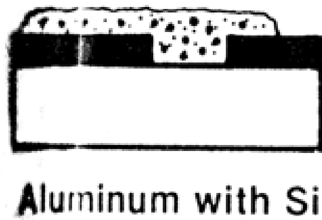



Fig. 1 Phase diagram of the aluminum-silicon system. From M. Hansen and A. Anderko, *Constitution of Binary Alloys*, 1958. Reprinted with permission of McGraw-Hill Book Co.

## Preventing Spike Through

- Adding Si to Al prevents spikes
- Also put down Barrier metal layers
- Tungstan, Molybdenum most common
- Refractory metals



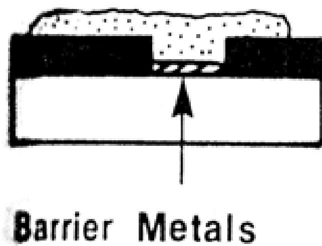




**Figure 13.6** Eutectic alloying of aluminum and silicon contacts.

## Aluminum and Hillocks

- When Al heated grows Hillocks
- Spikes up to 1 micron high!
- Can punch through intermetal glass layers
- Add copper to suppress
- Also for electromigration:
  tendency of metal to move when current applied
- Problem is Si/copper makes etching difficult

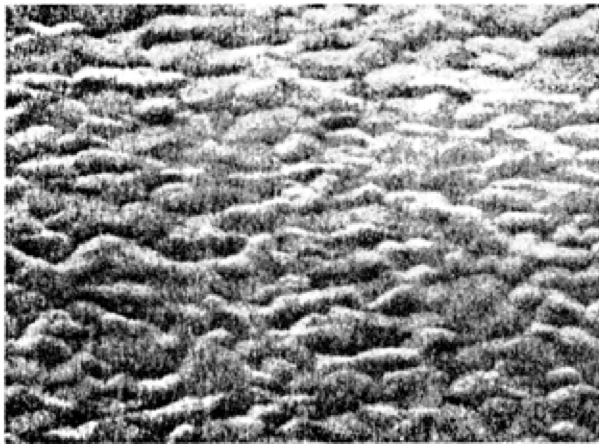
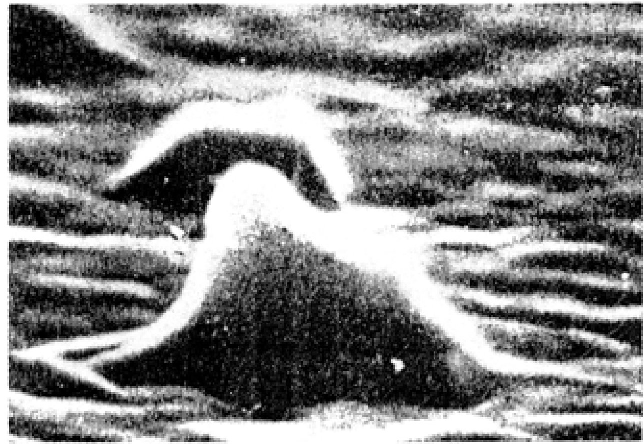



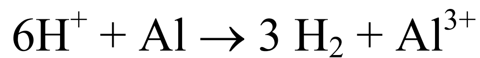
Fig. 36 Comparison of hillock-free and hillock containing films.

## Aluminum Etching

- Oxidation: removal of electrons or ions from material

$$M \rightarrow M^{+} + e^{-}$$

- Reduction: addition of electrons to reactant
- Redox reaction: both oxidation and reduction
- Aluminum etches are redox reactions



$$6H^{+} + Al \rightarrow 3\ H_2 + Al^{3+}$$

- Must remove aluminum oxide for reaction

## Typical Aluminum Etchants

- Most are Phosphoric Acid based ($H_3PO_4$)
- Acetic for dilution
- Note: without oxide Al would etch in water

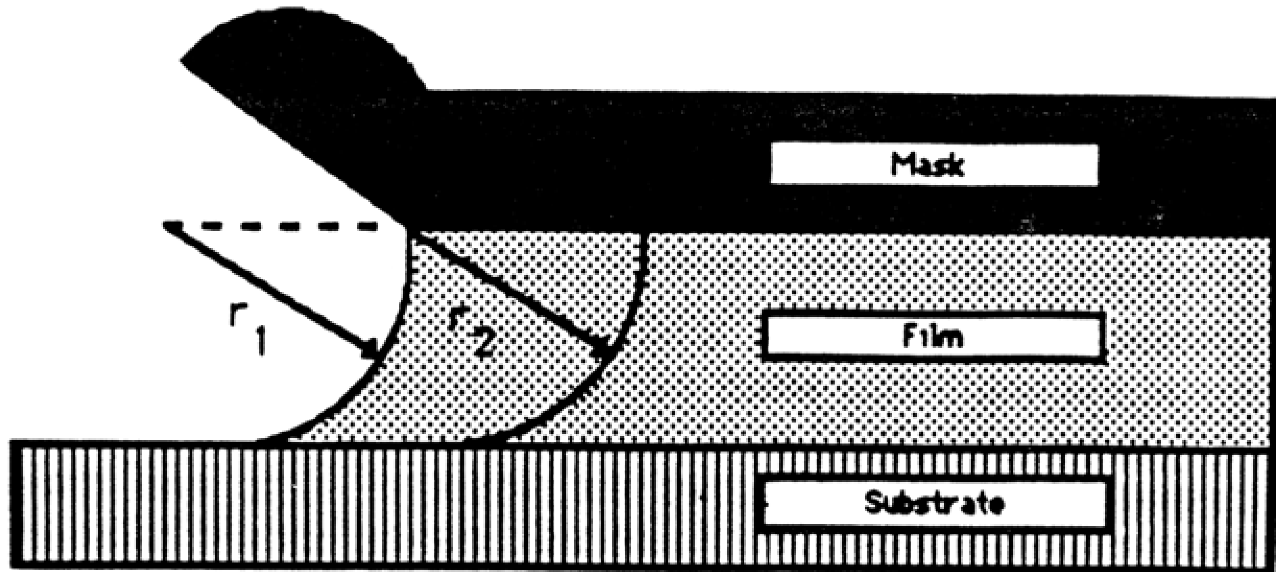
FORMULAS FOR ALUMINUM ETCHING

Table 11

| | Formula | Comments |
|---|---|---|
| | Phosphoric Acid Based Solutions | |
| 1 | 77 ml $H_3PO_4$, 20 ml $CH_3COOH$, 8 ml $HNO_3$ | 40 - 60°C |
| 2 | 73 ml $H_3PO_4$, 3.5 ml $CH_3COOH$, 4 ml $HNO_3$, 19.5 ml $H_20$ | 40 - 60°C |
| 3 | 90 ml $H_3PO_4$, 5 ml $HNO_3$, 5 ml $H_20$ | 40 - 60°C |
| 4 | 80 ml $H_3PO_4$, 5 ml $CH_3COOH$, 5 ml $HNO_3$, 10 ml $H_20$ | 40 - 60°C |
| 5 | 80 ml $H_3PO_4$, 5 ml $HNO_3$, 15 ml $H_20$ | 40 - 60°C |
| 6 | 40 ml $H_3PO_4$, 40 ml $CH_3COOH$, 10 ml $HNO_3$, 10 ml $H_20$ | 40 - 60°C |
| 7 | 75 ml $H_3PO_4$, 5 ml $HNO_3$, 20 ml $H_20$ | 40°C |

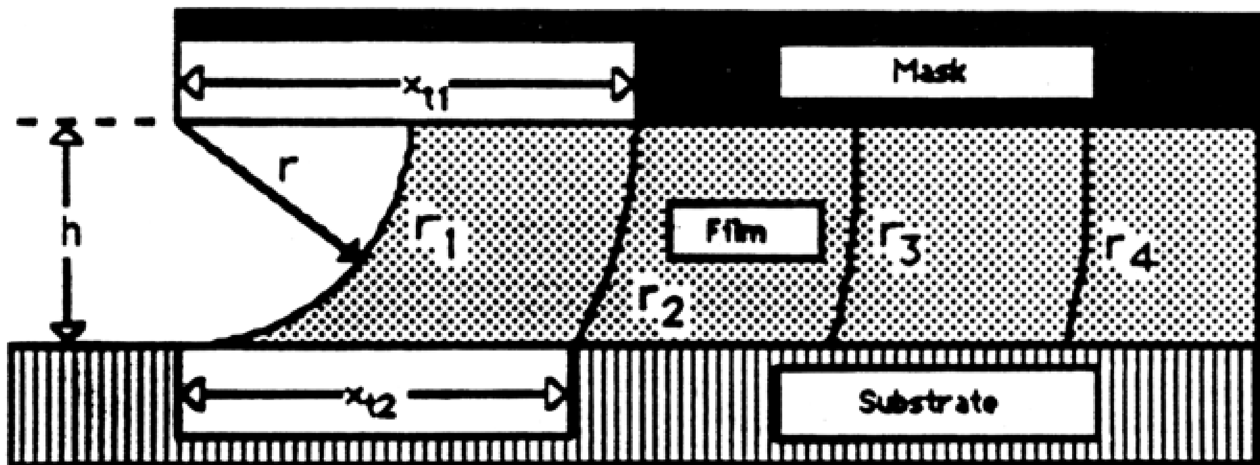
## Creating a Sloped Sidewall for Al

- Want sloped sidewall for step coverage
- Thus over etch aluminum
- Allow resist to lose adhesion




Moving Interface Etching

Fig 17a




Stationary Interface Etching

Fig 17b

## Sand Removal in AlSi or AlSiCu

- Metal etch leaves Al rich Si sand
- Copper makes reaction worse
- must remove with a "sand remover" wet etch
  29% $H_2O$, 70% HF, 1% $HNO_3$

# Lift Off Techniques

- Put defined resist below metal deposition
- Al goes through holes
- Then dissolve resist
- Extra Al floats away
- Problem is the "Sky is Falling Syndrome"
  material left behind

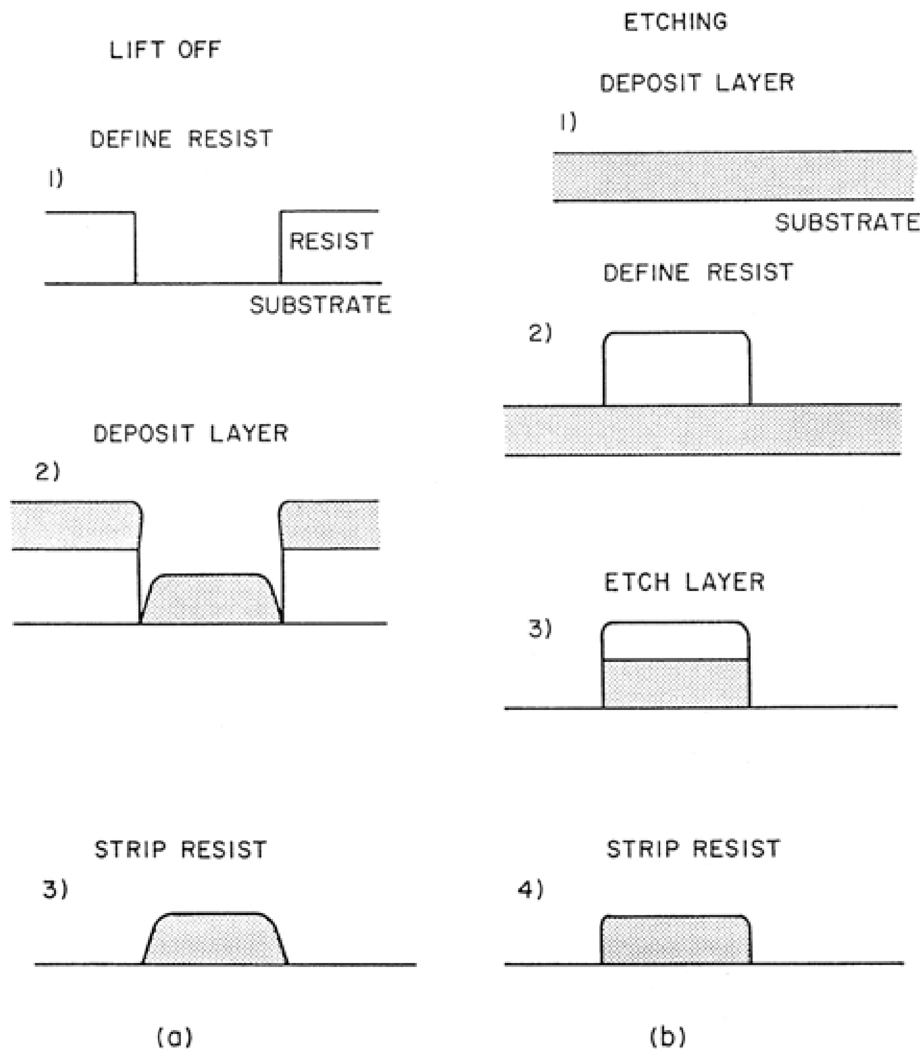



**FIGURE 9**
A schematic representation of two techniques for transferring resist features into a layer. (a) Shows the resist/deposition strip sequence of lift off, and (b) shows the deposit/resist/etch/strip sequence of etching.