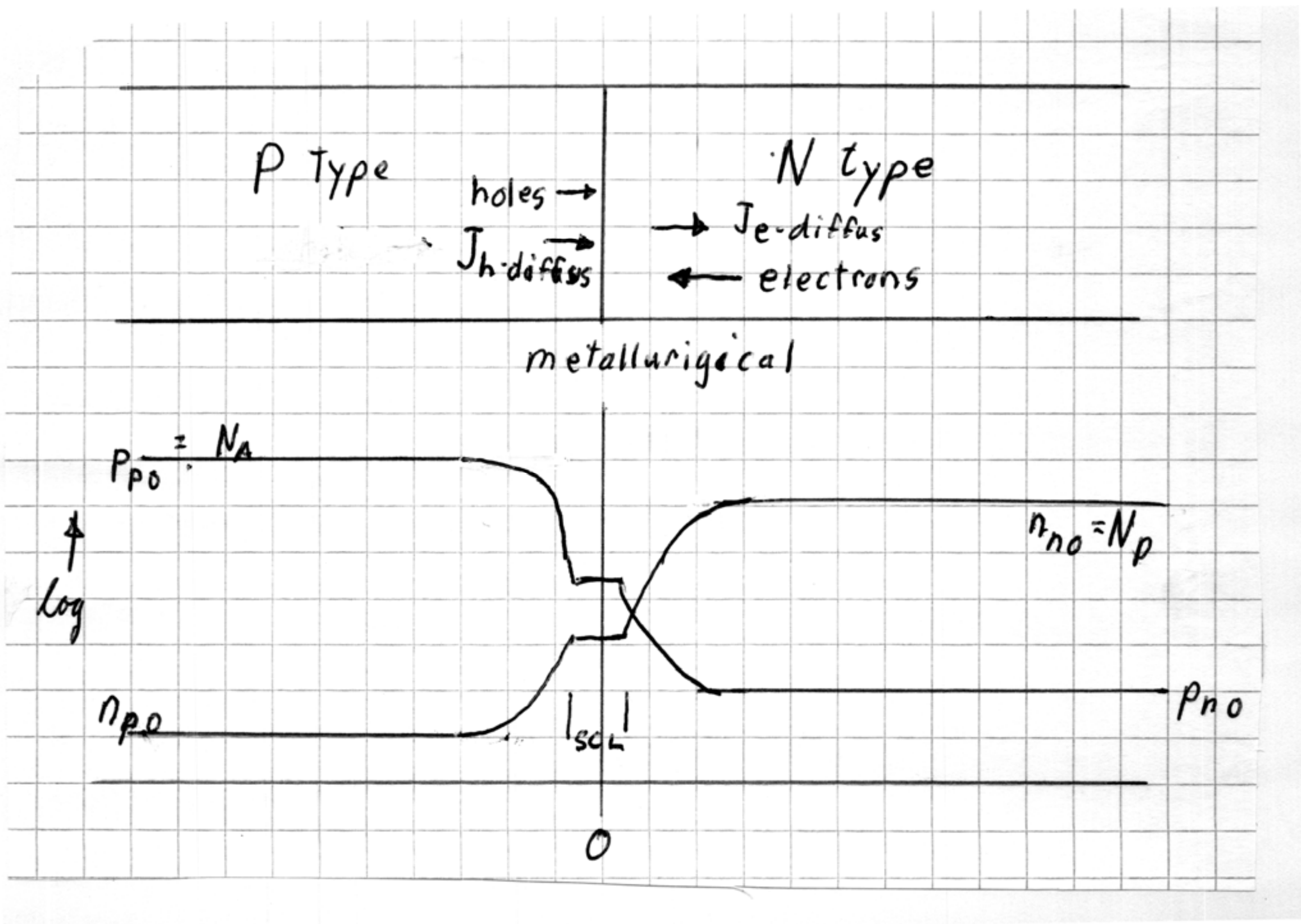
The PN Junction Diode

- PN junction diode is the basis of all semiconductor devices.
- Consider a block of P doped semiconductor,
- Attach it to block of N type,
- Forms an "abrupt" or "metallurgical" junction.
- Diffusion of electrons from N side, holes from P side Majority Carriers diffuse into minority region
- This sets up and electric field within the junction
- Result is a one directional, diode like I/V curve
- How is this obtained?



Photolithography method

- Grow an glass (oxide) on wafer (heat silicon in steam or air)
- Use photolithography to define (pattern) an area
- Etch away glass to create opening
- Use diffusion or Ion Implantion to create junction

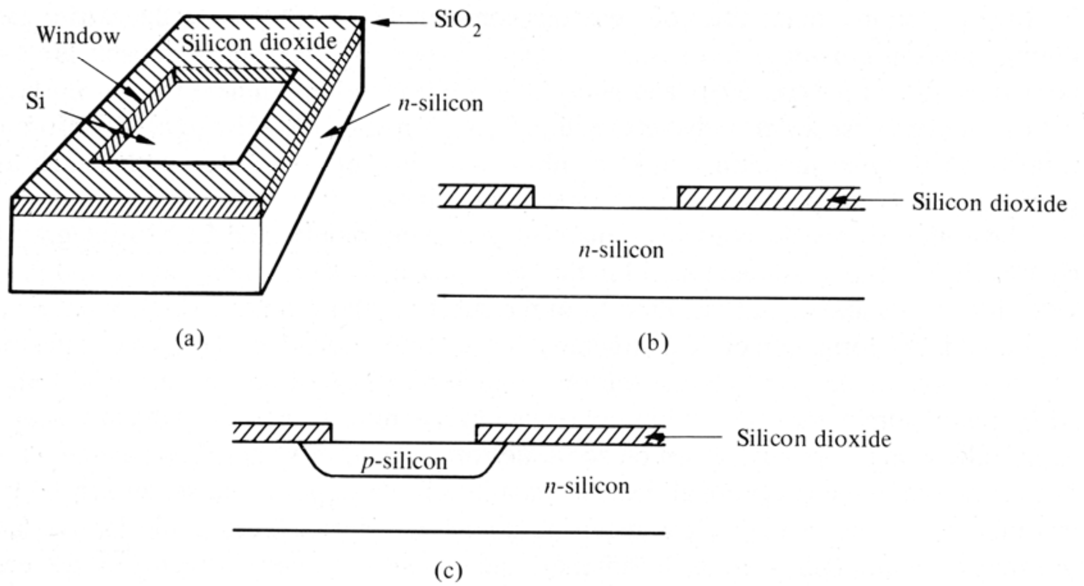


Fig. 1.2 (a) Window in SiO; (b) cross section before diffusion; (c) cross section after *p*-impurity diffusion.

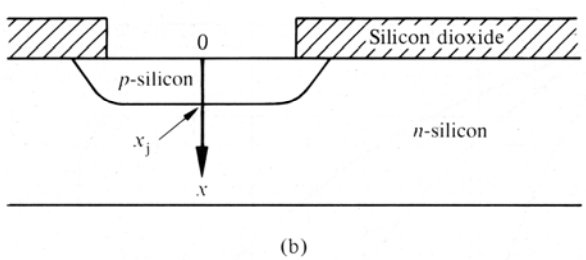


Fig. 1.3 (b) *x*-coordinate axis for impurities.

Potential Energy and Band Bending

- Energy band diagrams show change in E with position
- Electric fields in some areas my "bend" the bands
- Potential Energy (PE) shown by this
  relative to reference energy E_{ref}
- Change in partical position changes PE to Kinetic Energy

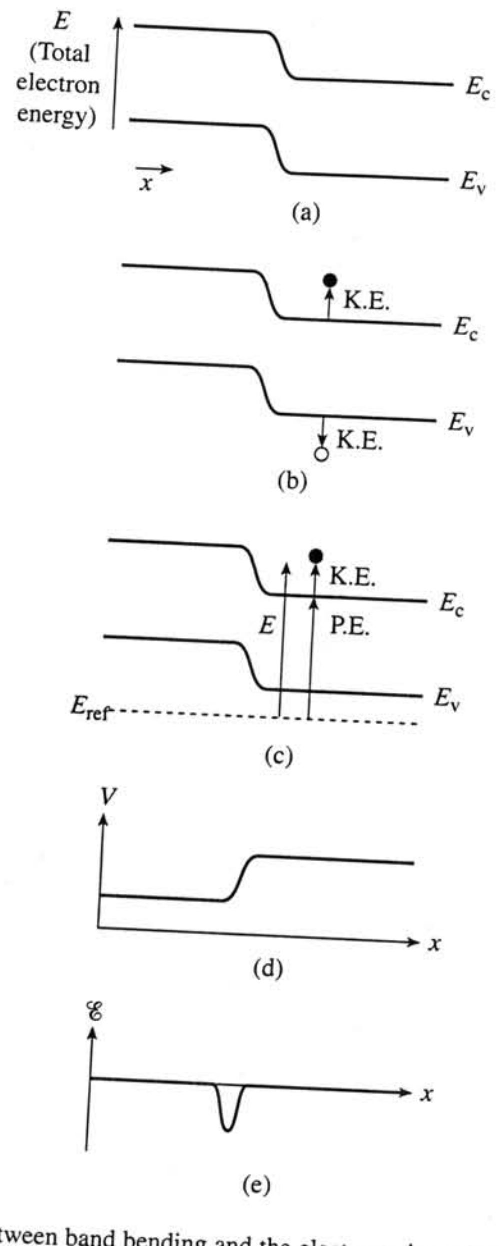


Figure 3.10 Relationship between band bending and the electrostatic variables inside a semiconductor: (a) sample energy band diagram exhibiting band bending; (b) identification of the carrier kinetic energies; (c) specification of the electron potential energy; (d) electrostatic potential and (e) electric field versus position dependence deduced from and associated with the part (a) energy band diagram.

PE and Voltages

- Related PE to the electrostatic potential (V) by

$$PE = -qV = E_c - E_{ref}$$

$$V = -\frac{(E_c - E_{ref})}{q}$$

- Definition V related to the Electric field by the gradient

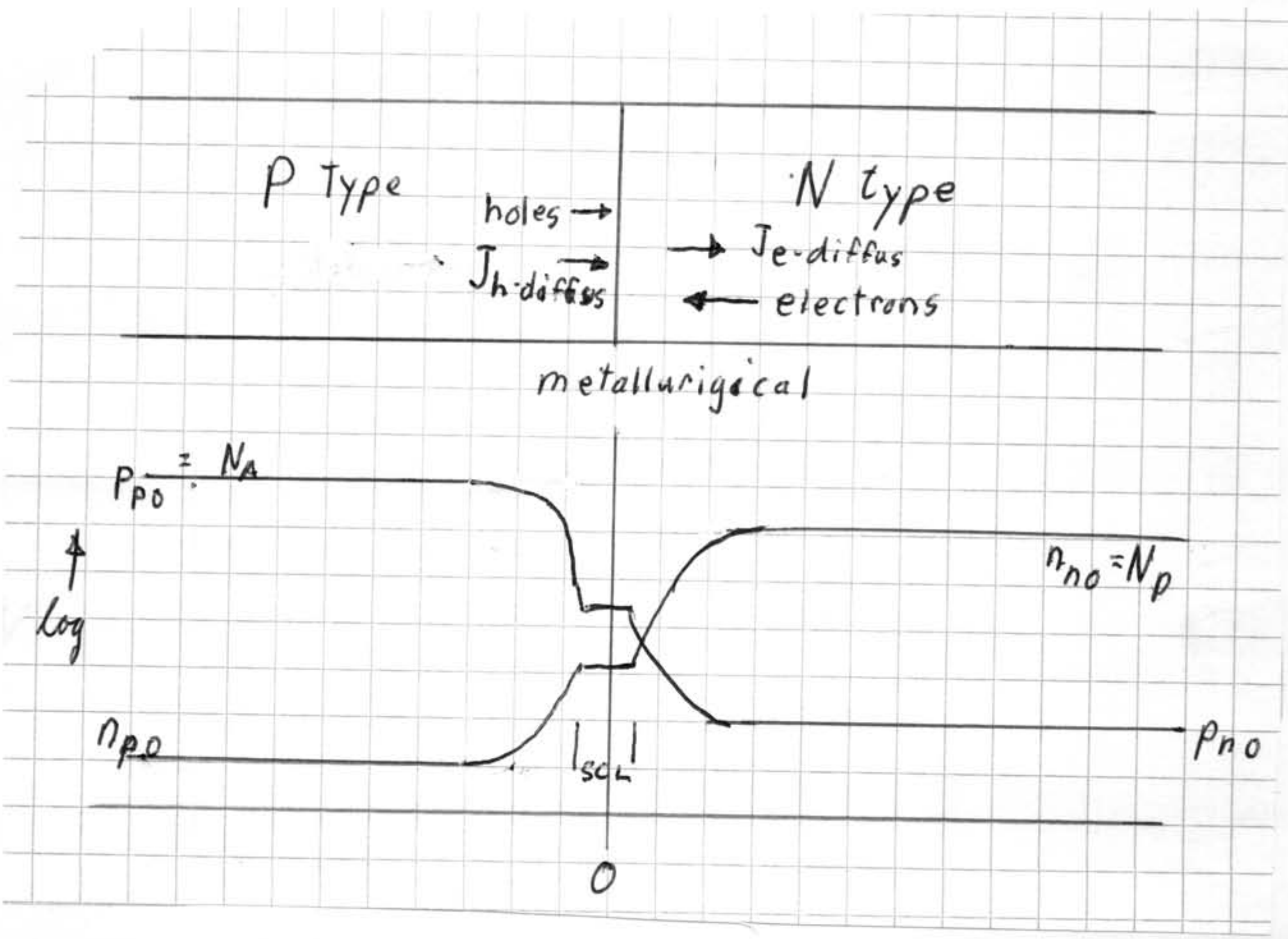
$$\vec{E} = -\nabla V$$

- Thus

$$\vec{E} = \frac{1}{q}\frac{dE_c}{dx}$$

PN Junction Diode

- For an abrupt junction
- (a) initially diffusion forces: cause holes near junction to diffuse from the P material to the N type,
- while electrons diffuse from the N type to the P.
- depletes the carriers in junction area,
- called the "depletion region" or the "Space Charge Layer"
- (b) injected excess minority carriers from the diffusion current (hole in the N type, electrons in the P type)
- minority carrier decays due to the recombination lifetime
- (c) diffusion leaves neg ion cores in P type near junction, positive ion cores in the N type.
- ions create an E field which balances out the diffusion forces.
- E field is a reflection of the difference in the Fermi Energy levels between the P and N.



E field in the PN junction

- Build up of charge can be related to E field by

$$\vec{E} = \frac{1}{\varepsilon_r \varepsilon_0} \int_{-\infty}^{x} \rho(x)\,dx \;\; V/m$$

- where ε_0 = permitivity of free space = $8.854\text{x}10^{-14}$
- ε_r is the relative dielectric constant

  ε_r = 11.9 for silicon

  (also called ε_s, K_s or K_r in some books) (book uses •

The total charge at any point is

$$\rho = q(p - n + N_D - N_A)$$

PN Charge Density, Carriers & E Field

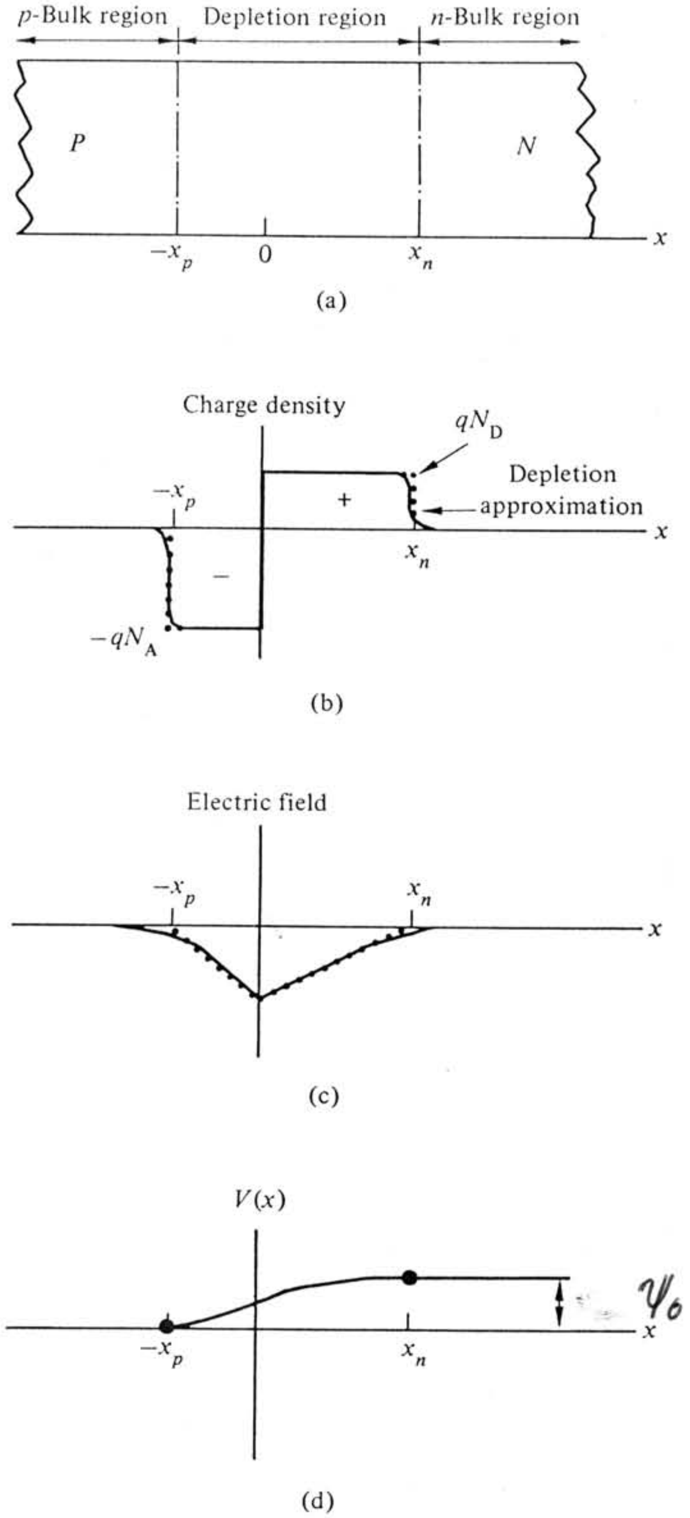


Fig. 2.5 Depletion approximation to the step junction.

The Unbiased diode

- difference in the doping levels generates
  a difference in the Fermi on the P and N region.

$$E_{FN} - E_i = k_B T \ln\left(\frac{n_n}{n_i}\right)$$

$$E_i - E_{FP} = k_B T \ln\left(\frac{p_p}{n_i}\right)$$

- unbiased condition Fermi energy must be at same potential
  throughout the device,
- thus the potential energy levels must change
  so that the E_{FN} matches the E_{FP}.
- This creates a potential energy barrier called:

$$\psi_0 = \frac{E_{FN} - E_{FP}}{q} = \frac{k_B T}{q} \ln\left(\frac{N_D N_A}{n_i^2}\right)$$

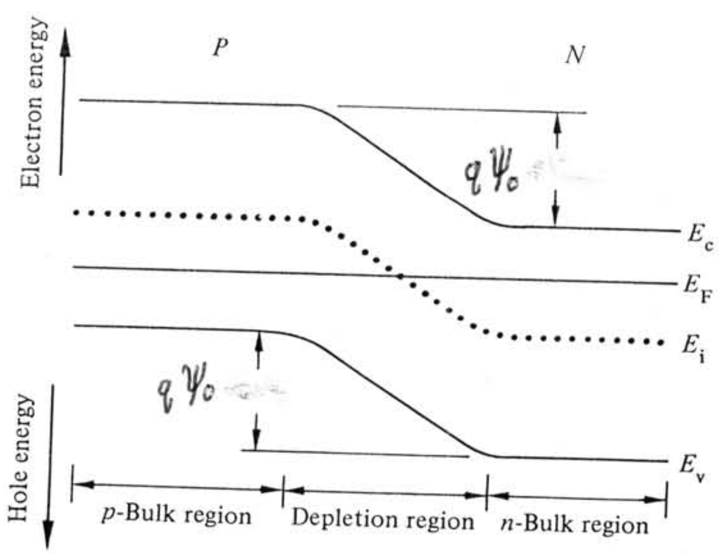


Fig. 2.4 A p-n junction energy band diagram at thermal equilibrium.

Built in Potential Barrier

- Since the minority holes in the N region are

$$p_n = \frac{n_i^2}{N_D}$$

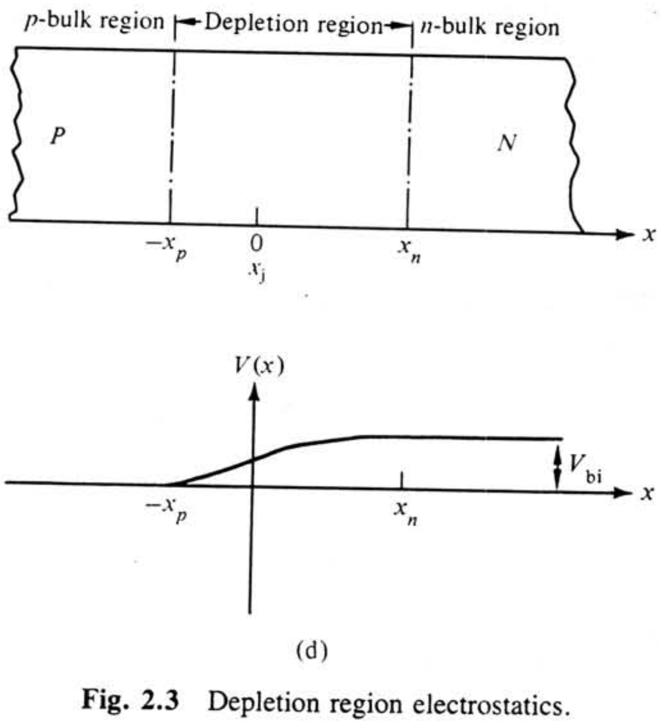
- this gives the "Boltzmann relationship"

$$\psi_0 = \frac{k_B T}{q} \ln\left(\frac{p_{p0}}{p_{n0}}\right)$$

- Similarly for the electrons

$$\psi_0 = \frac{k_B T}{q} \ln\left(\frac{n_{n0}}{n_{p0}}\right)$$

- where the zero subscript on carriers represents the densities well away from the junction.
- Note: book uses V_{bi} for potential; most others use Ψ_0
- This built in potential creates a voltage barrier to the flow of current in the diode.



(d)

Fig. 2.3 Depletion region electrostatics.

Example of Potential Barrier

- Example: For $N_D = 10^{15}$ and $N_A = 10^{14}$ what is the potential barrier height at 300 K in silicon

$$\psi_0 = 0.0259 \ln\left(\frac{10^{15}10^{14}}{[1.5X10^{10}]^2}\right) = 0.52\ V$$

- This represents the voltage barrier that must be overcome before the diode can be "turned on".
- Thus the Fermi energies appear as the fundamental characteristic of operation of the PN diode.

Depletion Approximation

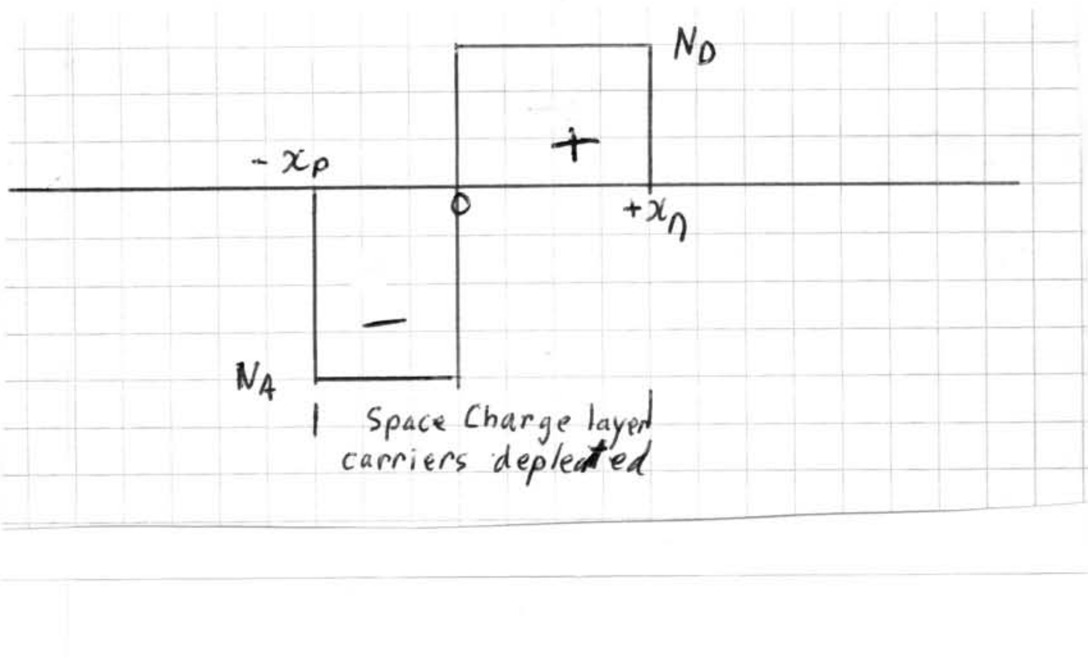
- diffusion of carriers sweeps the charges out of "Space Charge Layer" (SCL)
- making a depleted region.
- approximation is made that since there are few carriers there is no recombination in the Space Charge Layer.
- Thus only the ionic cores are present
- SCL extends from $-x_p$ to x_n
- Assume dopant level much greater than intrinsic level
- (a) Thus on P side

$$N_A > n_p \quad \rho = -qN_A \quad -x_p \le x \le 0$$

- (b) Thus on N side

$$N_D > p_n \quad \rho = qN_D \quad 0 \le x \le -x_n$$

- (c) Charge density is zero in bulk (outside SCL)



E field in the Space Charge Layer

- the requirement that net charge be the same on either side junctions requires:

$$qx_pN_A = qx_nN_D$$

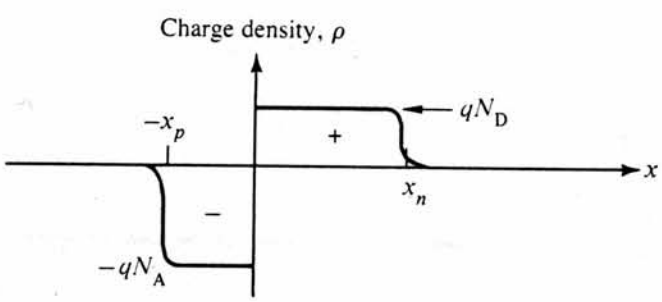
- Which reduces to the important depletion relationship

$$x_pN_A = x_nN_D$$

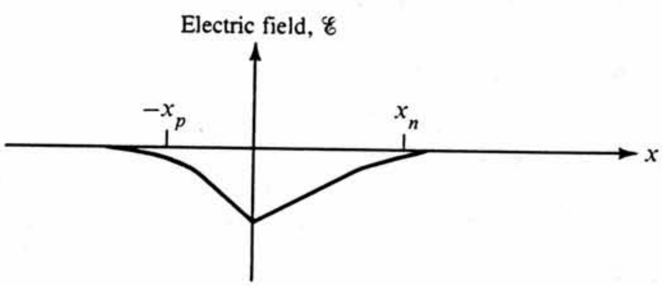
- E field created by charges can be though of as the field between the two charged parallel plates of a capacitor
- then for the space charge layer the E field is linear:

$$E(x) = \frac{Q}{A\varepsilon_r\varepsilon_0} = \frac{qN_A}{\varepsilon_r\varepsilon_0}(x - x_p) = \frac{qN_D}{\varepsilon_r\varepsilon_0}(x + x_n)$$

- where A = the area of the junction
  ε_0 = permittivity of free space = 8.85×10^{-14} F/cm
  ε_r is the relative dielectric constant



(b)



(c)

Width of E field in the Space Charge Layer

- For points within the space charge layer since the potential (voltage) across the junction is given by

$$\psi_0 = \int_{-x_p}^{0} E(x)\, dx + \int_{0}^{x_n} E(x)\, dx$$

- Since

$$E(x) = \frac{qN_A}{\varepsilon_r \varepsilon_0}(x - x_p) = \frac{qN_D}{\varepsilon_r \varepsilon_0}(x + x_n)$$

- Hence

$$\psi_0 = \frac{qN_A x_p^2}{2\varepsilon_r \varepsilon_0} + \frac{qN_D x_n^2}{2\varepsilon_r \varepsilon_0}$$

- Substituting in the charge balance

$$x_p = x_n \frac{N_D}{N_A}$$

$$\psi_0 = \frac{qN_D^2 x_n^2}{2\varepsilon_r \varepsilon_0 N_A} + \frac{qN_D x_n^2}{2\varepsilon_r \varepsilon_0}$$

- Solving for the N side width

$$x_n = \left[\frac{2\varepsilon_r \varepsilon_0 \psi_0}{q} \left(\frac{N_A}{N_D(N_A + N_D)} \right) \right]^{\frac{1}{2}}$$

Width of the Space Charge Layer

- Solving for the P side width by subsititution

$$x_n = \left[\frac{2\varepsilon_r \varepsilon_0 \psi_0}{q} \left(\frac{N_D}{N_A(N_A + N_D)} \right) \right]^{\frac{1}{2}}$$

- Then let the width of the space charge layer be W_{scl}

$$W_{scl} = x_p + x_n$$

and solve for

$$W_{scl} = x_p + x_n = \left[\frac{2\varepsilon_r \varepsilon_0 \psi_0}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{\frac{1}{2}}$$

- Note the charges separated by a distance creates an effective capacitance
- C varies with the dopant level and junction width.

Example Width of Space Charge Layer

- Example: for $N_A = 10^{15}$ and $N_D = 10^{14}$ cm^{-3}
- then find the width of the space charge layer.
- As before

$$\psi_0 = 0.0259 \ln\left(\frac{10^{15}10^{14}}{[1.5X10^{10}]^2}\right) = 0.52\ V$$

- Then the widths are

$$x_n = \left[\frac{2\varepsilon_r\varepsilon_0\psi_0}{q}\left(\frac{N_D}{N_A(N_A+N_D)}\right)\right]^{\frac{1}{2}}$$

$$x_n = \left[\frac{2\ 11.8\ 8.85X10^{-14}\ 0.52}{1.6X10^{-19}}\left\{\frac{10^{15}}{10^{14}(10^{15}+10^{14})}\right)\right]^{\frac{1}{2}} = 2.5X10^{-4}\ cm$$

$$x_n = 2.5 microns$$

$$x_p = x_n \frac{N_D}{N_A} = 2.5x10^{-4}\ \frac{10^{14}}{10_{15}}\ 0.25 microns$$

$$W_{scl} = \left[\frac{2\ 11.8\ 8.85X10^{-14}\ 0.52}{1.6X10^{-19}}\left\{\frac{10^{15}+10^{14}}{10^{15}10^{14}}\right)\right]^{\frac{1}{2}} = 2.7X10^{-4}\ cm$$

$$W_{scl} = \ = 2.7 microns$$

Voltage within Space Charge Layer

- For points within the space charge layer, since the potential (voltage) across the junction is given by

$$\psi_0 = \int_{-x_p}^{0} E\,dx + \int_{0}^{x_n} E\,dx = \frac{qN_A x_p^2}{2\varepsilon_r\varepsilon_0} + \frac{qN_D x_n^2}{2\varepsilon_r\varepsilon_0}$$

- Let the width of the space charge layer be W_{scl}. Since

$$x_p = \left[\frac{N_D}{N_A}\right] x_n$$

- Thus substituting into the potential equation gives

$$W_{scl} = x_p + x_n = x_n\left[1 + \frac{N_D}{N_A}\right] = \left[\frac{2\varepsilon_r\varepsilon_0\psi_0}{q}\left(\frac{N_A + N_D}{N_A N_D}\right)\right]^{\frac{1}{2}}$$

- Note the existence of such charges separated by a distance creates an effective capacitance
- C varies with the dopant level and junction width.

Example of E field within the junction

- Example: for $N_A = 10^{15}$ and $N_D = 10^{14}$ cm^{-3} then

(a) find the width of the space charge layer.

(b) calculate the electric field at the junction

- (a) As before

$$\psi_0 = 0.0259 \ln\left(\frac{10^{15}10^{14}}{1.5X10^{10}}\right) = 0.52\ V$$

$$W_{scl} = \left[\frac{11.8\ 8.85X10^{-14}\ 0.52}{1.6X10^{-19}}\left\{\frac{10^{15}+10^{14}}{10^{15}10^{14}}\right)\right]^{\frac{1}{2}} = 2.73X10^{-4}\ cm = 2.7\ \mu m$$

- (b) At the junction (x = 0) then

$$x_n = \frac{W_{scl}}{[1+\frac{N_D}{N_A}]} = \frac{2.73X10^{-4}}{[1+\frac{10^{14}}{10^{15}}]} = 2.48X10^{-4}\ cm$$

$$E(0) = \frac{qN_D}{\varepsilon_r\varepsilon_0}(x_n) = \frac{1.6X10^{-19}\ 10^{14}}{1.05X10^{-12}}\ 1.7X10^{-4} = 3.79X10^{3}\ V/_{cm}$$

- The electric field is strong in the junction.

Currents in the unbiased PN diode

- There must be no current flowing without an applied voltage.
- Thus currents must balance in each region.
- The junction electric field creates a drift field of holes and electrons that exactly compensates the diffusion current.
- Thus in both regions:

$$J_{drift} = -J_{diff} \quad but \quad J_{drift} \neq 0$$

- In the Energy diagram electrons in N type conduction band above P type conduction band have no barrier to overcome
- These can move across the depletion region.
- Holes in P type valance band below the N type valance band have no barrier to overcome
- move across the depletion region.
- These are the energy states that drift and diffuse across the barriers.

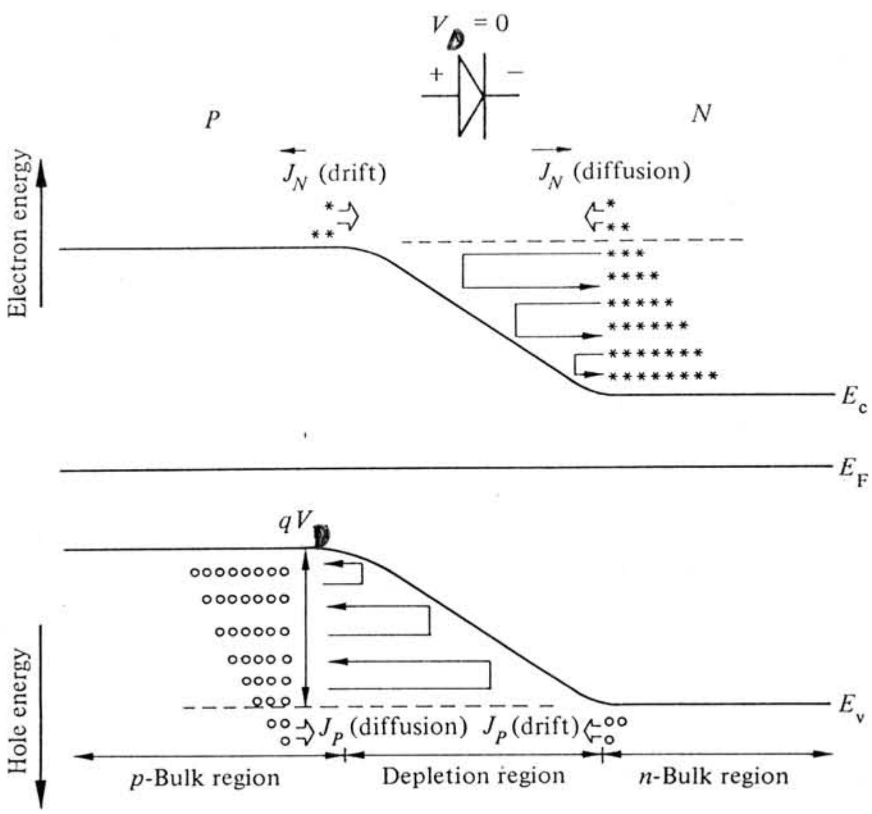


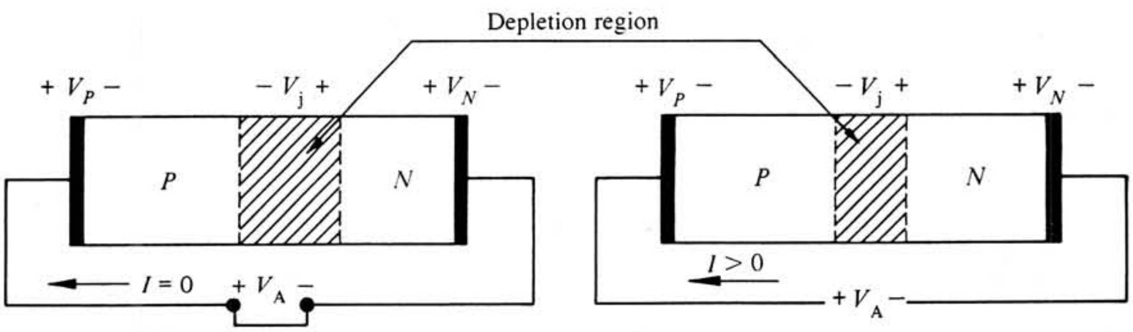
Fig. 3.1 Thermal equilibrium energy band diagram.

Applying bias to the PN junction

- When you apply a voltage V_A to the diode
- Voltage across Space Charge Layer different
- First there is contact potentials at metal contacts
- V_N on N side, V_P on P side
- When no voltage applied (no current flows)

$$\psi = V_D = V_N + V_P$$

where V_D = applied junction voltage (Book uses V_j)



(a) Thermal equilibrium $V_j = V_{bi}$

(b) Forward bias $V_A > 0$, $V_j = V_{bi} - V_A$

Fig. 2.6 Junction potential: (a) thermal equilibrium, $V_j = V_{bi}$; (b) forward bias $V_A > 0$, $V_j = V_{bi} - V_A$.

Applying bias to the PN junction

- If current flows there is resistive losses in diode as well

$$V_D = V_N + V_P - V_A + I(R_N + R_P$$

- The effective potential at the junction is

$$\psi = \psi_0 - V_D$$

- As the diode is forward biased, the potential barrier shrinks
- as it is reversed biased the barrier grows larger.

Applied Bias and SCL Width in PN junction

- From the Possion solution to the junction width
  can just substitute the new potential into the junction
- the widths and potentials of the space charge layer to be:
- Thus on the p side

$$-x_p \le x \le 0$$

$$x_p = \left[\frac{2\varepsilon_r\varepsilon_0(\psi_0 - V_D)}{q}\left(\frac{N_D}{N_A(N_A + N_D)}\right)\right]^{\frac{1}{2}}$$

$$V(x) = \frac{qN_A}{2\varepsilon_r\varepsilon_0}(x_p + x)^2$$

$$E(x) = -\frac{qN_A}{\varepsilon_r\varepsilon_0}(x + x_p)$$

Applied Bias and SCL Width in PN junction

- On the N side of the SCL

$$0 \le x \le x_n$$

$$x_n = \left[\frac{2\varepsilon_r \varepsilon_0 (psi_0 - V_D)}{q} \left(\frac{N_A}{N_D(N_A + N_D)} \right) \right]^{\frac{1}{2}}$$

$$V(x) = (\psi_0 - V_D) - \frac{qN_A}{2\varepsilon_r \varepsilon_0}(x_n - x)^2$$

$$E(x) = \frac{qN_D}{\varepsilon_r \varepsilon_0}\left(x_n - x\right)$$

- The combined SCL width changes as

$$W_{scl} = \left[\frac{2\varepsilon_r \varepsilon_0 (\psi_0 - V_D)}{q} \left(\frac{N_A + N_D}{N_A N_D} \right) \right]^{\frac{1}{2}}$$

- as forward bias applied: space charge layer becomes smaller,
- while as the reverse is applied it becomes larger.
- thus capacitance of diode changes with the applied bias, decreasing with reverse bias.

Real Changes in Junction width for applied Voltages

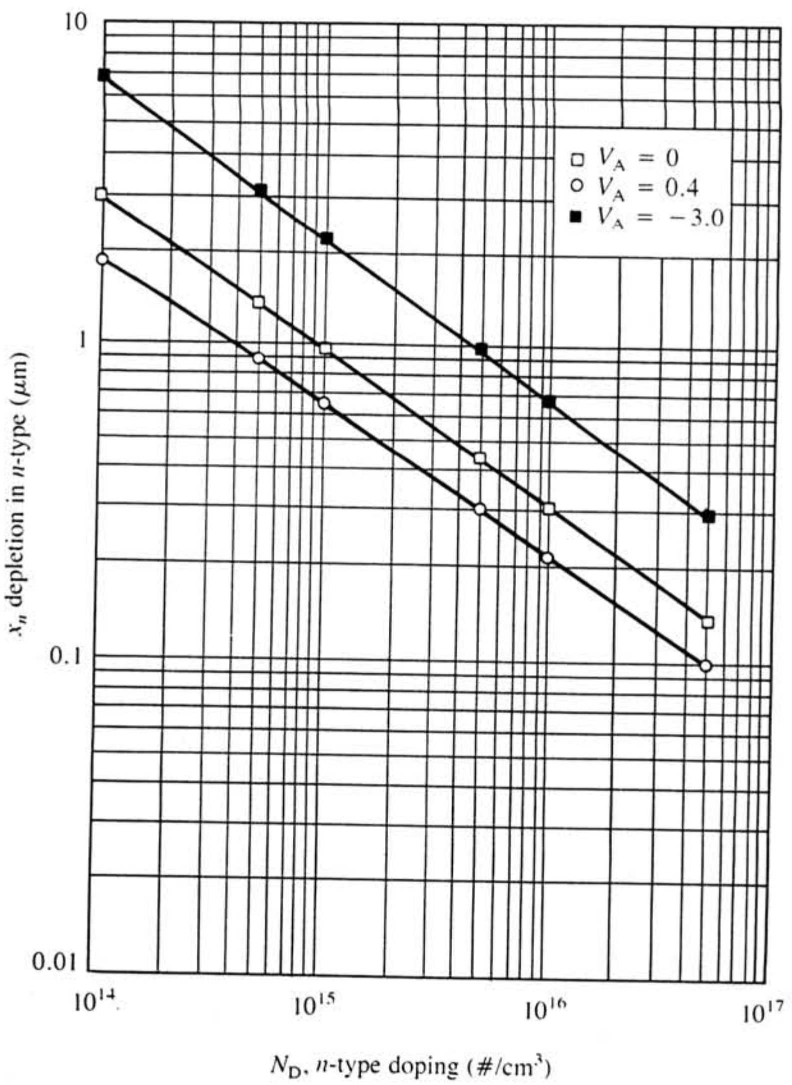


Fig. 2.9 n-depletion region for V_A = 0, 0.4, and −3.0 volts.

Forward Applied Bias and PN junction

- When $V_D > 0$ and $V_D < \psi_0$
- SCL width is reduced on both sides
- E field is reduced by the added potential
- Potential barrier height is reduced
- Thus easier for carriers to move across

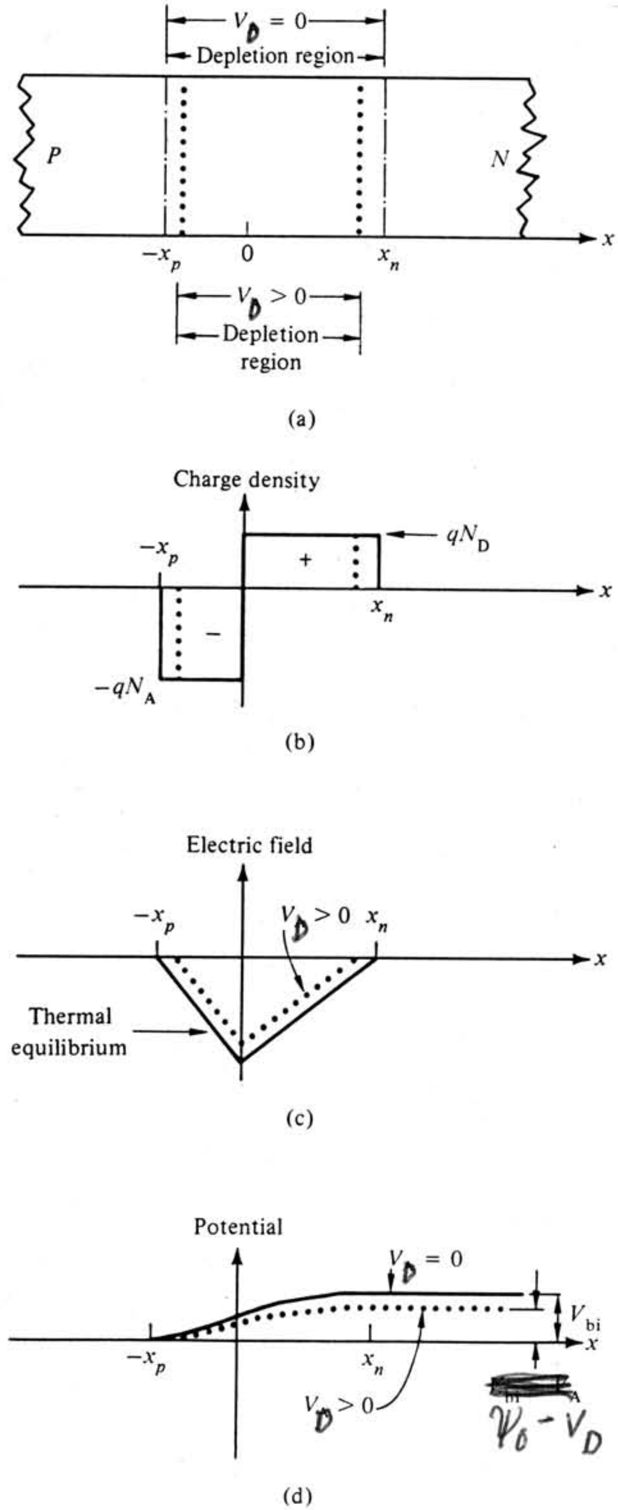


Fig. 2.7 Effect of forward bias on the diode electrostatics ($V_D > 0$, dotted lines; $V_D = 0$, unbroken lines).

Reverse Applied Bias and PN junction

- When $V_D < 0$
- SCL width is increased on both sides
- E field is increased by the added potential
- Potential barrier height is heighened
- Thus harder for carriers to move across

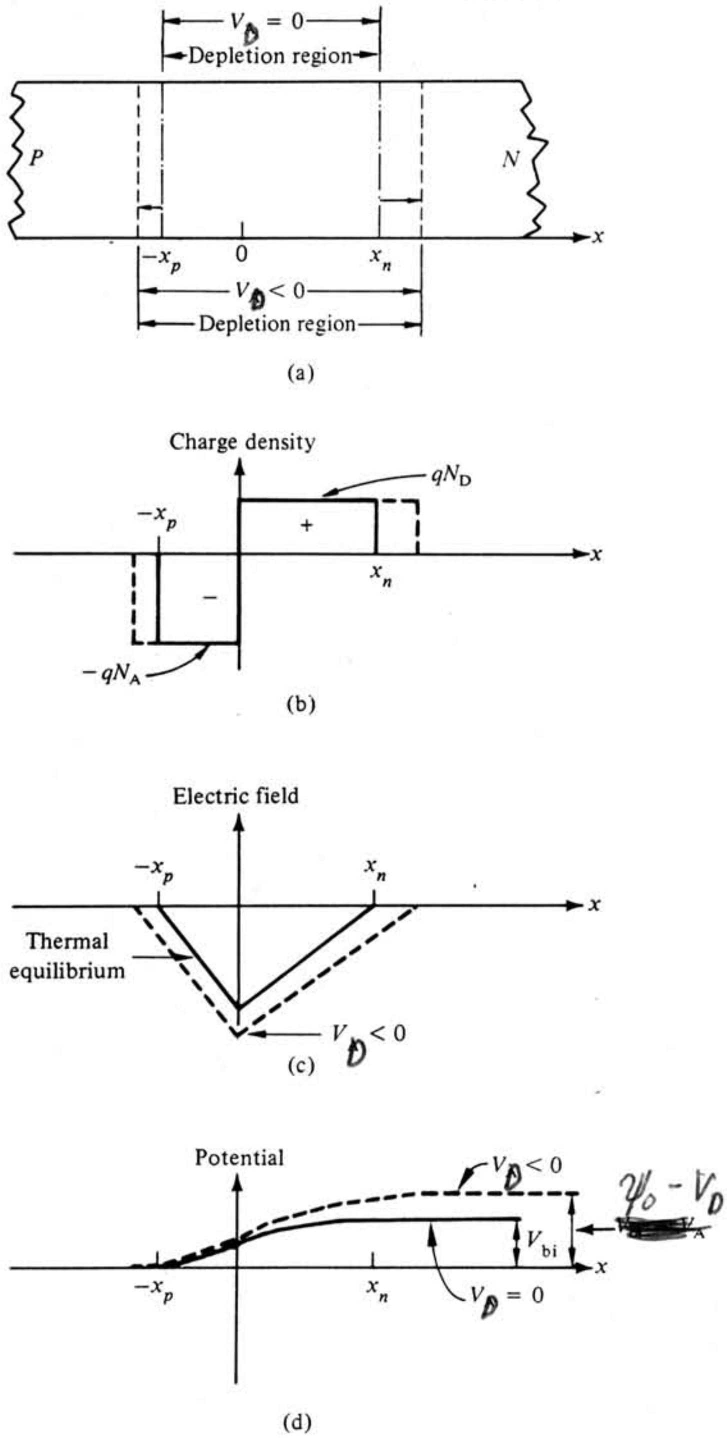


Fig. 2.8 Effect of bias on depletion region electrostatics ($V_D < 0$, dashed lines; $V_D = 0$, unbroken lines).

Applied Bias and PN junction

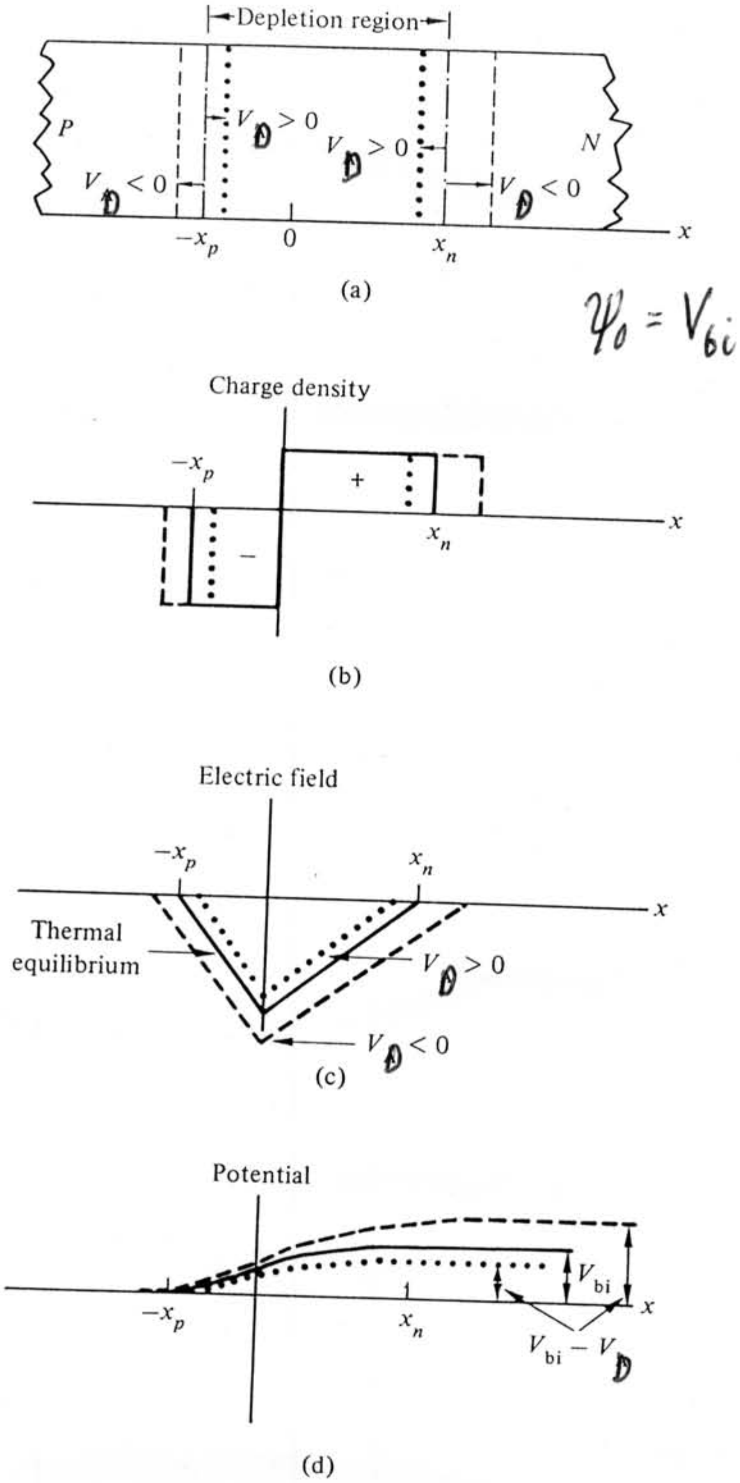


Fig. 2.8 Effect of bias on depletion region electrostatics.

Applied Bias PN Energy Diagrams

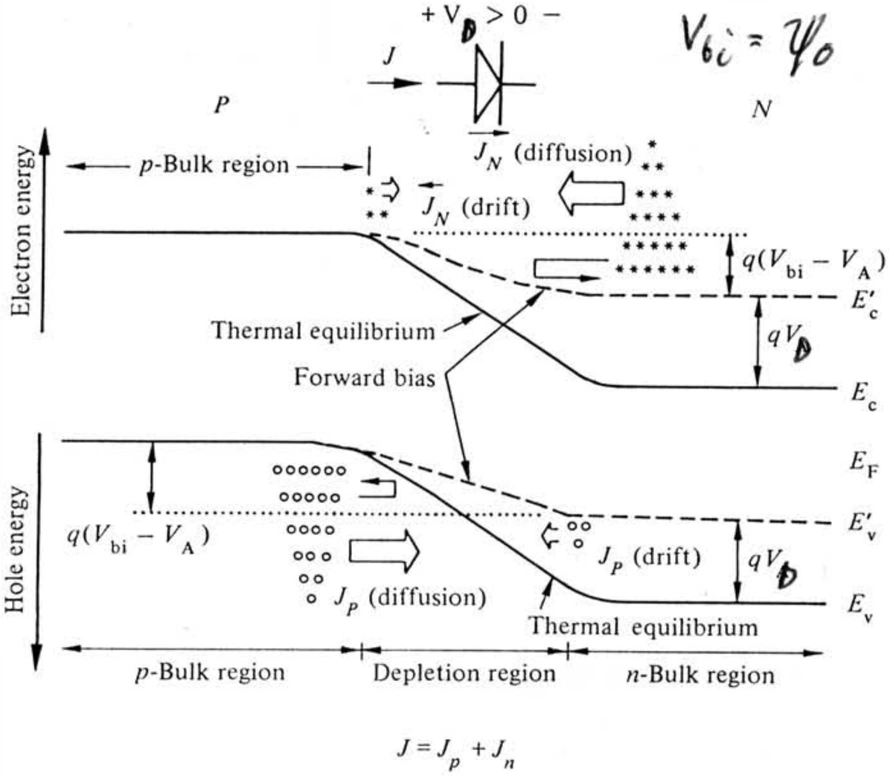


Fig. 3.3 Energy band diagram for forward bias and at thermal equilibrium.

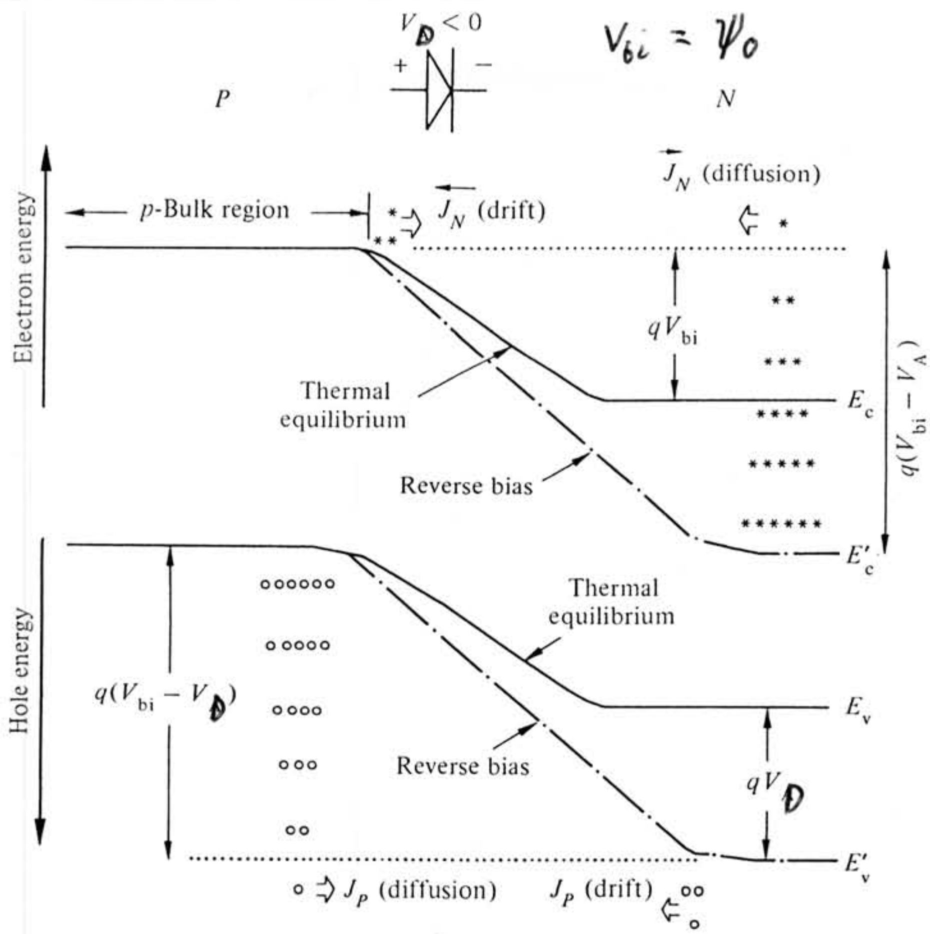
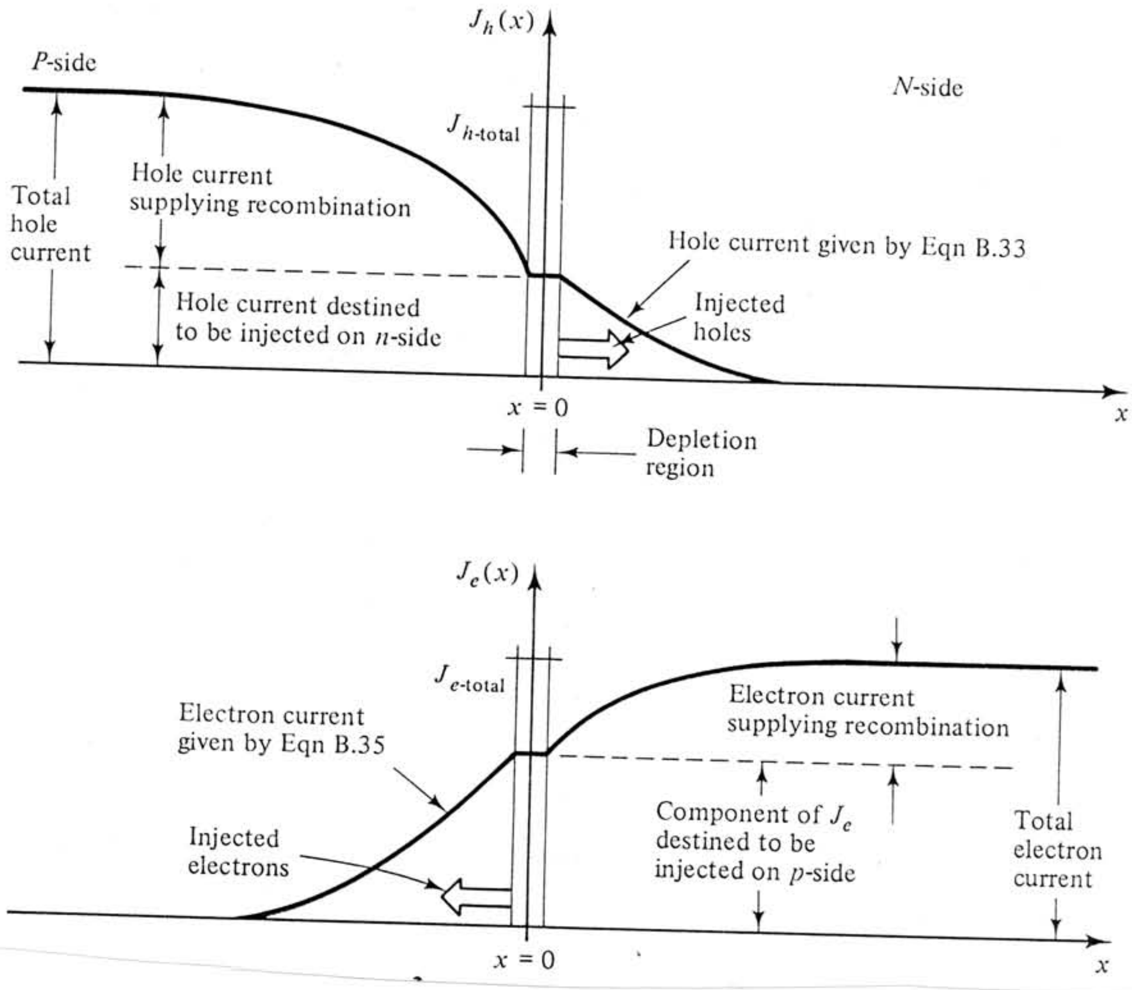


Fig. 3.4 Energy band diagram for reverse bias and at thermal equilibrium.

Applying Forward bias to the PN junction

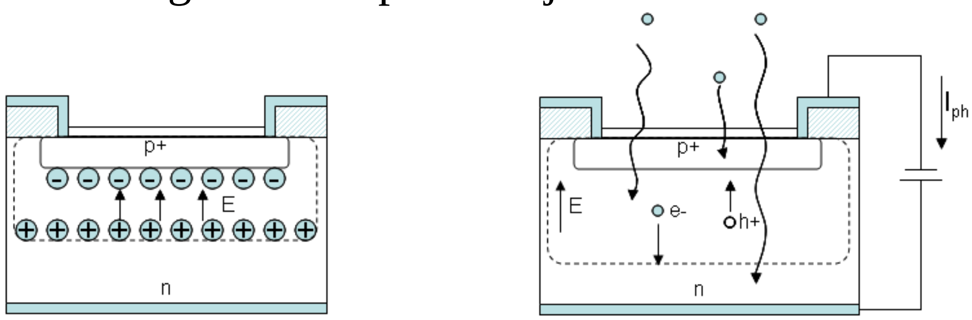
- apply a voltage to the diode: drift current increases
- more holes are carried from P region into the N region,
- where they become minority carriers
- similarly electrons go from major carriers in N region to minority carriers in the P region.
- Thus you are injecting minority carrier into each region.

Figure B.6 Hole and electron current density components in the forward-biased PN junction of Fig. B.4. The total current density is uniform at any position x.



Photodiode and light

- Any large diode is a photodiode
- Light creates electron hole pairs as it is absorbed
- The E field at junction separates the charges
- Holes (p) go in direction of E field
- e’s (n) opposite E field
- Result is charge builds up on the junction



(a) unbiased **(b) reverse biased**

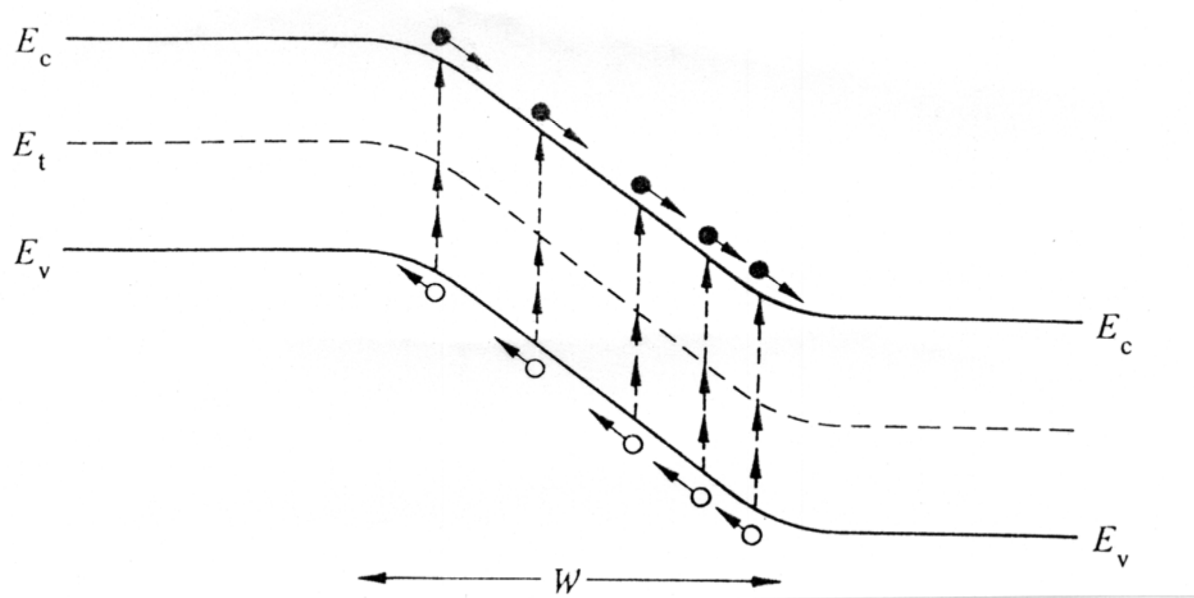
Generation and the Reverse Current

- Previously assumed no generation in the Space Charge Layer
- Within space charge layer the temperature electron-hole pairs
- When reverse biased diode very few carriers in the junction,
- Thus carriers generated within the junction dominate.
- Generated carriers swept out of junction by the electric field
- Holes pulled to the N side and electrons to the P
- There recombine with the majority carriers
- Create an additional current
- Called the "Recombination/Generation current")
- Same recombination behaviour as in bulk
- Generation rate of these carriers is given by:

$$G = \frac{n_i}{2\tau_0}$$

- τ_0 is the effective lifetime
- Average of the electron and hole lifetimes.

$$\tau_0 = \frac{\tau_n + \tau_p}{2}$$



Total Recombination/Generated Current in Junction

- Thus total recombination/generated current in junction is
- Amount generated within the space charge layer
- Times the charge of the carriers q, and the junction area A:

$$I_{RG} = \frac{qAn_i}{2\tau} W_{scl}$$

- Recall as reverse bias is increased
- space charge layer width W_{scl} becomes larger
- Hence recombination/generation current becomes more important.

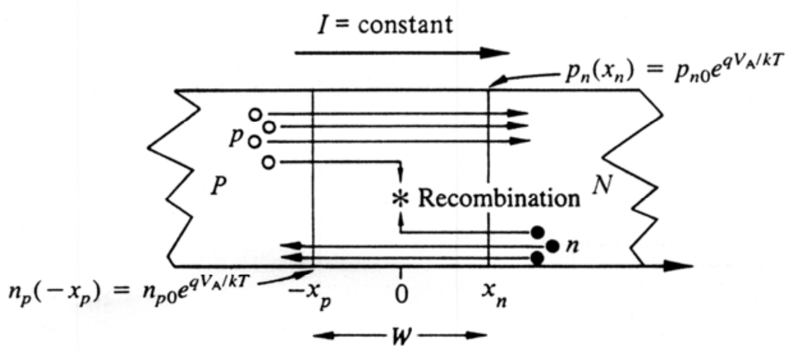


Fig. 4.8 Recombination as an additional current to the ideal diode in the depletion region under forward bias.

Diode Equation with RG

- Diode equation now becomes:

$$I = \left[I_s \, exp\left(\frac{qV_D}{k_B T}\right) + I_{RG} \, exp\left(\frac{qV_D}{2k_B T}\right) - 1 \right]$$

- Forward biased diode the I_{RG} term can often be neglected
- For silicon it is actually the dominate factor at room temperature
- Hence reverse leakage is much higher than expect
- Thus cannot measure reverse current and stick in diode equation
- Note as temperature drops closer to ideal

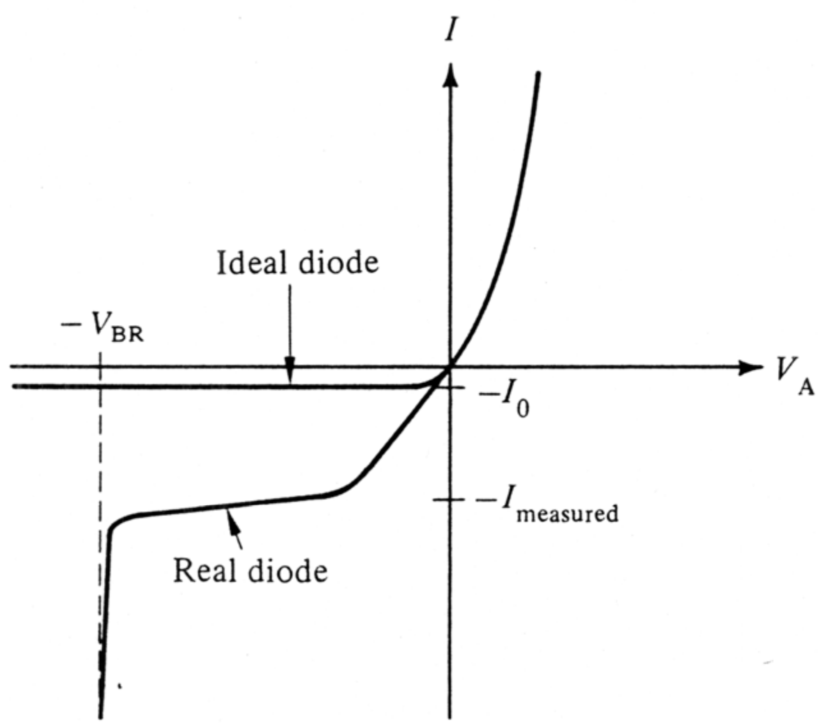


Fig. 4.1 Reverse-biased deviations from ideal.

Forward Bias Deviation from Ideal Diode Equation

In practice in silicon shows some modification from the ideal

$$I = I_s\left[exp\left(\frac{qV_D}{\eta k_B T}\right) - 1\right]$$

Where η is the ideality factor

Measure of how ideal the diode is

For modern silicon η ranges from 1.0 to 1.06 for 5 decades of I

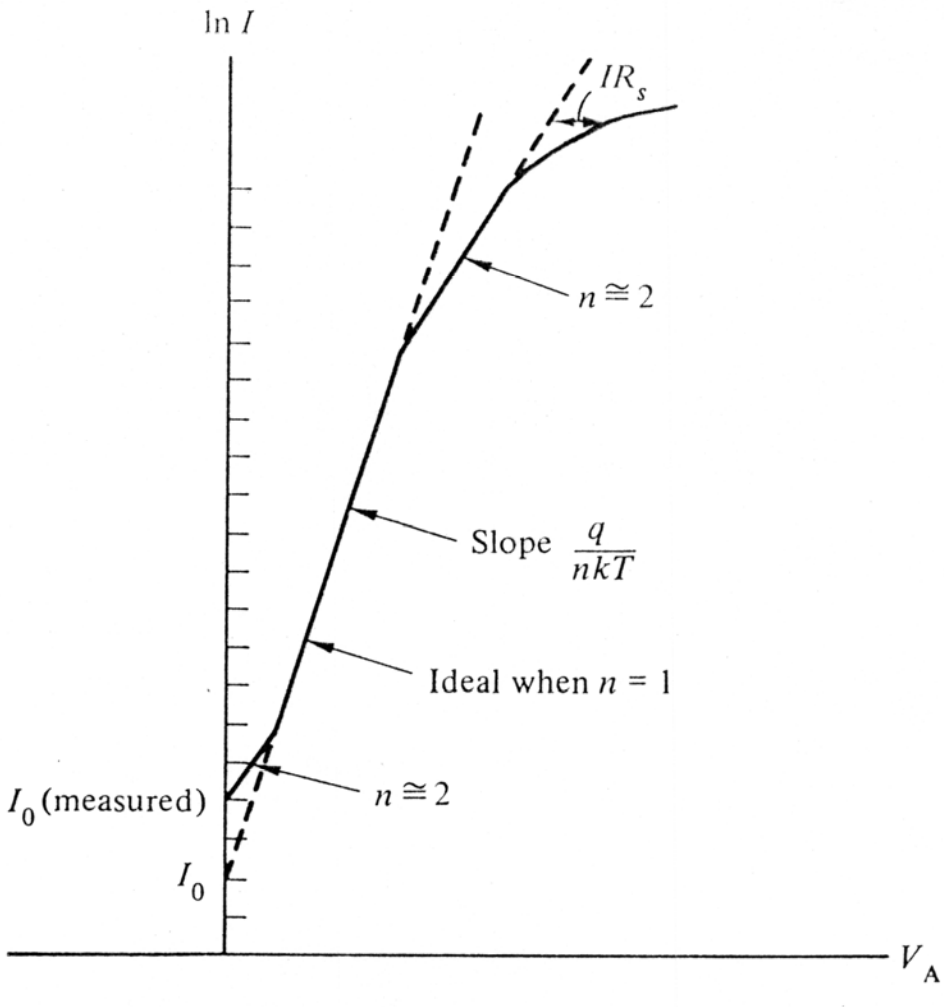


Fig. 4.7 Forward bias deviations from the ideal.