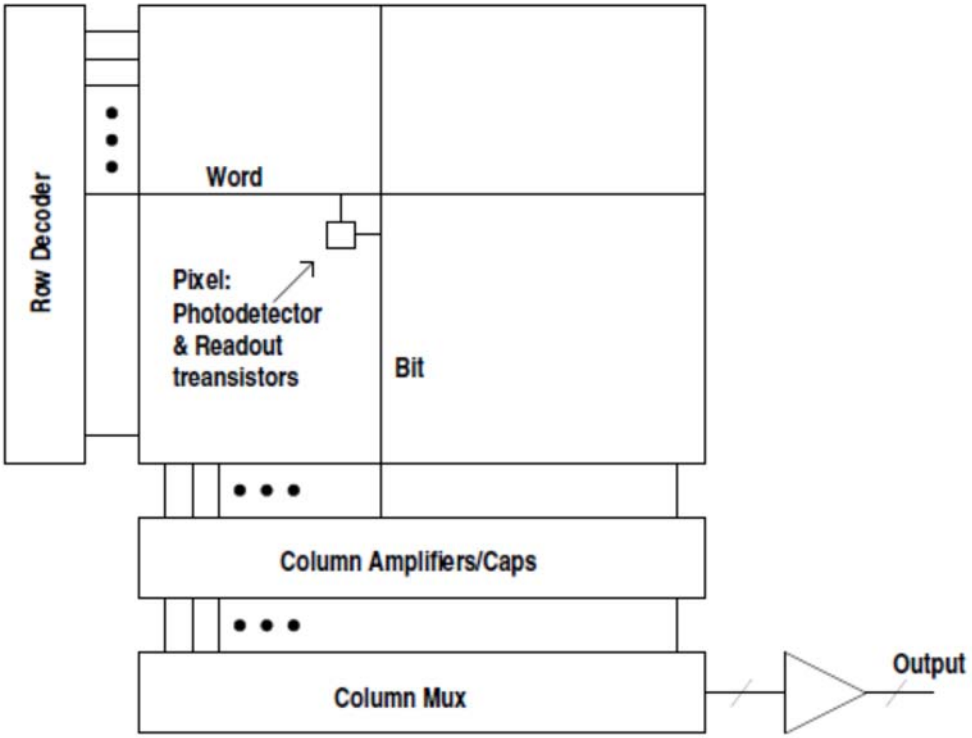
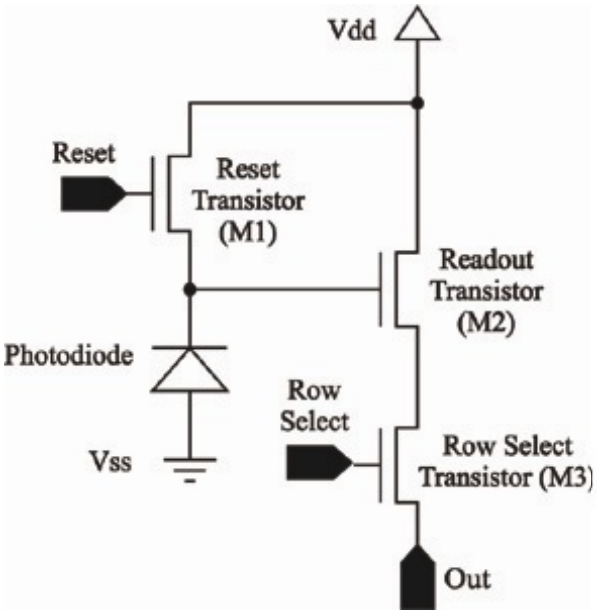
CMOS Imager Architecture

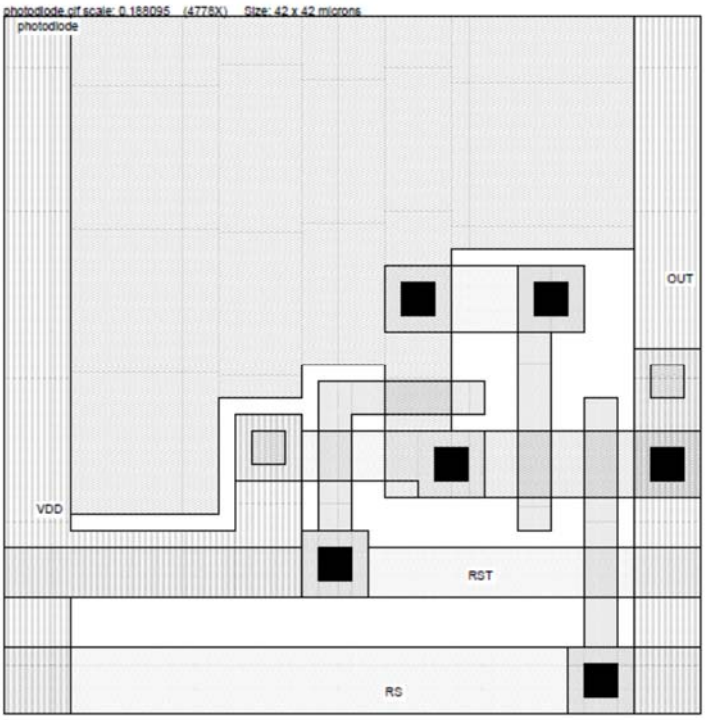
- Now look at pixel within the overall imager
- Architecture is that pixels are addressed by row and column
- Row Decoder selects row of pixels for readout
- Generally all the columns read to col storage Capacitors
- Usually col amplifiers as well
- Then row output in parallel to a Multiplexer
- Then output to A/D converter
- As CMOS all these circuits are on chip
- In CCD as technology different they were on separate chip



Pixel contains the 3T

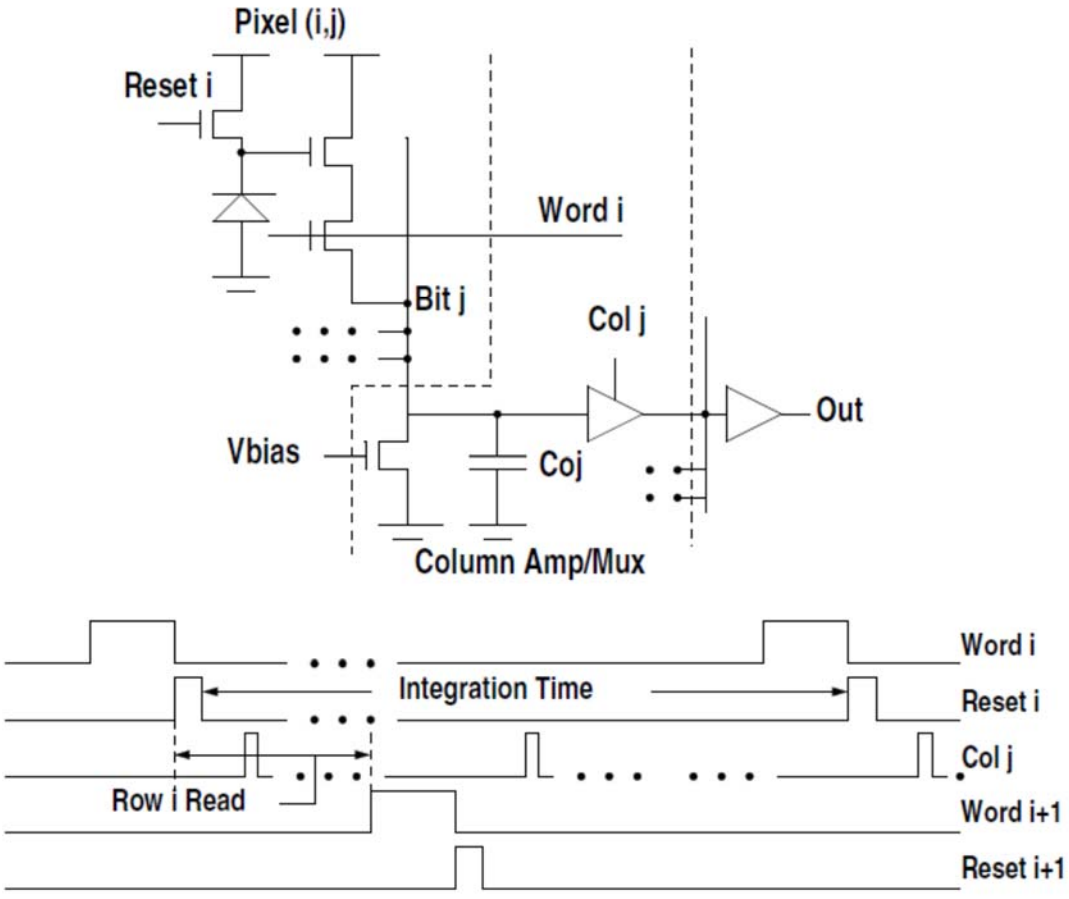
- Typically pixel has transistors close in design
- Want characteristics (eg V_{th} - theshold) close to same
- Thus diode is often not square
- Fill Factor (diode area) is 20%-50%
- Much smaller than CCD





3T Pixel Operation

- Looking beyond the pixel to column
- Output is buffered by readout transistor
- Add a Vbias transistor at bottom of column
- Vbias sets the output voltage
- Output voltage charges the Coj

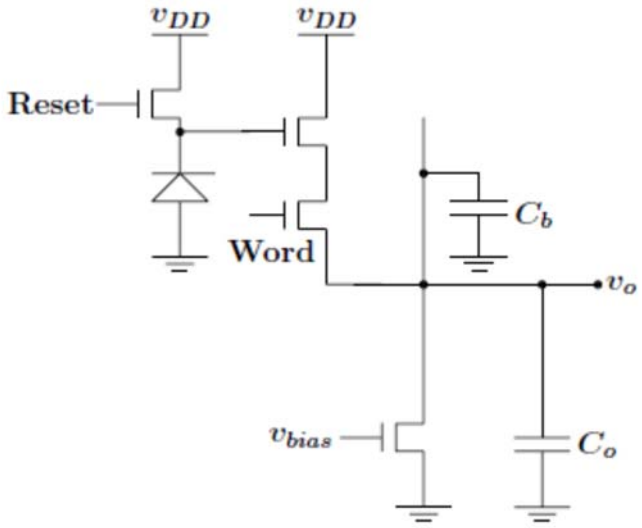


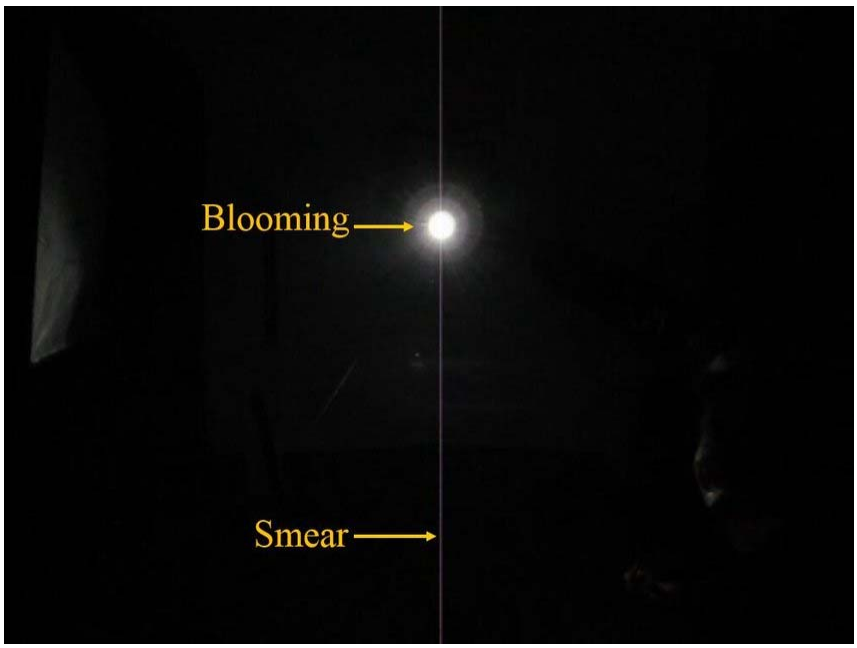
Pixel Operation – Reset implications

- Photodiode & out gate is reset to

$$v_D = v_{DD} - v_{tr}$$

- v_{tr} is the reset transistor threshold voltage
- set $v_{reset} > v_{tr}$ instead of to ground during integration
- This removes pixel blooming
- Blooming is where charge spread to neighboring pixels
- Blooming problem in CCDs at larger exposures
- Almost eliminated in APS





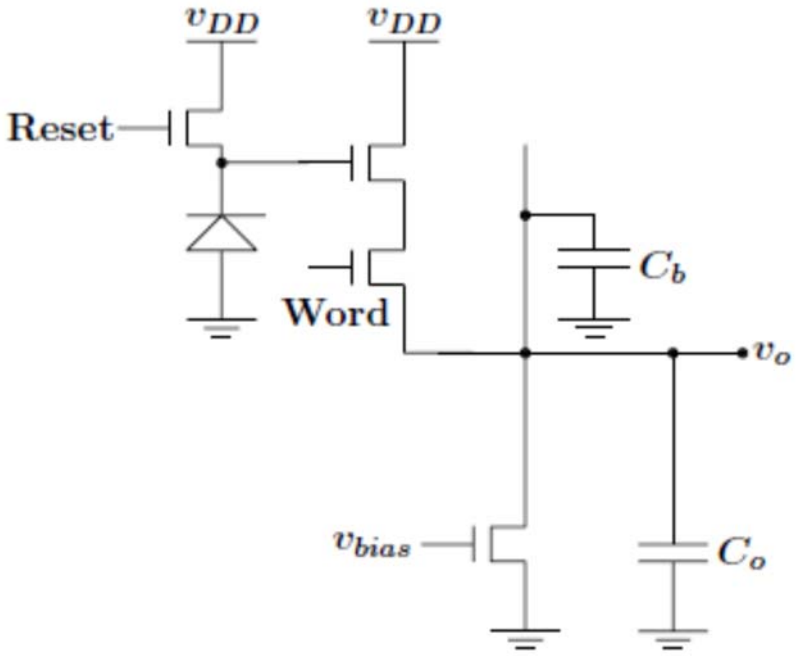
APS Pixel output voltage

- Assume charge Q is left on diode/gate at end of integration
- Let us ignore v drop across word transistor
- The v output v_o is

$$v_o = v_D - \frac{Q}{C_D} - V_{gsf}$$

- v_{gsf} is the follower (amp) transistor gate to source voltage
- Sensor conversion gain is

$$\frac{Q}{C_D}\mu \;\; Volts/electron$$



Pixel Keeping output in saturation

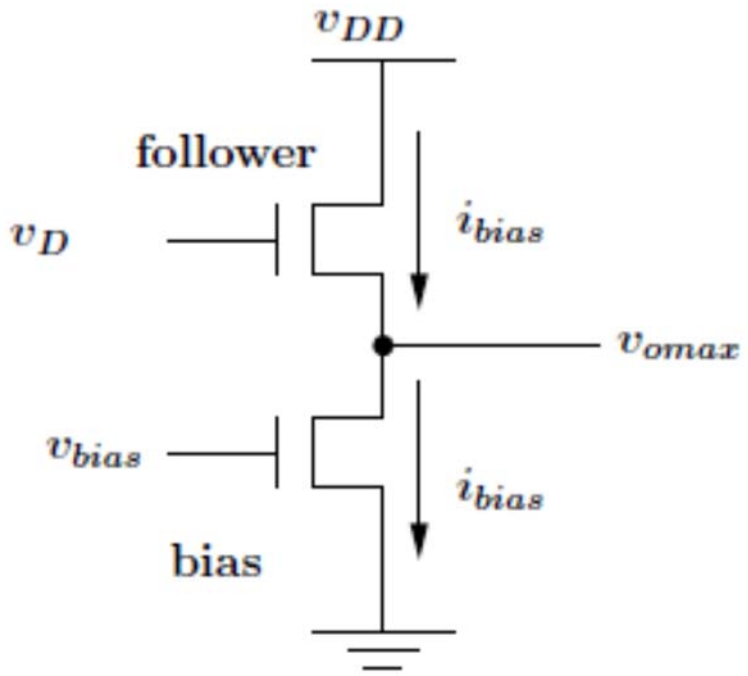
- Want the output bias transistor kept in saturation

$$v_{o-min} = v_{bias} - v_{trB}$$

- Where v_{trB} is the bias transistor threshold
- Max output occurs when Q=0

$$v_{o-max} = v_{DD} - v_{tr} - v_{gsf}$$

- Let i_{bias} be col amplifier bias current



Follower transistor gate to source voltage

- Assume static MOS transistor model
- Follower transistor has gate width W_F and length L_F
- Then bias current is

$$i_{bias} = \frac{k_n}{2}\frac{W_F}{L_F}\left(v_{gsf} - v_{tr}\right)^2$$

- Thus rewriting get

$$v_{gsf} = v_{tr} + \sqrt{\frac{2L_F}{k_n V_F}}$$

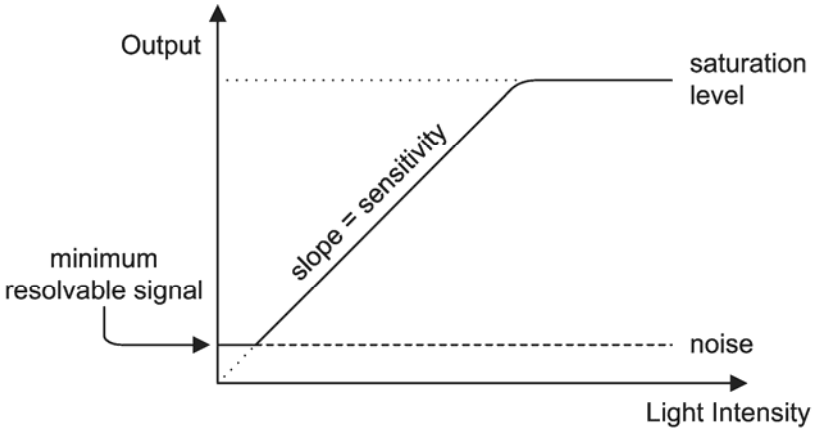
- Thus voltage swing is

$$v_s = v_{DD} - v_{tr} - v_{gsf} - v_{bias\_}v_{trB}$$

- Available well capacity

$$Q_{max} = v_D x C_D$$

- Cannot be obtained as $v_{o\text{-}min}$ is not at ground
- Out is somewhat nonlinear



Why APS sensitivity does not scale with Area

- Charge collect depend on number of photons

$$Q = I * T * A$$

- Where I is the light intensity in w/cm^2 & T the exposure Time
- A is the photodiode area
- But C of diode is proportional to the area A
- For a parallel plate C with area A and distance d between the plates

$$C = \epsilon \frac{A}{d}$$

- Since the pixel output voltage is

$$v_o = v_D - \frac{Q}{C_D} - V_{gsf}$$

- Since

$$\frac{Q}{C_D} = \frac{I * T * A}{\frac{\epsilon A}{d}} = \frac{I * T * d}{\epsilon}$$

- Thus APS pixel sensitivity depends only on light gathered
- Same as two different sized tubes in the rain
- Water level stays the same
- Common error among both photographers and researchers