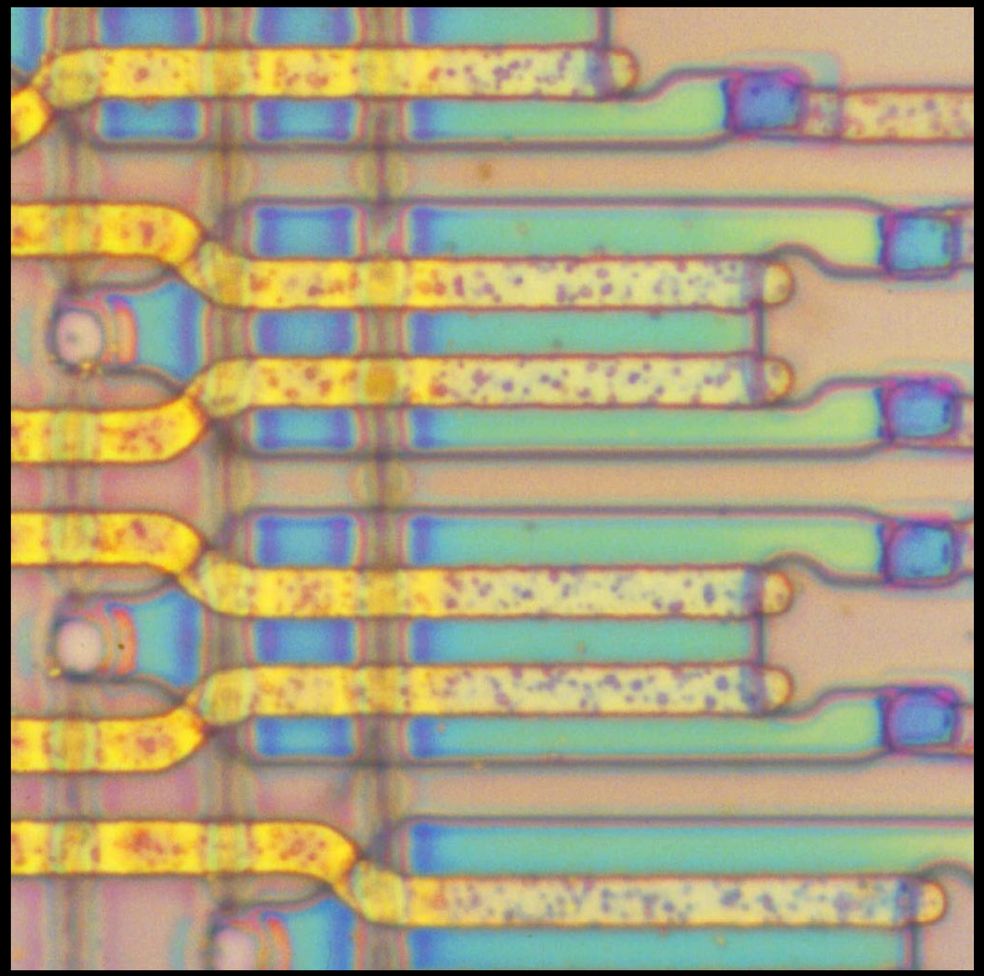


Traveling Inside a Chip

Ricardo Reis

UFRGS

a trend without return

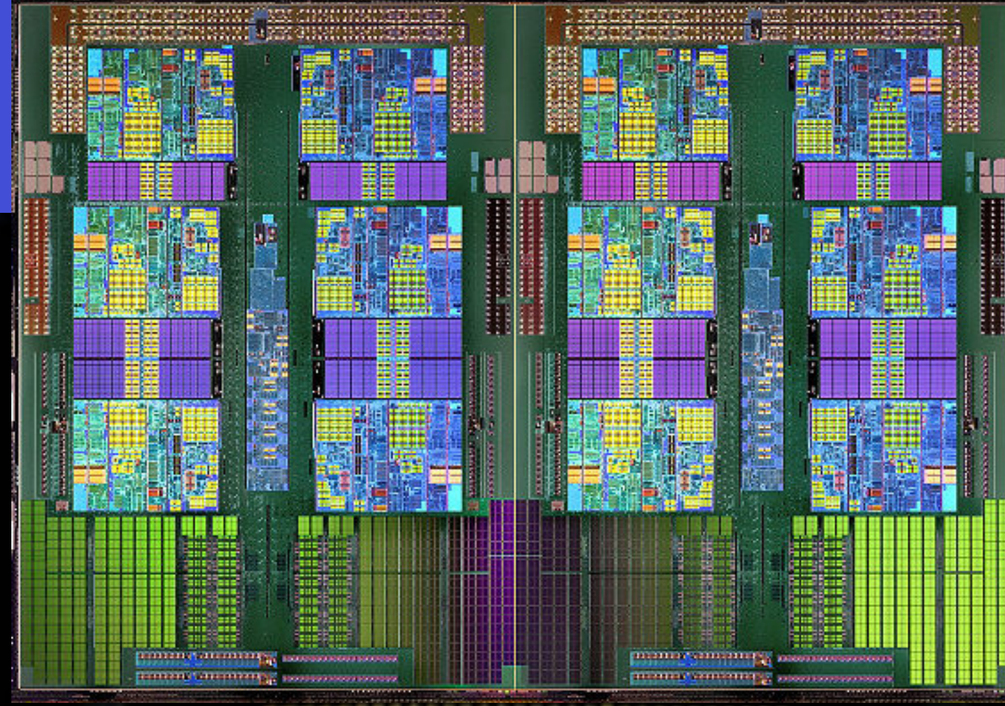
more & more

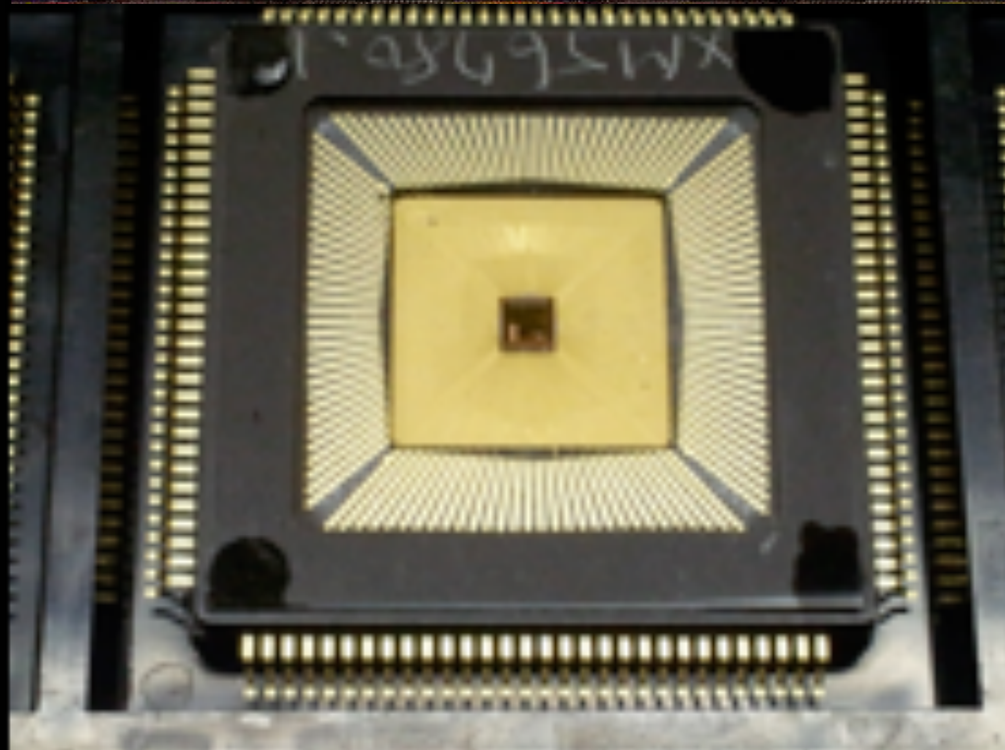
Everything ends in a Chip

Silicon is everywhere

Transistor

1947





Transistors Density Evolution

AMD Epyc Rome 2019 has up to 39.54 billion transistors

1950s
Silicon Transistor

1
Transistor

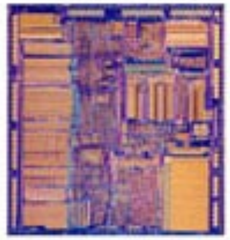
1960s
TTL Quad Gate

16
Transistors

1970s
8-bit Microprocessor

4500
Transistors

1980s
32-bit Microprocessor



275,000
Transistors

1990s
32-bit Microprocessor

3,100,000
Transistors

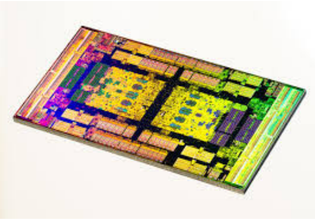
2000s
64-bit Microprocessor

592,000,000
Transistors

2010s
3072-Core GPU

8,000,000,000
Transistors

2020
AMD EPYC



39.54 billion
Transistors

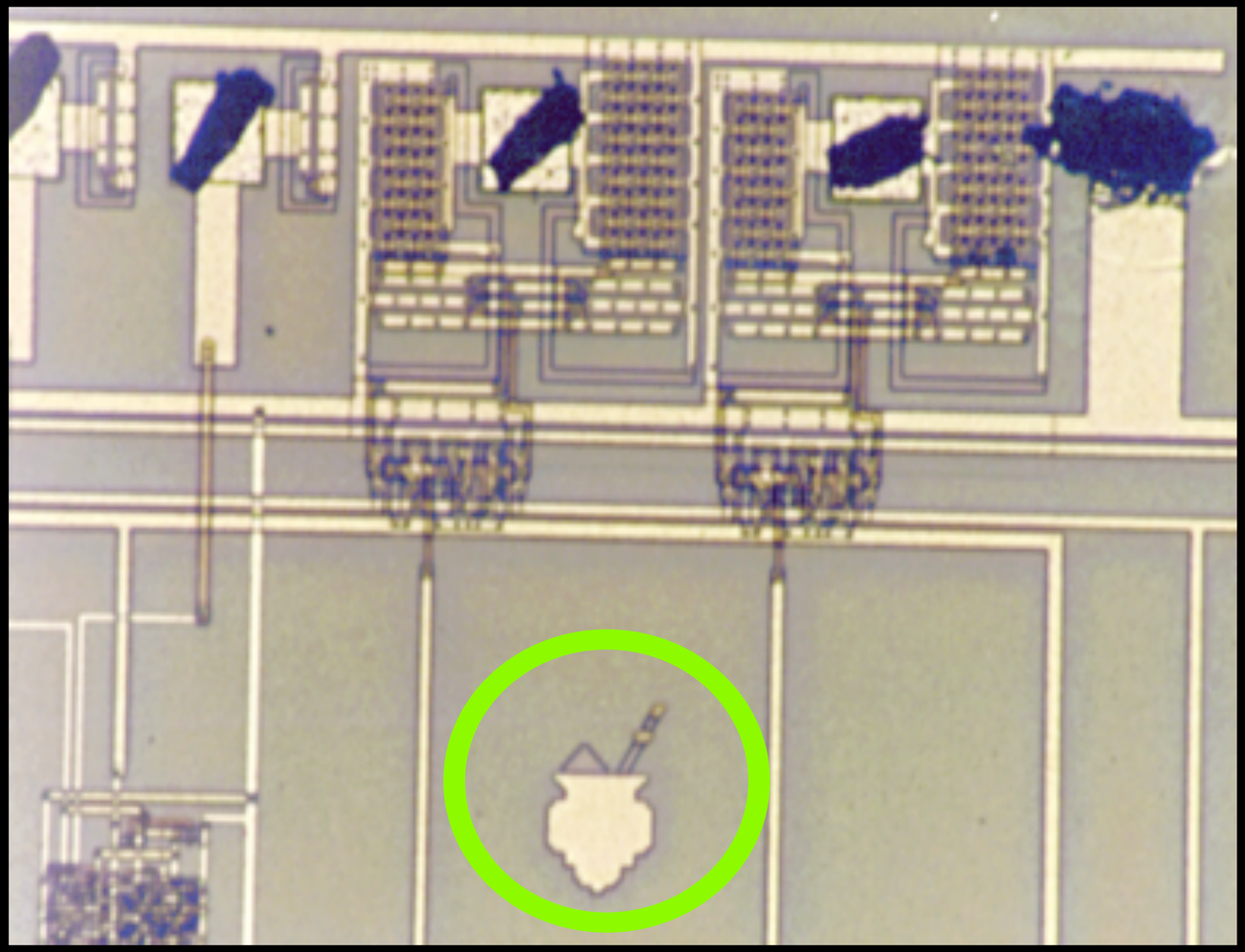
http://www.computerhistory.org/siliconengine/

GME

UFRGS

A bit of History

1984 – Access to MPW prototyping (fabricated at ES2, France)



1986 – RISCO 16b/32b completed
First RISC Microprocessor in Brazil (Architecture to Layout)

Visualization of Working Chips using E-Beam Microscope

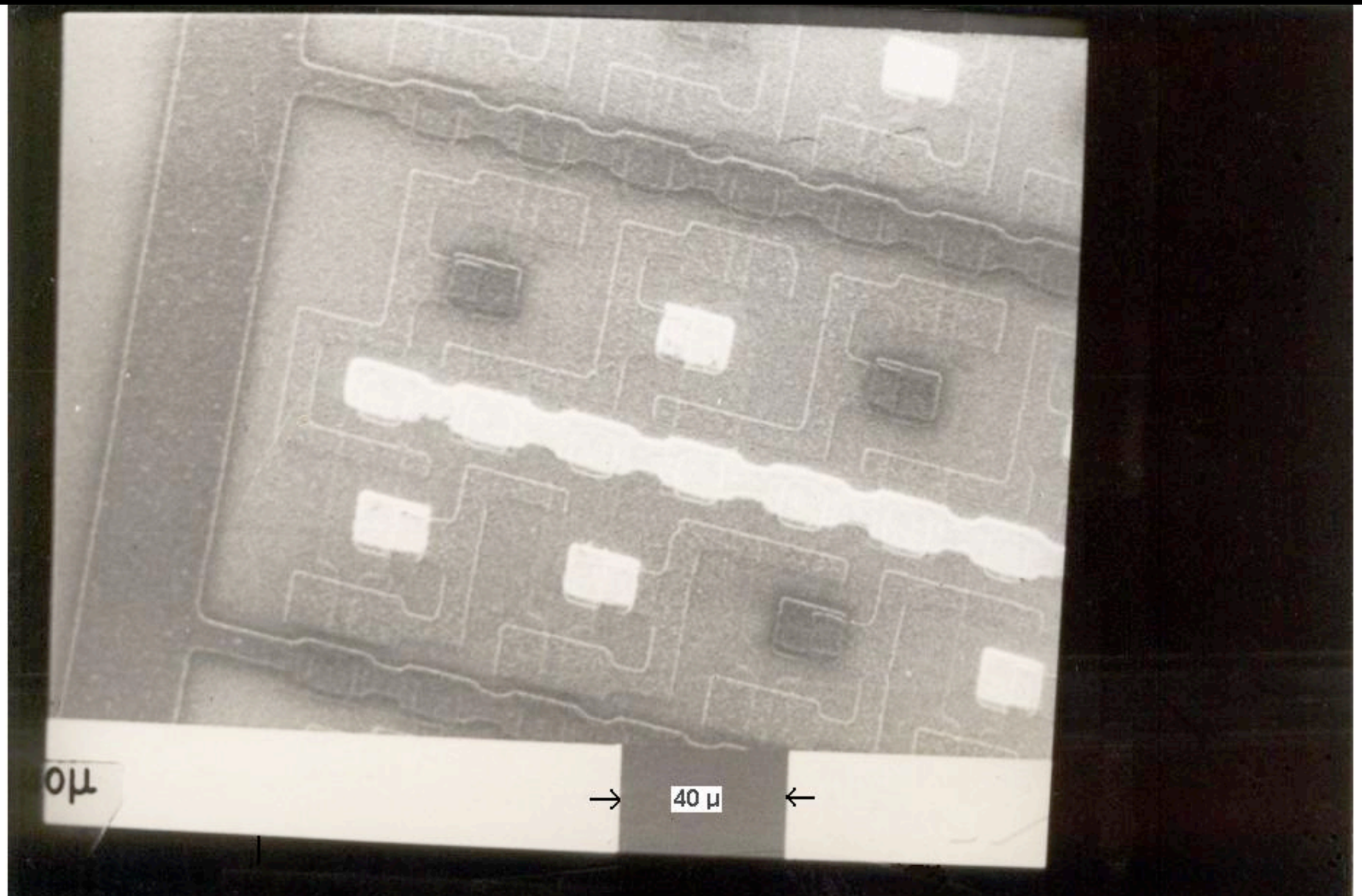
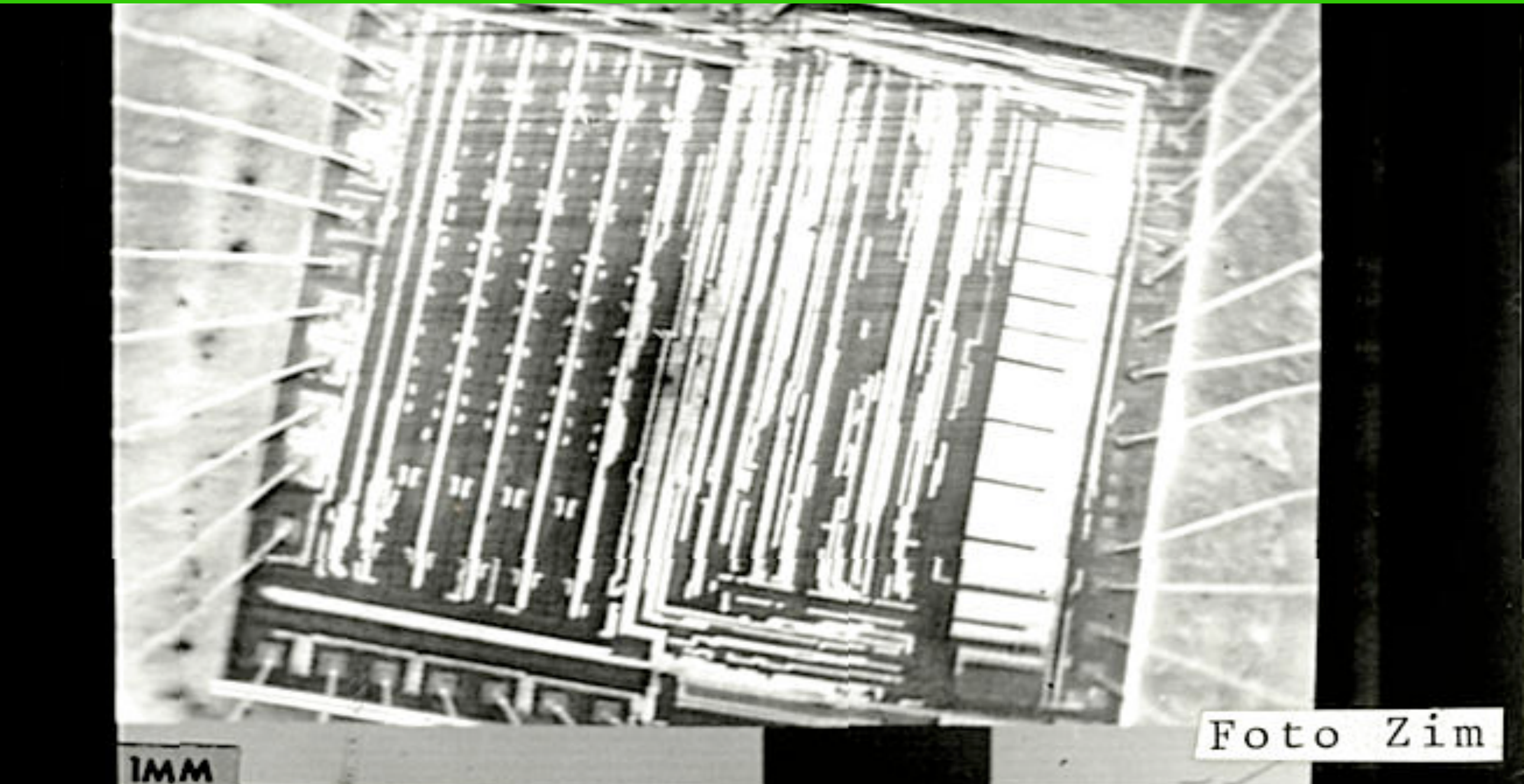


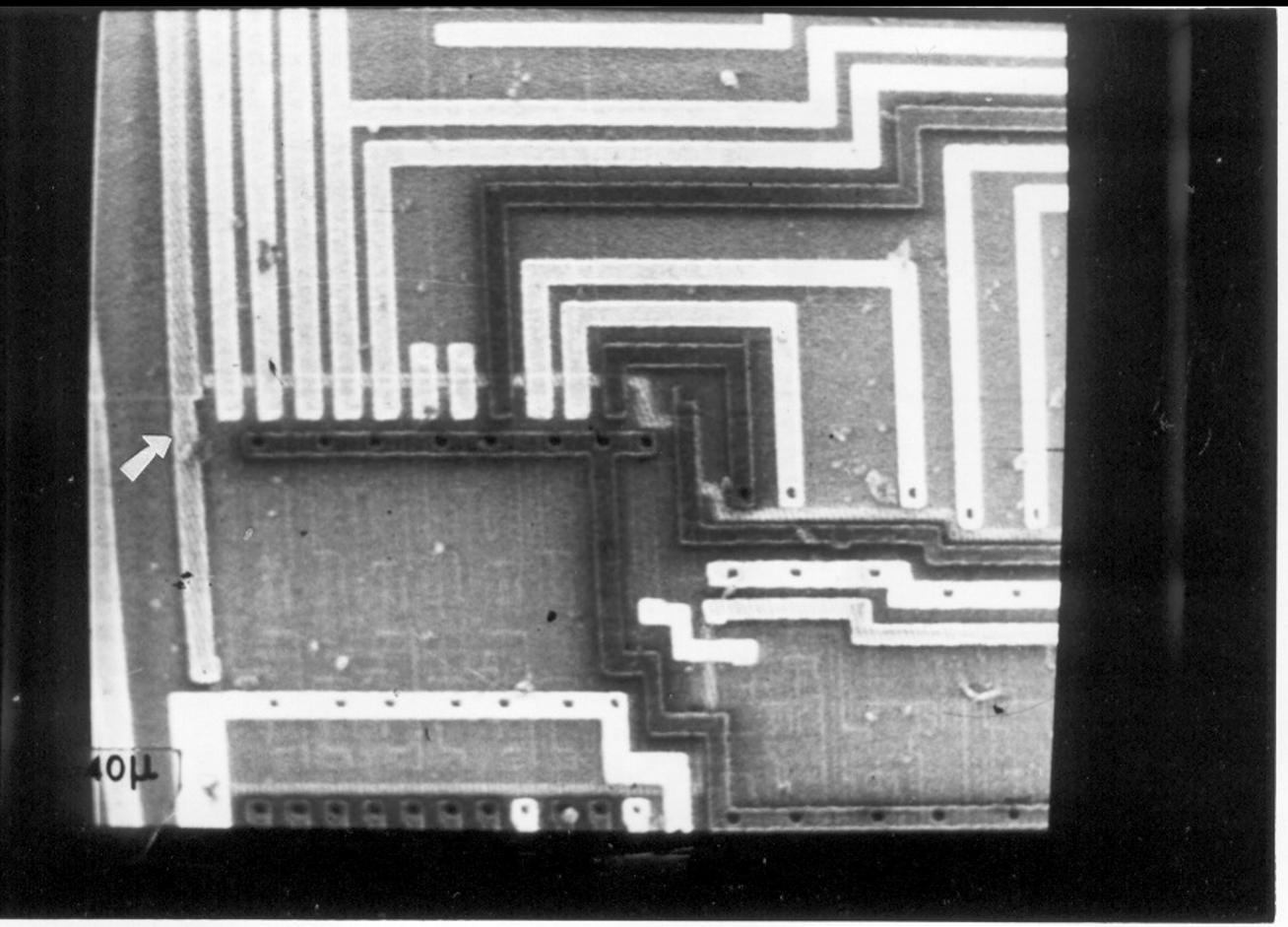
Image from Voltage Contrast
(A= x500, E = 40 µm)

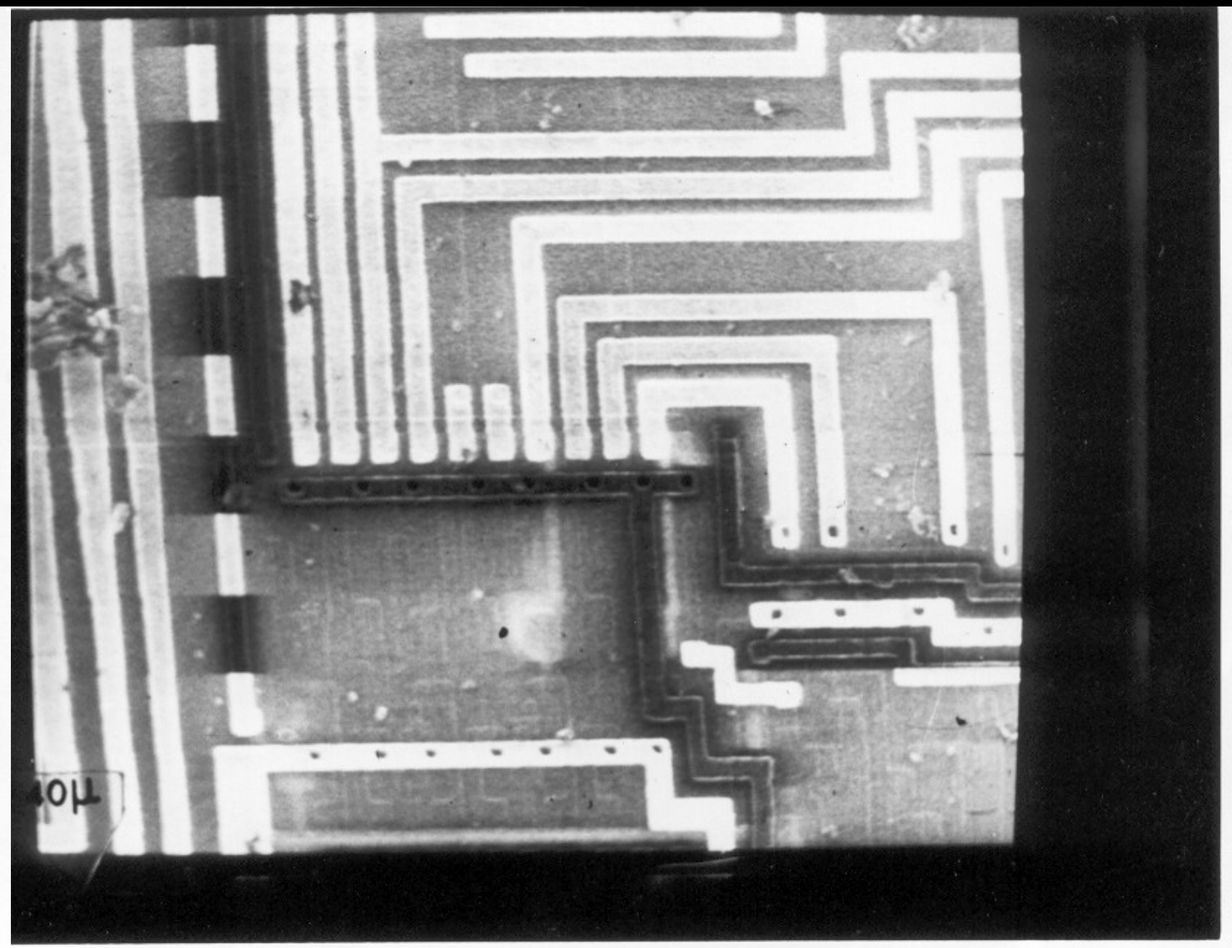
Carlos Hurtado
UFRGS 1986

Visualization of Working Chips using E-Beam Microscope



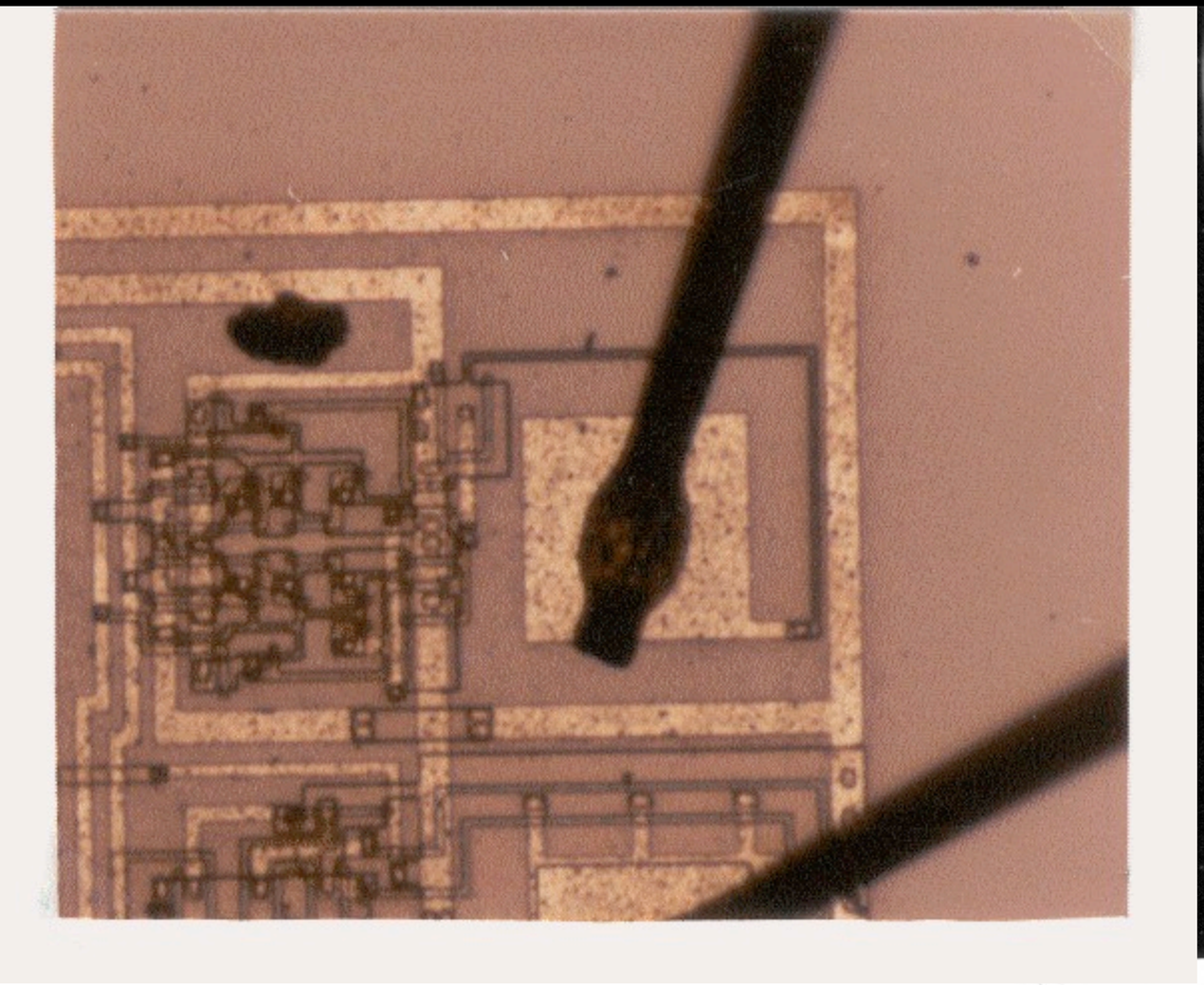
Visualization of Working Chips using E-Beam Microscope



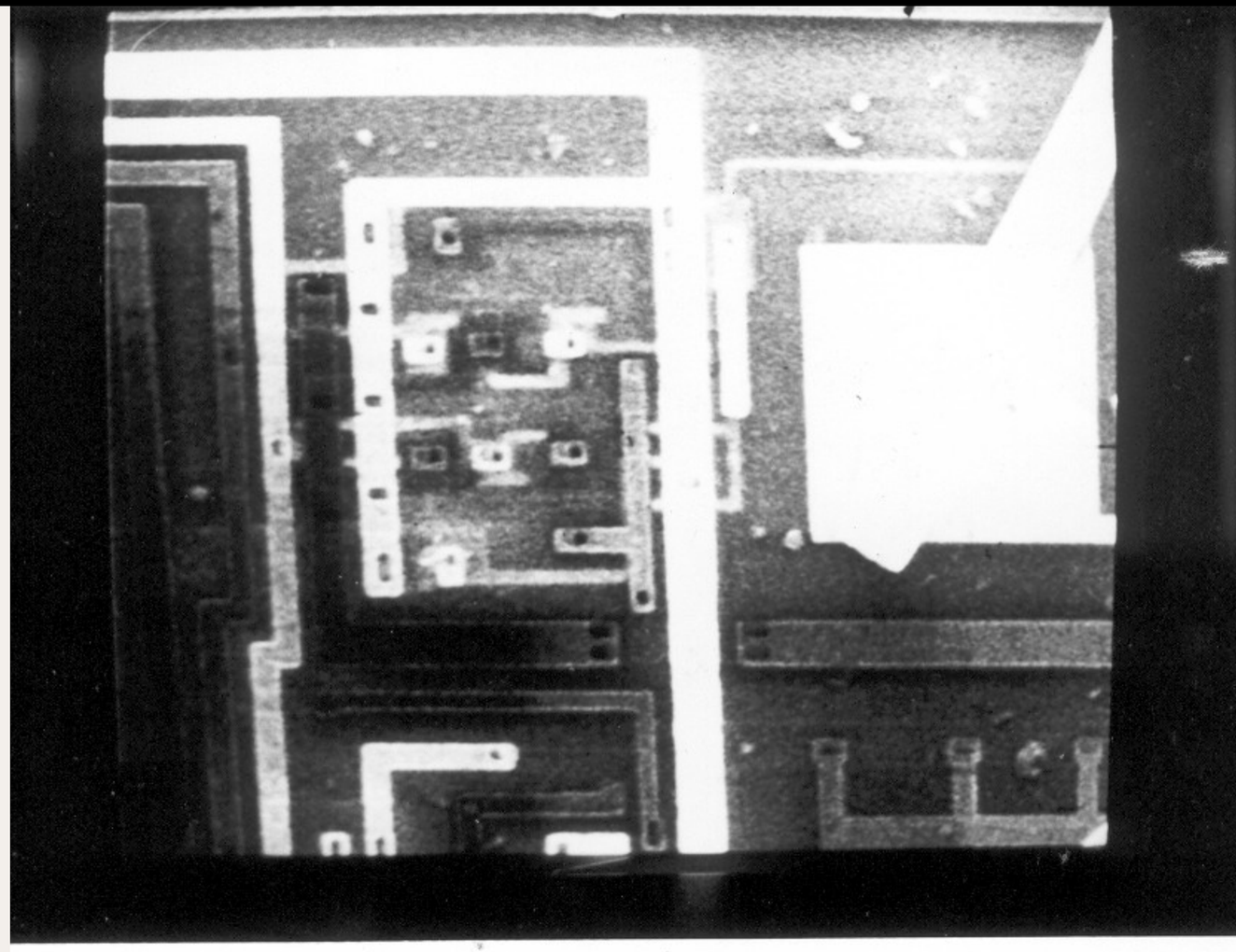


Observation of DC Signals (A= x500)
Carlos Hurtado 1986

Visualization of Working Chips using E-Beam Microscope



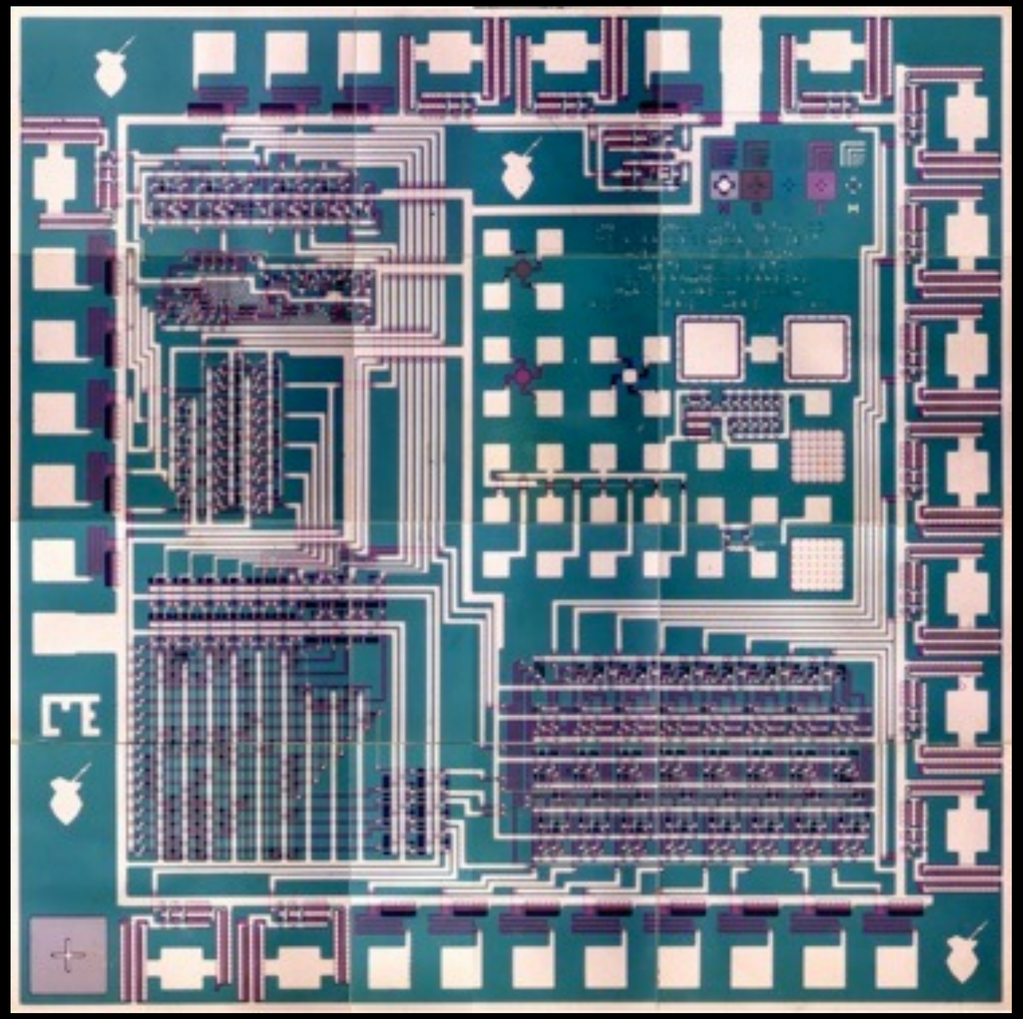
View of the Clock Pad with two phases
with an optical microscope (A= x200)



View of the Clock Pad at phase 1
with an EBeam microscope (A= x200)

Carlos Hurtado 1986

M1B Microprocessor (1990)

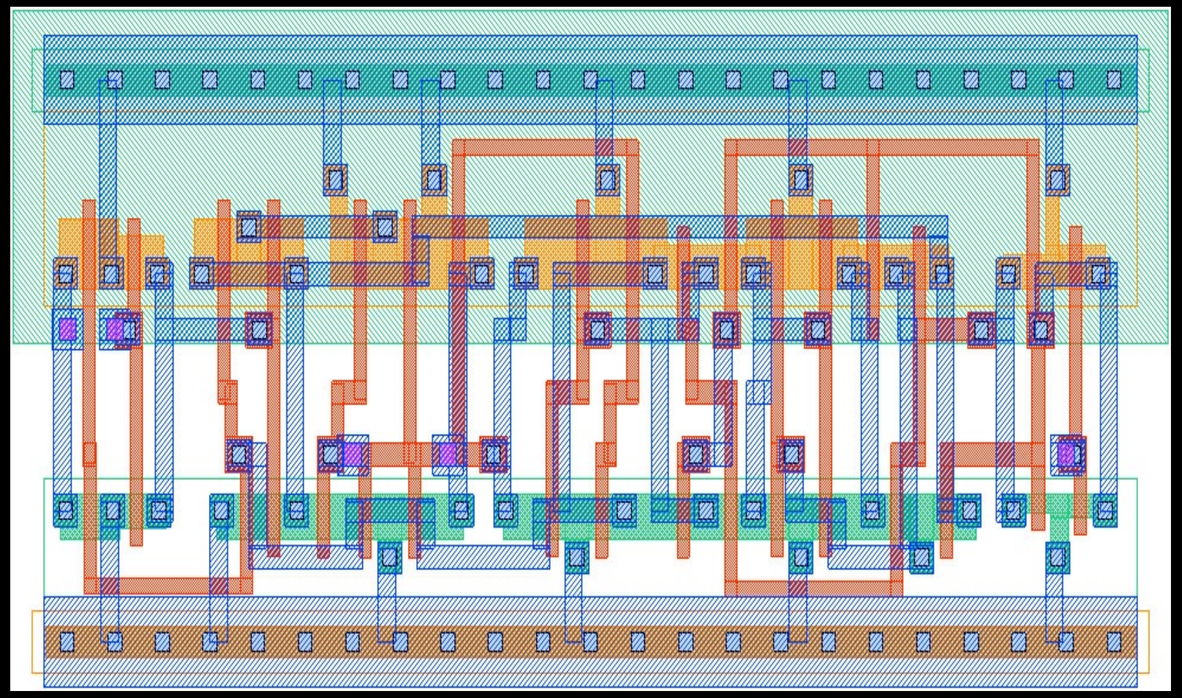


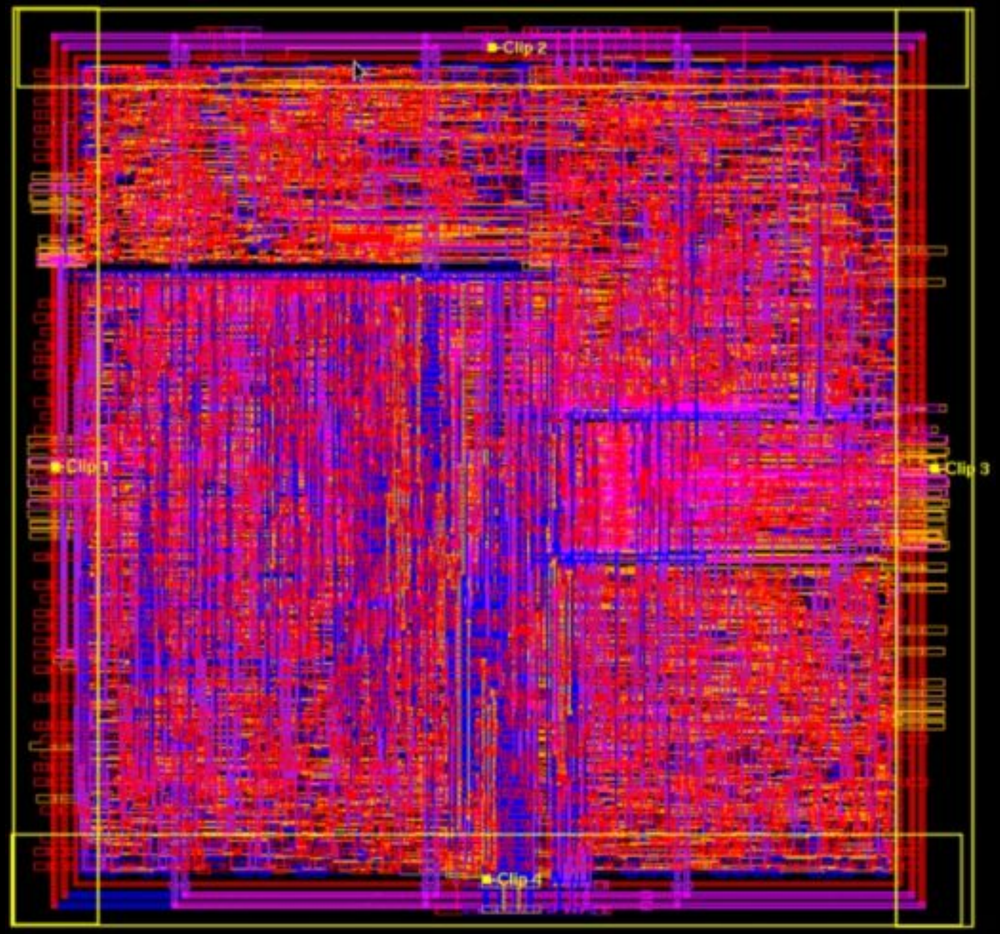
Transistors with metal gate

First chip (NMOS) design at the UFRGS Graduate Program on Computing and fabricated at Physics Institute of UFRGS

UFRGS

Layout Visualization





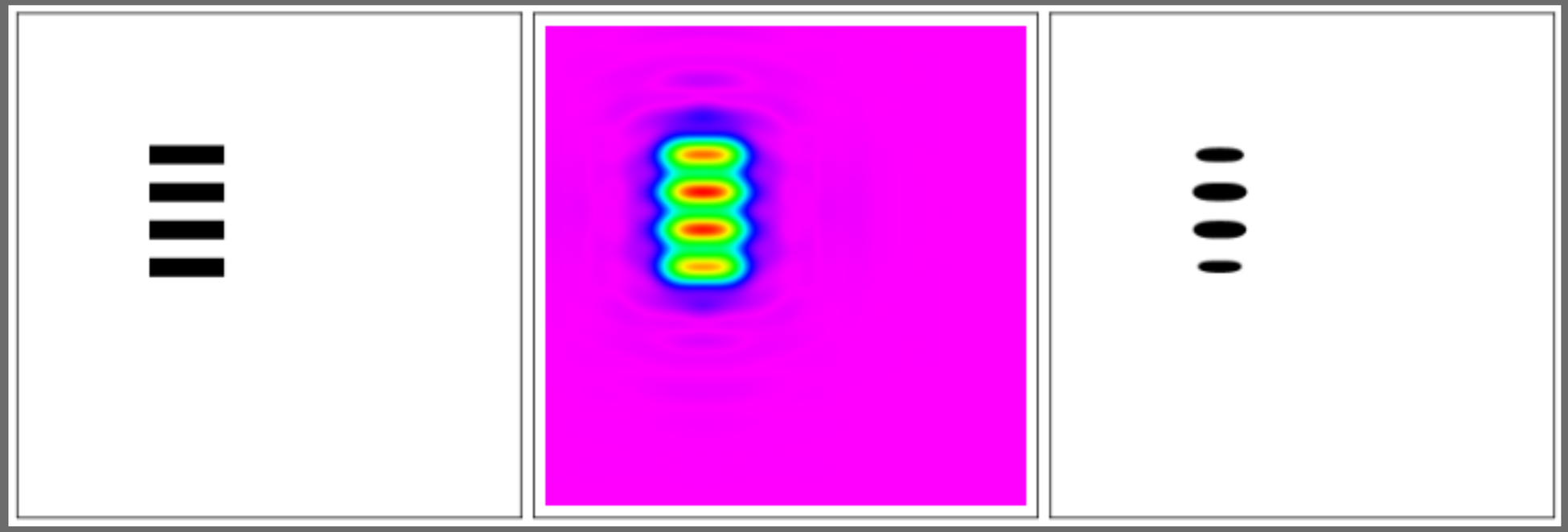
Close visualization
Important to see rectangles

Far visualization
Not important to see rectangles

After a level of visualization, it can be done a rendering to see the full circuits as an rendered image

Lithux

EDA tool for Lithography Simulation



Mask

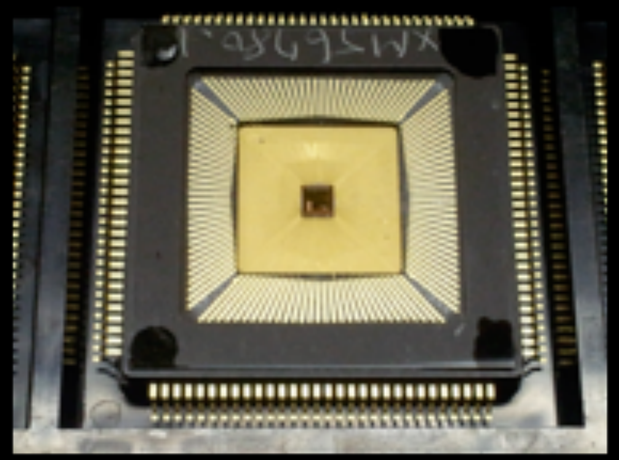
Intensity Map

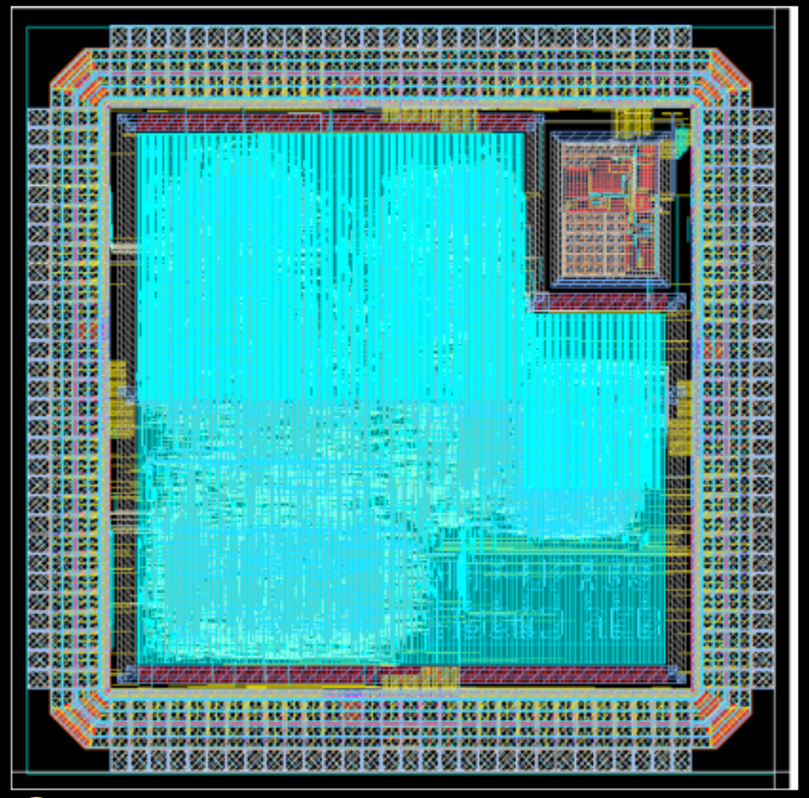
Printing Pattern

Tania Ferla

TMR MIPS Duo Core 32 bits

chip tolerant to radiation effects 2012

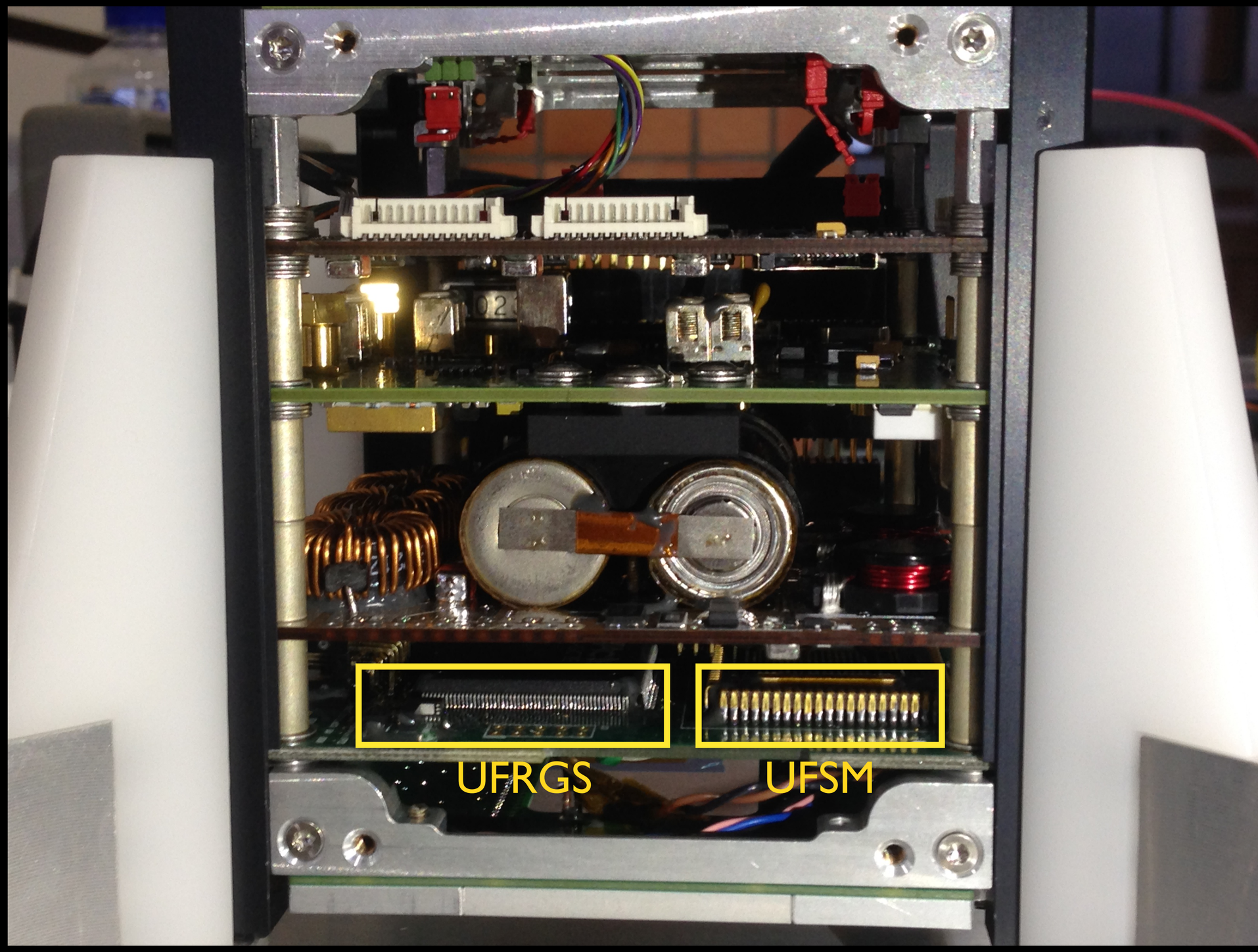




See more at: http://www.nscad.org.br/site/nsc21101

UFRGS

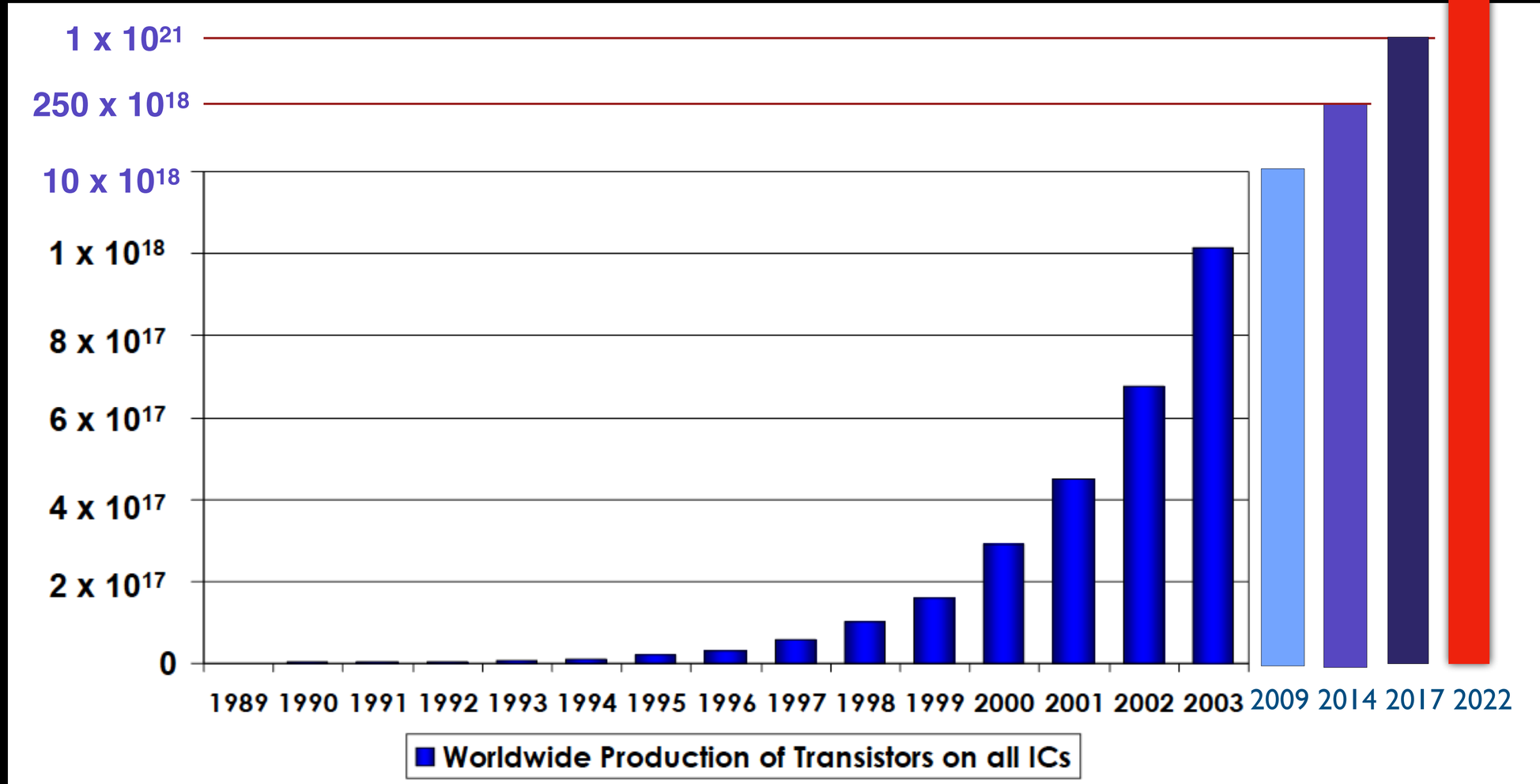
NanoSatC-BR I



1 sextillion in 2017

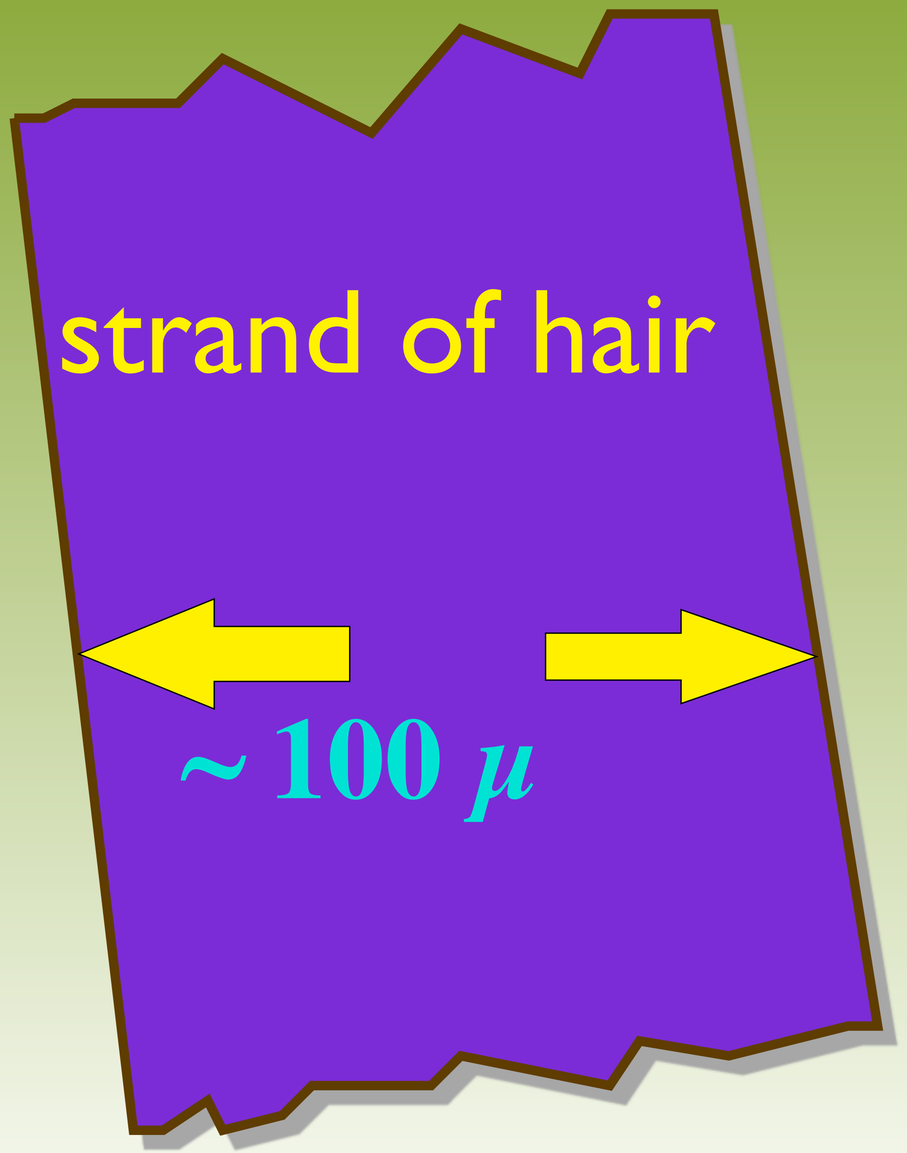
13 Sextillions Transistors Produced from 1947 to 2018

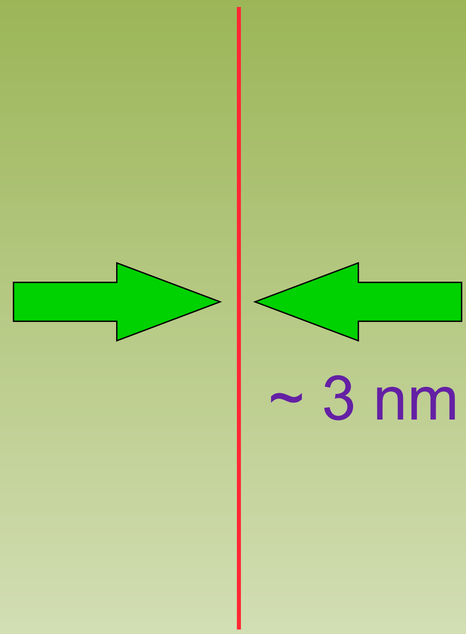
Estimated more than 8 sextillions



Source: SIA

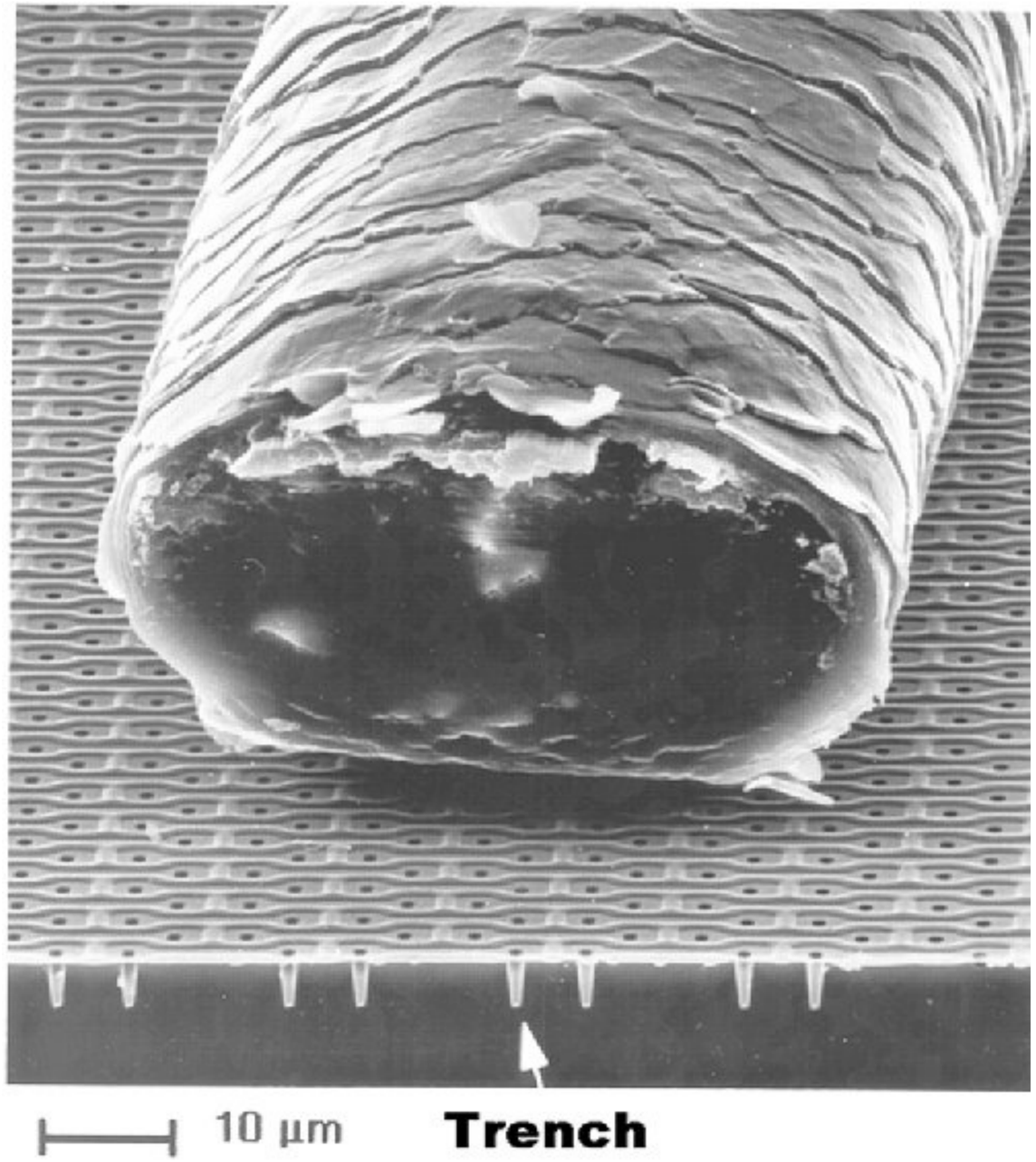
SIA SEMICONDUCTOR INDUSTRY ASSOCIATION





tech node dimensions

33000 smaller

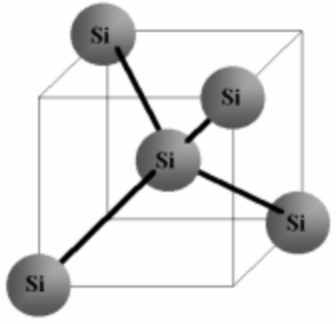


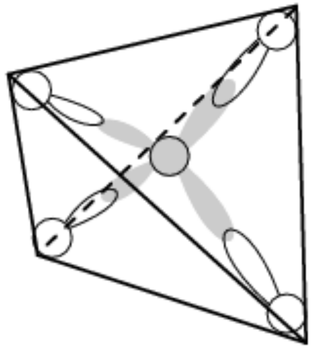
strand of hair over a memory (from Siemens, 1989)

Semicondutors

Silicon Cristals

Crystal Silicon Ingots

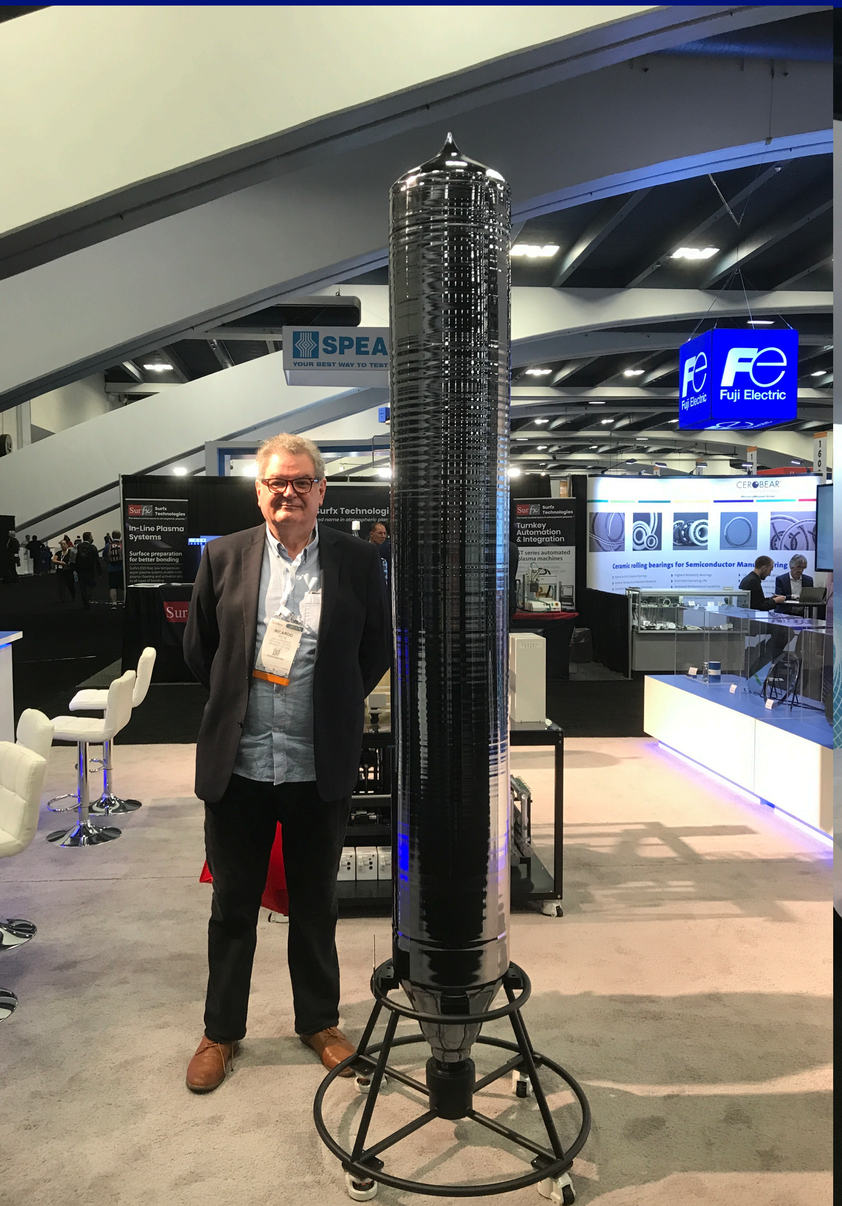




GME

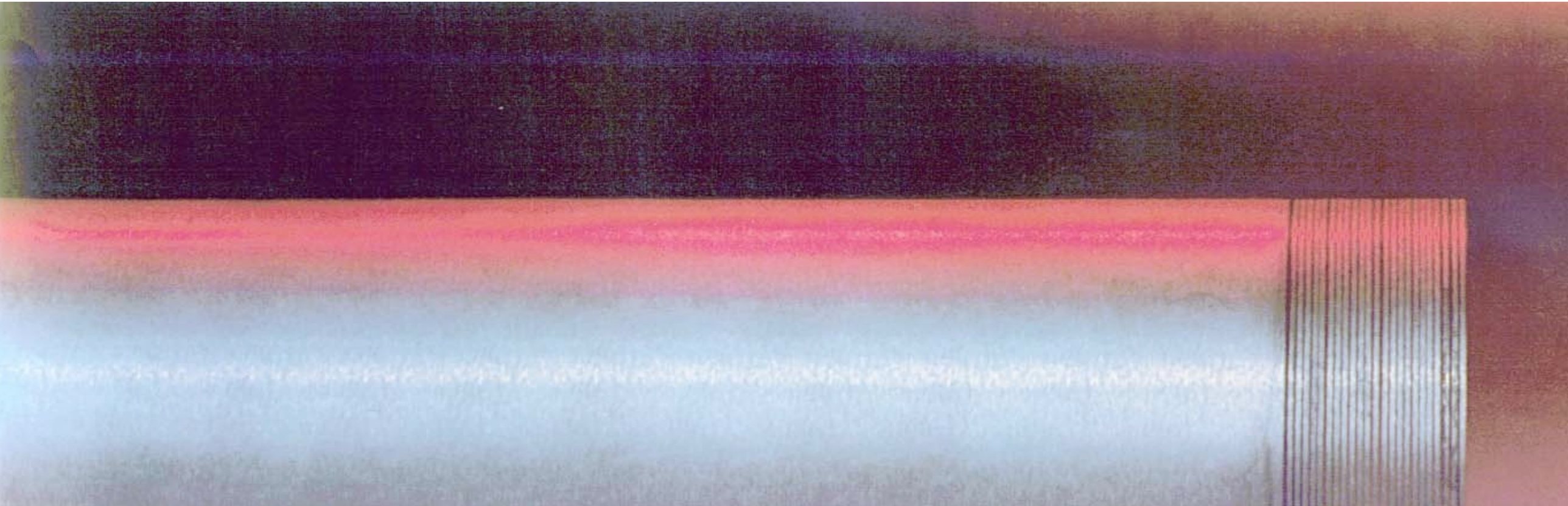
UFRGS

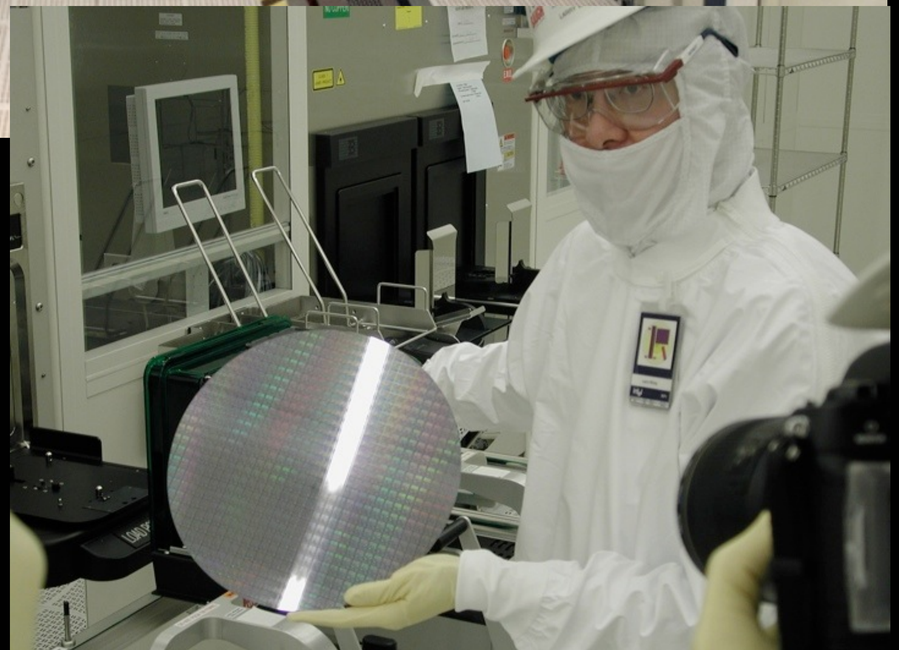
Crystal Silicon Ingot



Ingot cutting

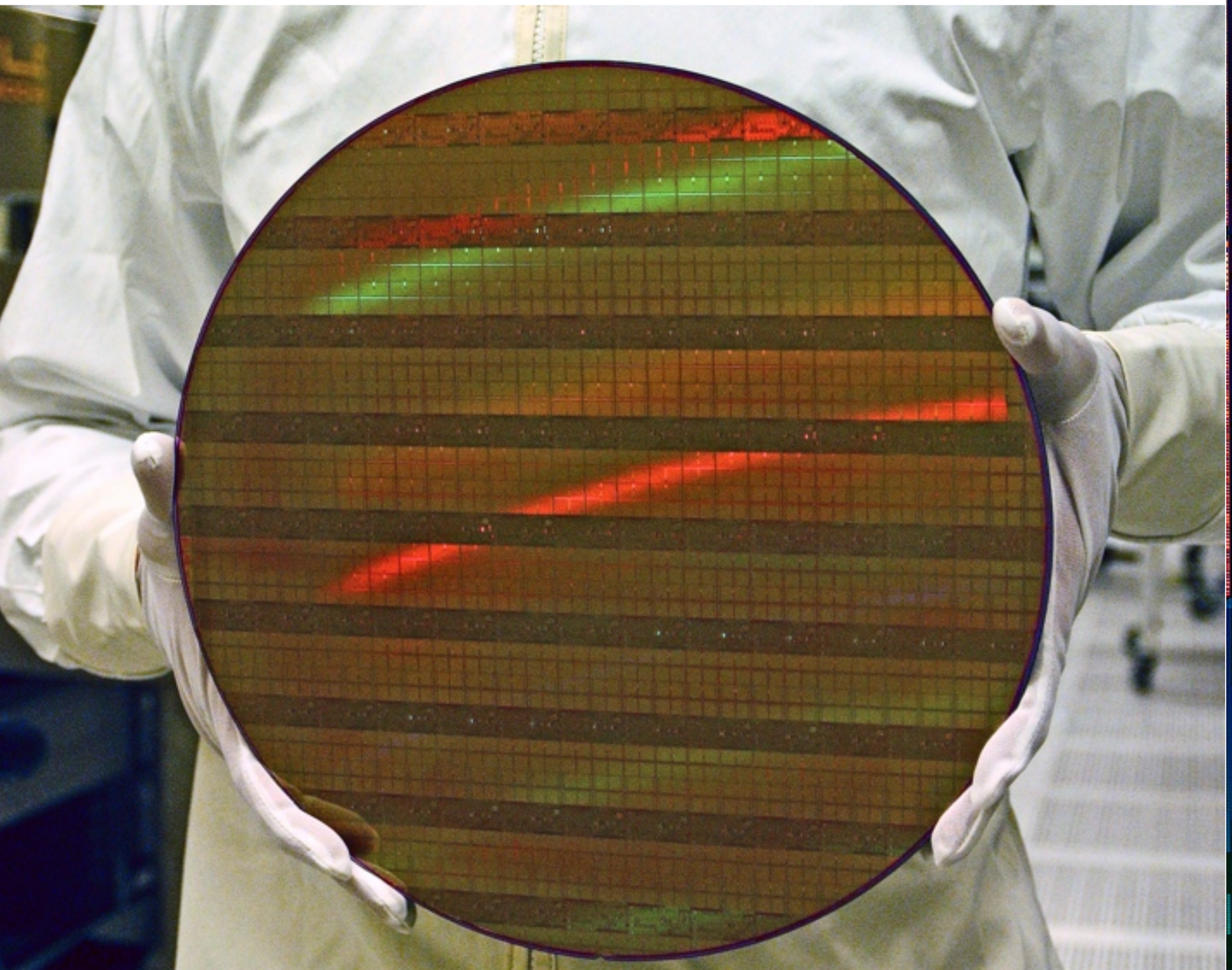
Production of Silicon Wafers

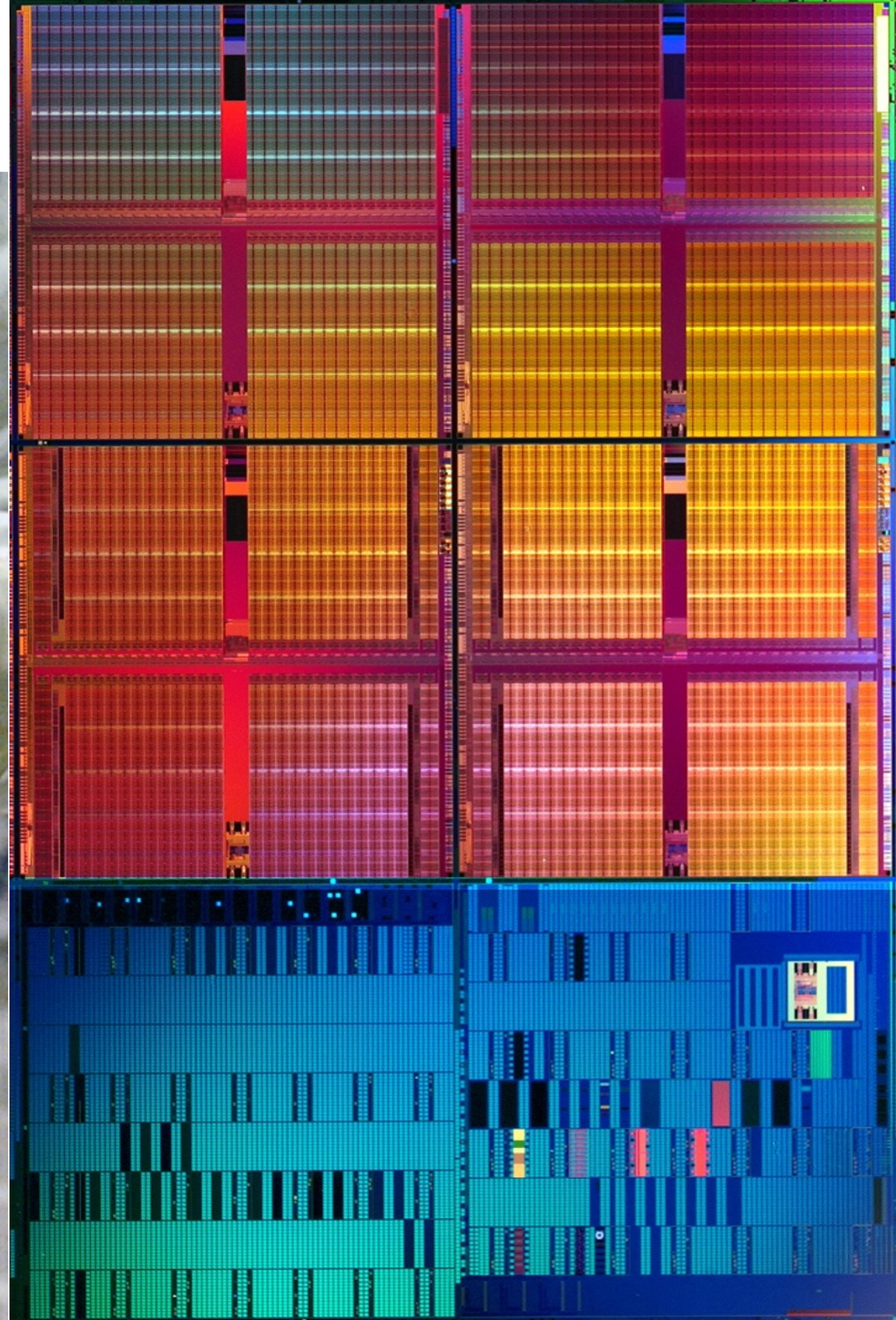




Source: Intel

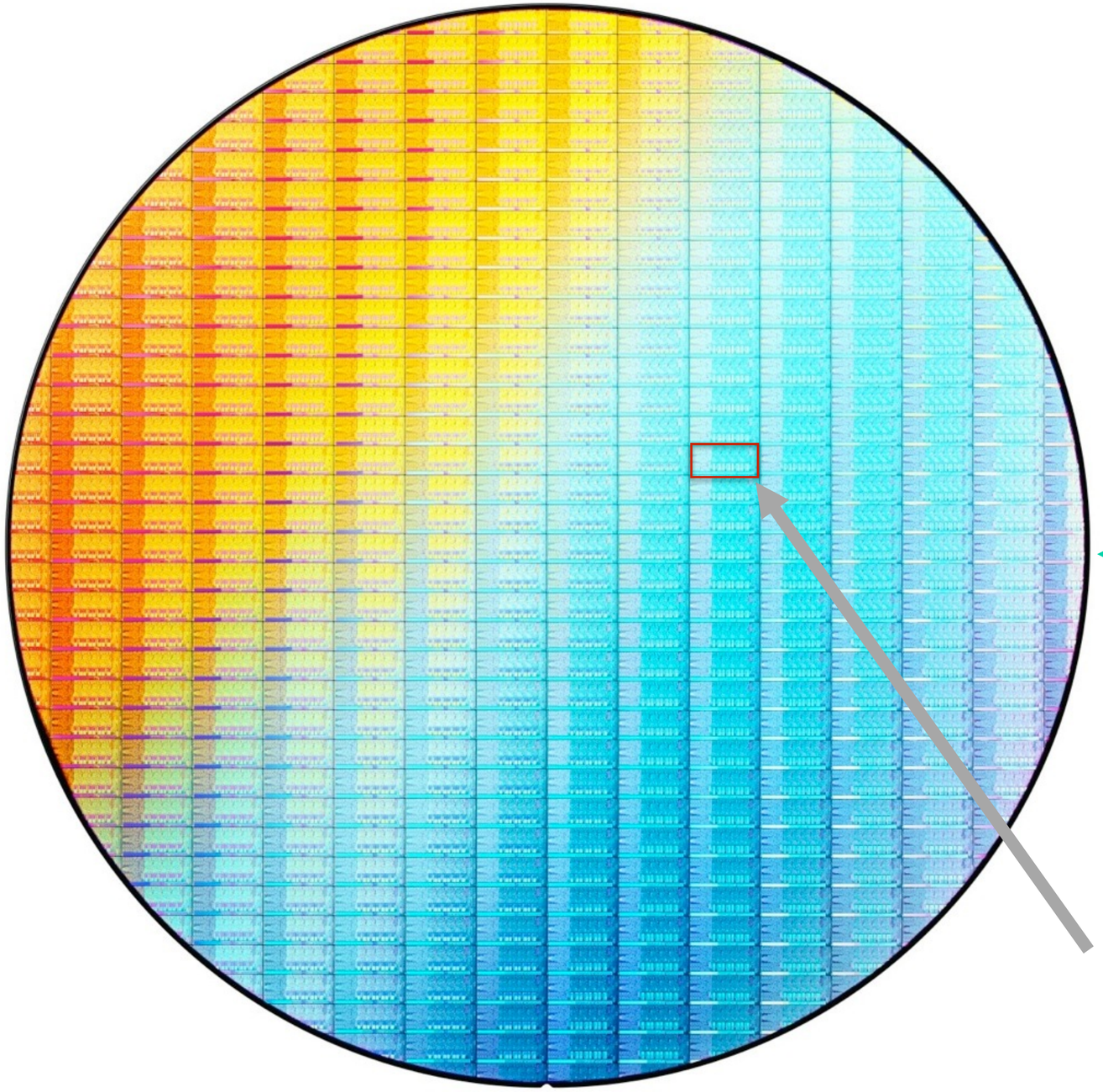
Intel SRAM Wafer
45 nm





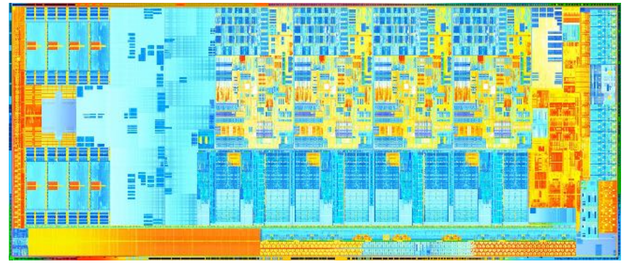
April 2012

22 nm technology



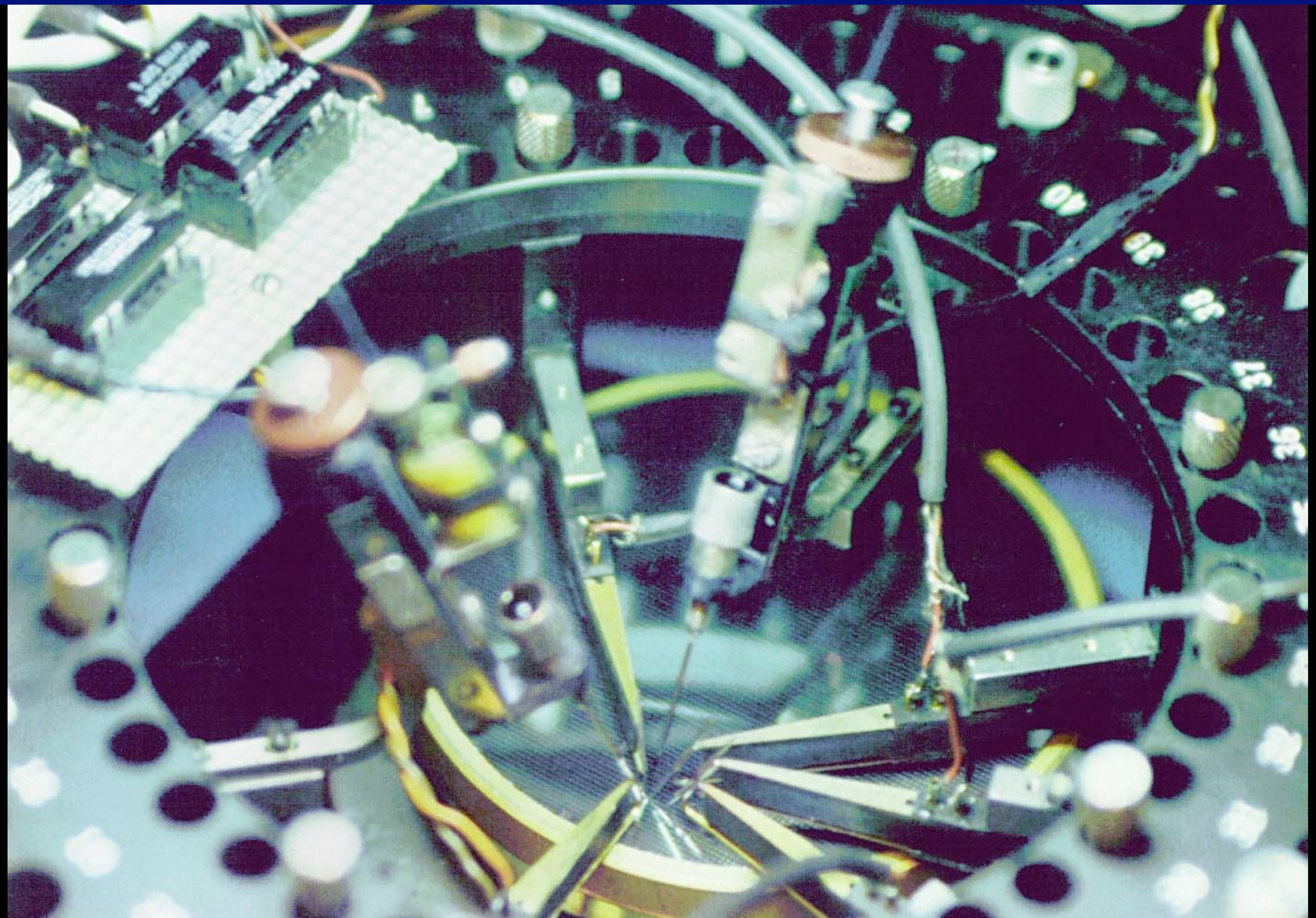
Wafer

single die

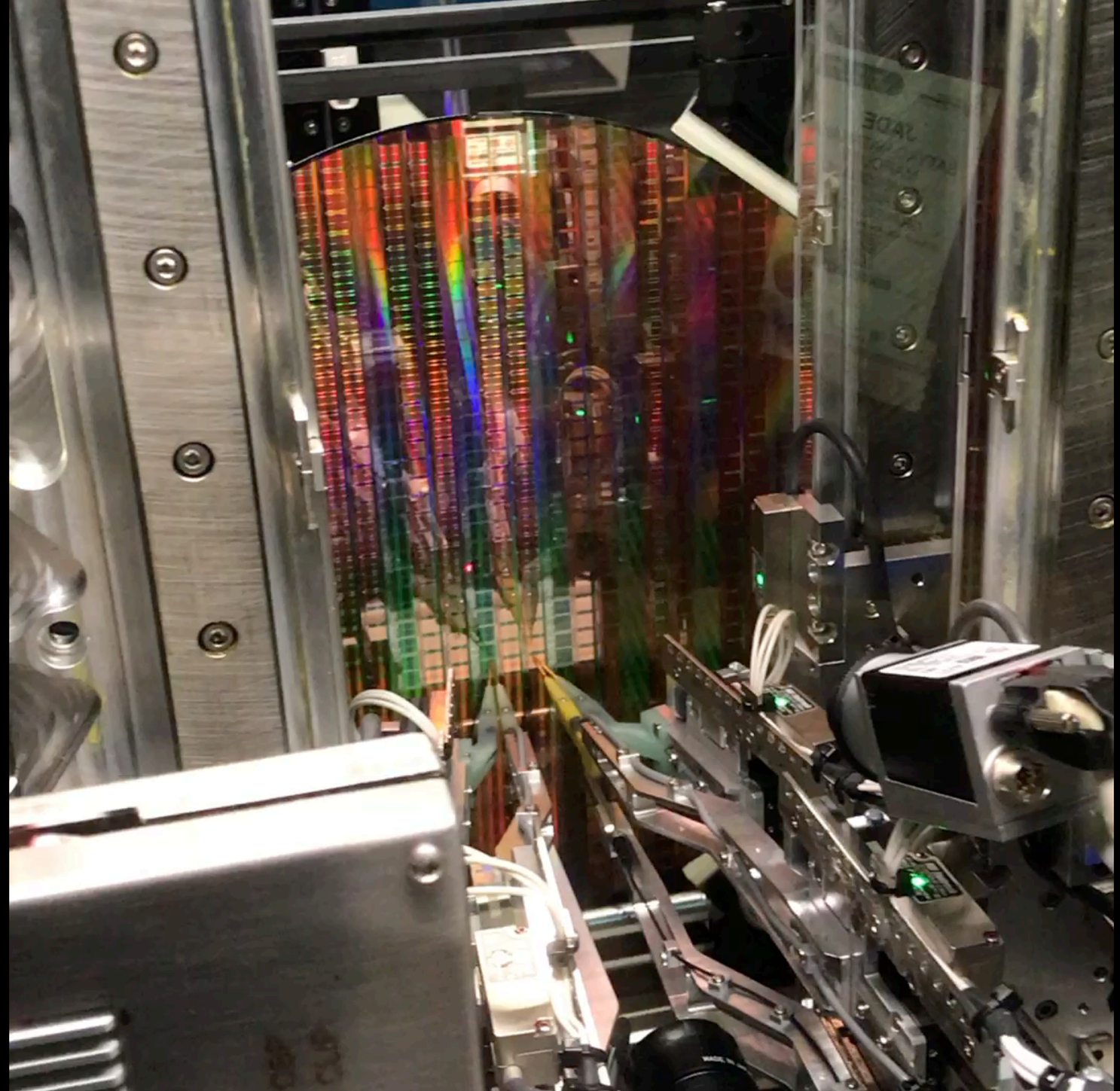


Intel® Core™ i7 -3920 of third generation
1,4 Billions of Transistors using 160mm²

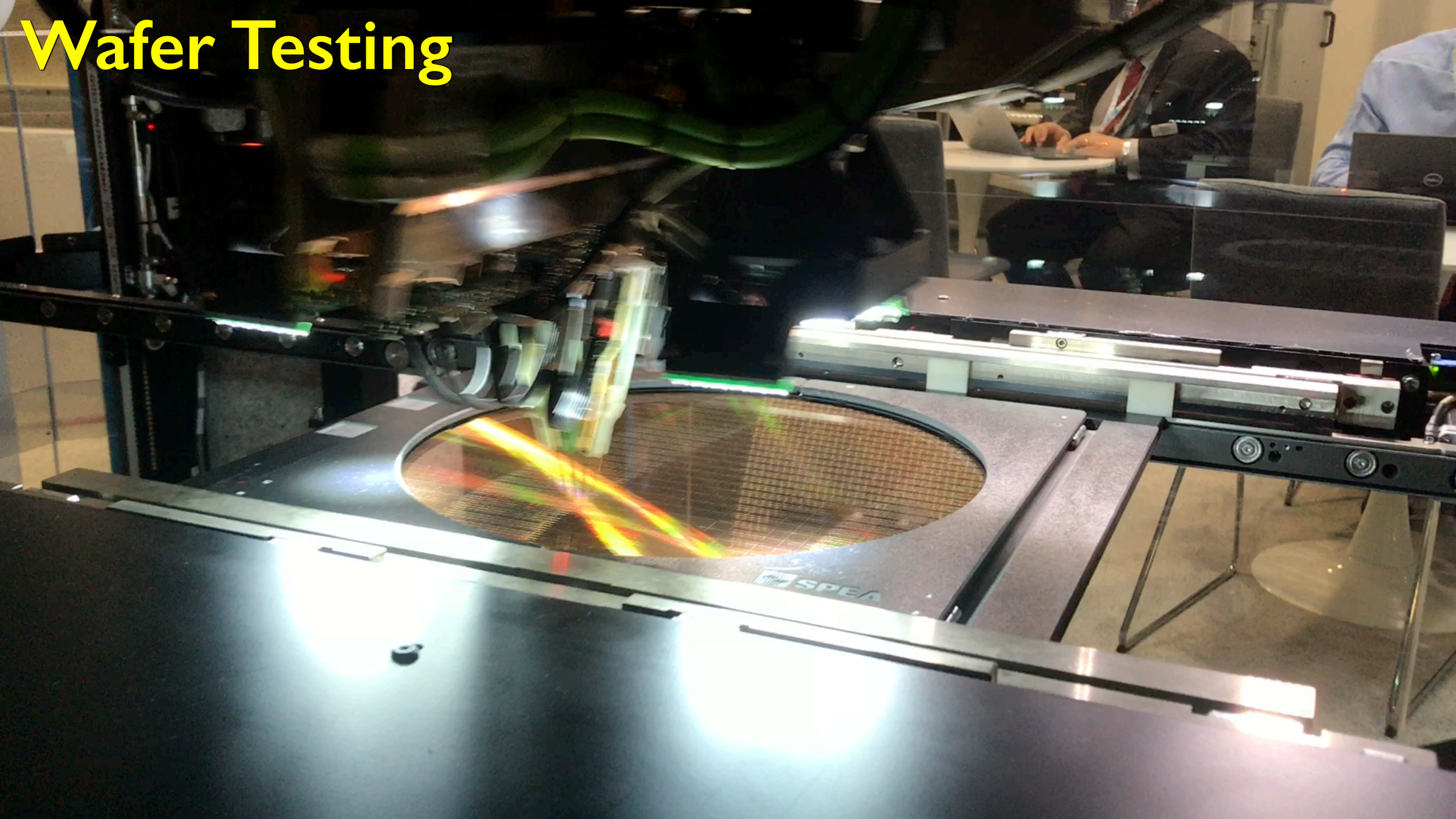
Wafer Testing



Wafer Testing

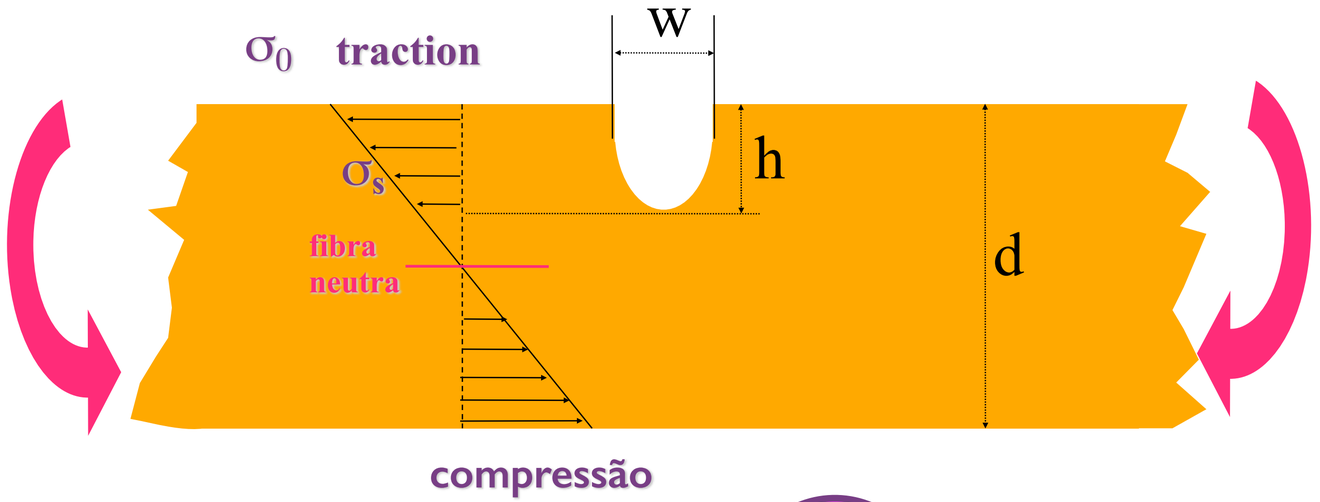


Wafer Testing



Chips Separation

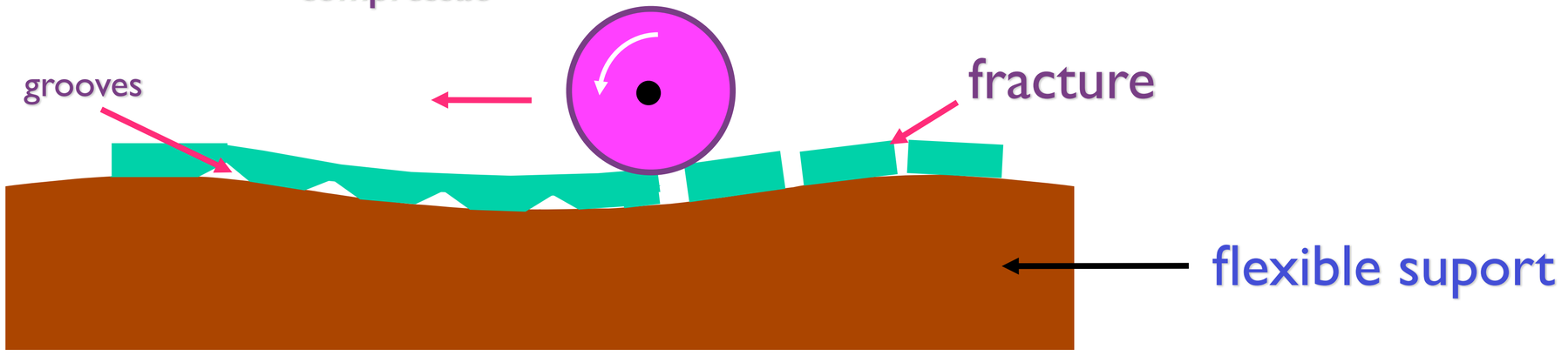
F= applied force concentration factor



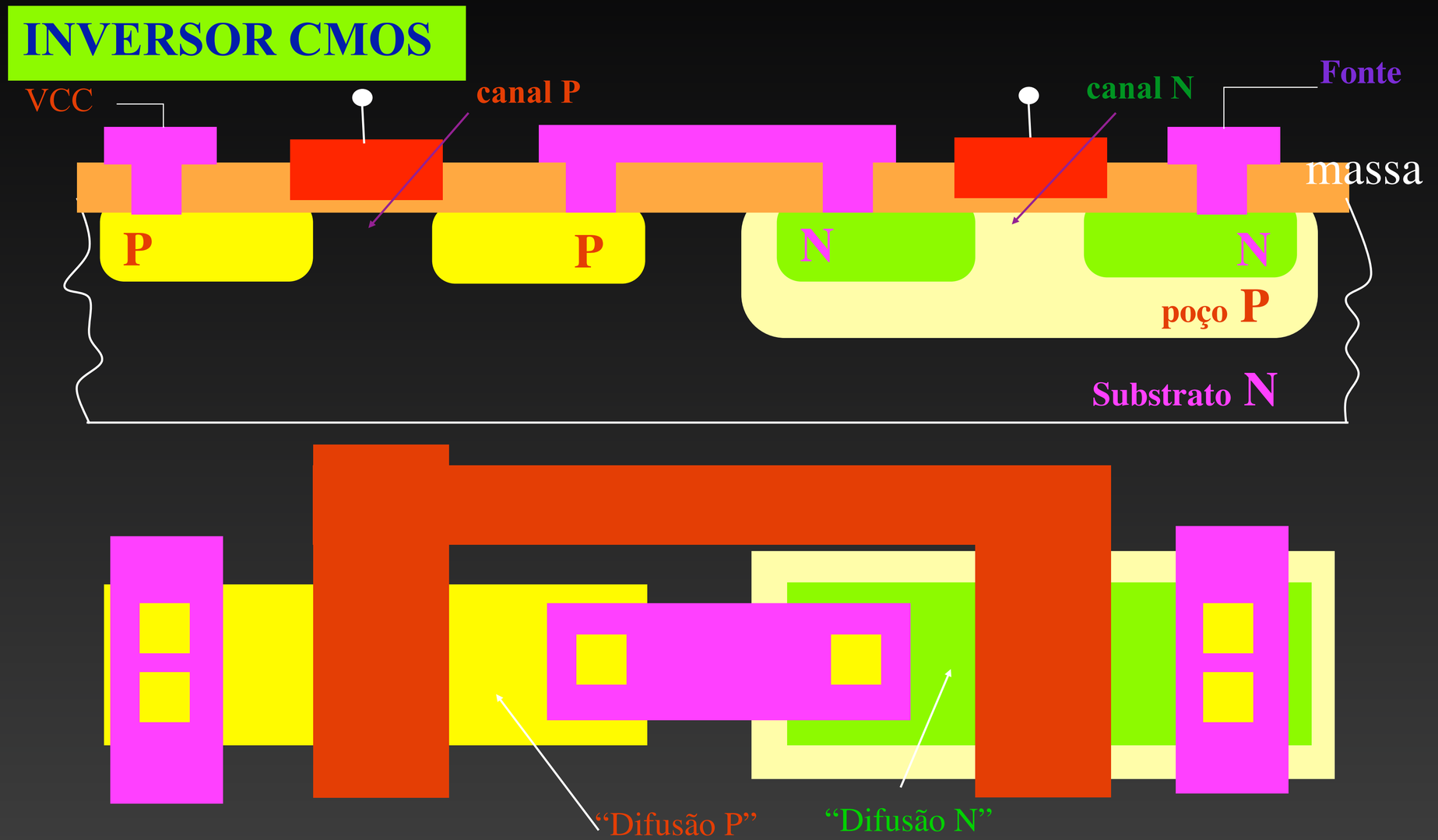
$$F = \frac{\sigma_s}{\sigma_0} = f(H,W)$$

$$H = \frac{h}{d}$$

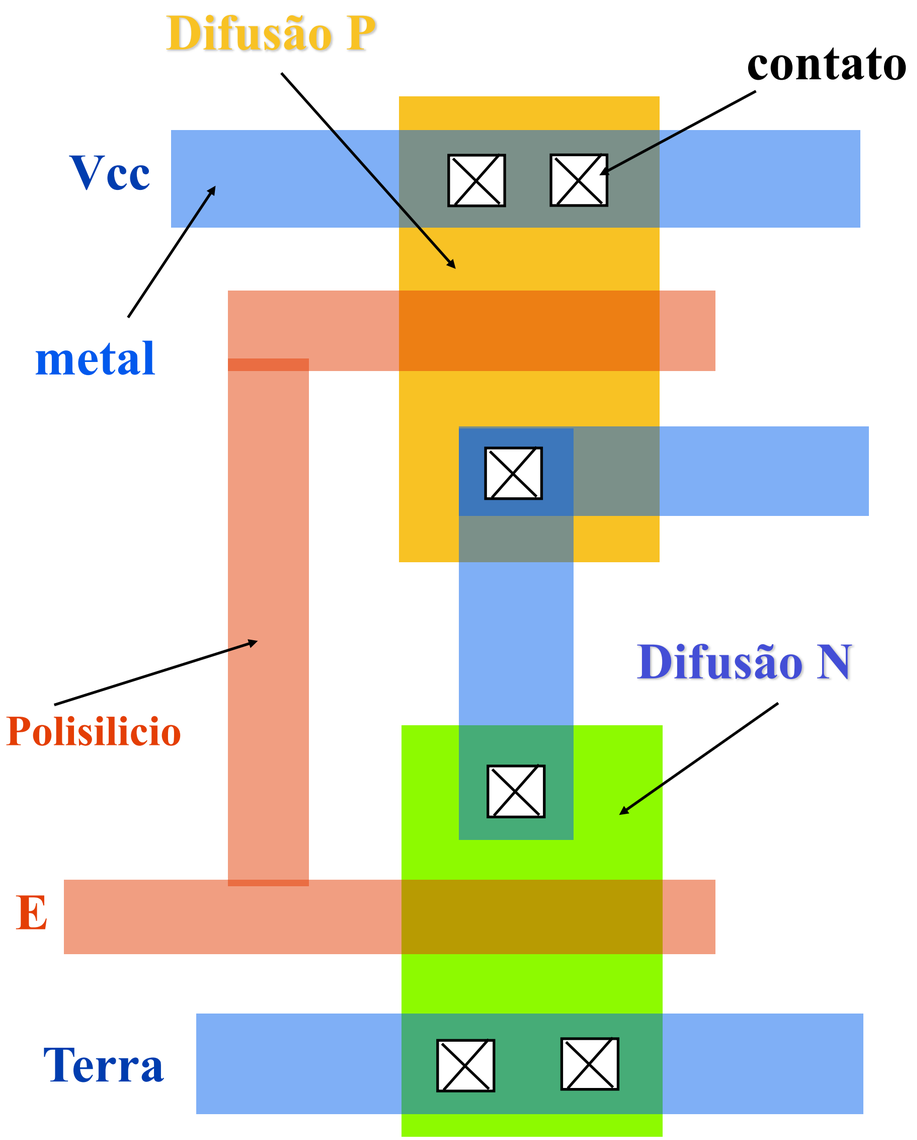
$$W = \frac{w}{h}$$



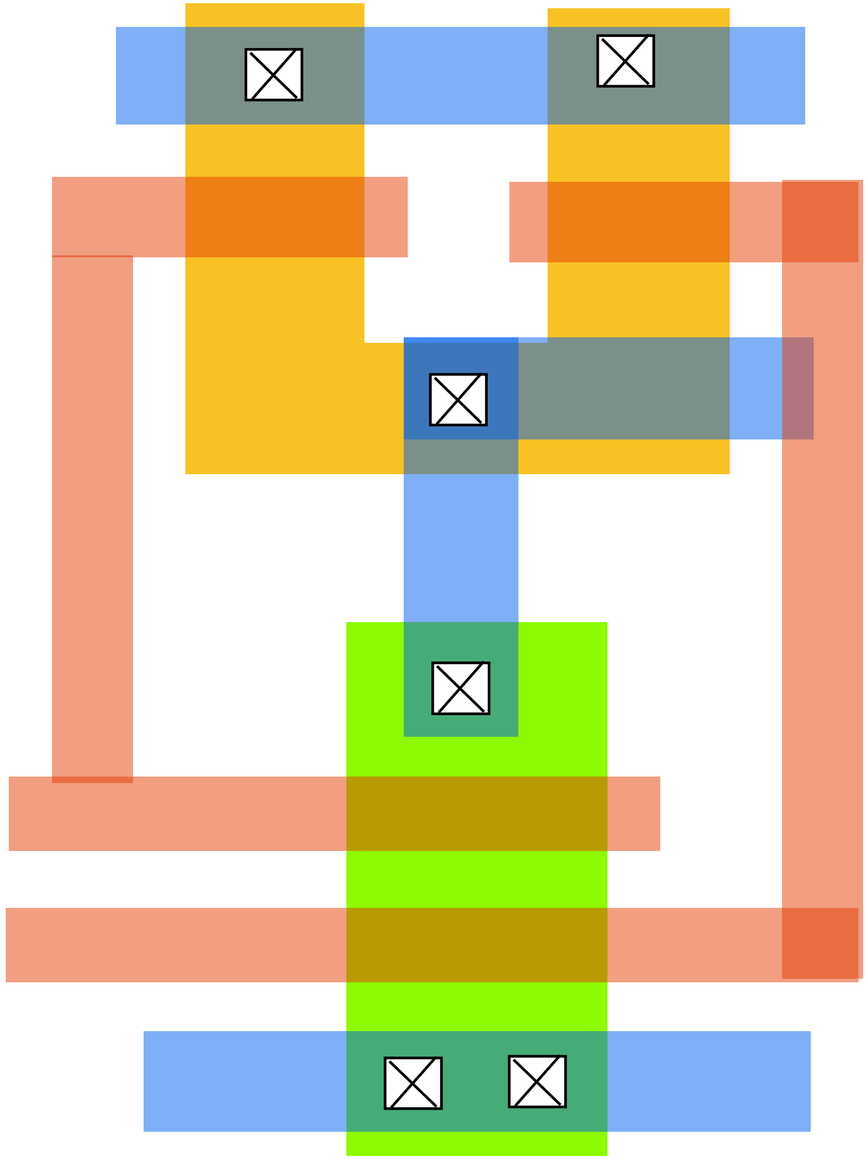
Projeto de Portas Lógicas

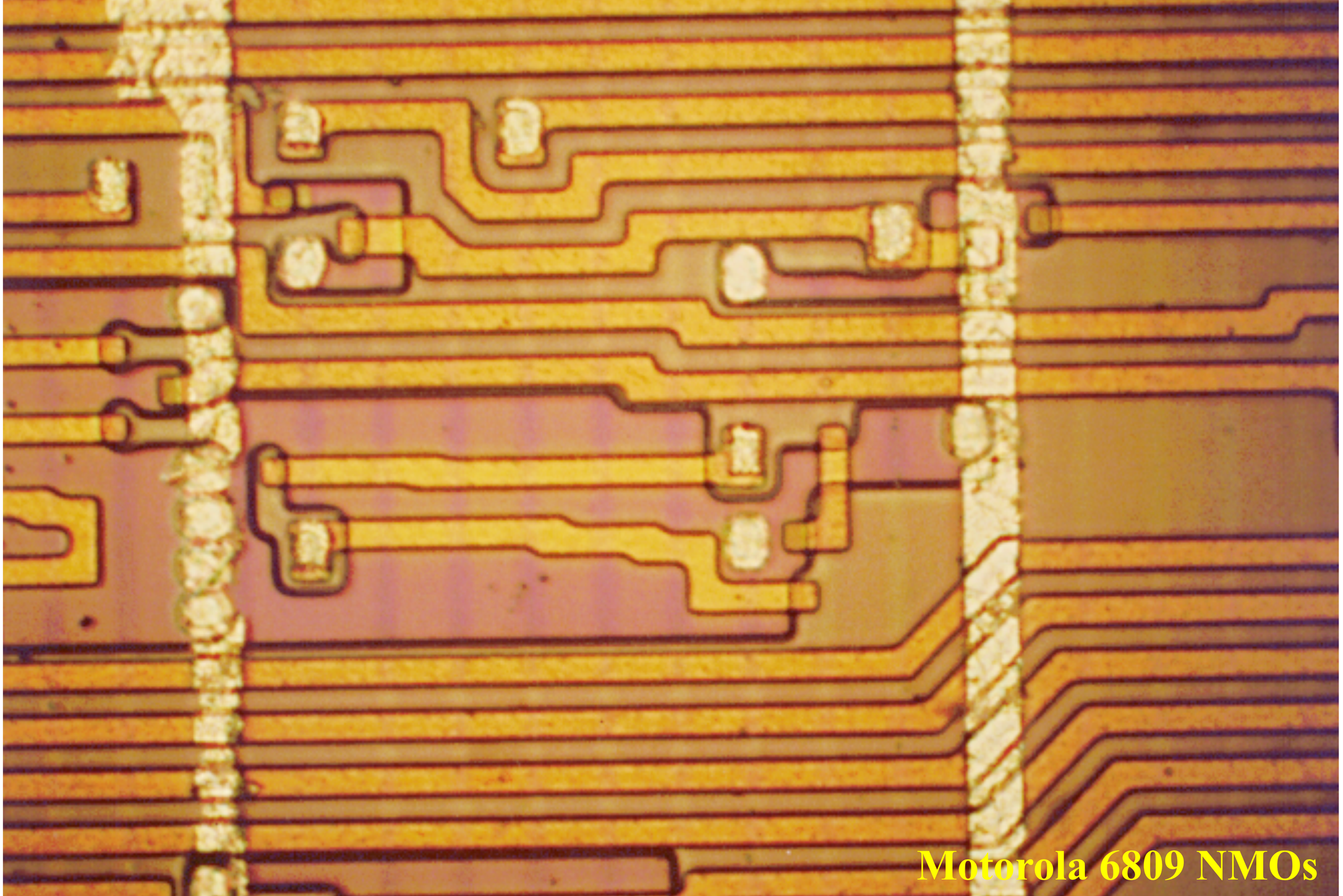


C M O S INVERTER LAYOUT



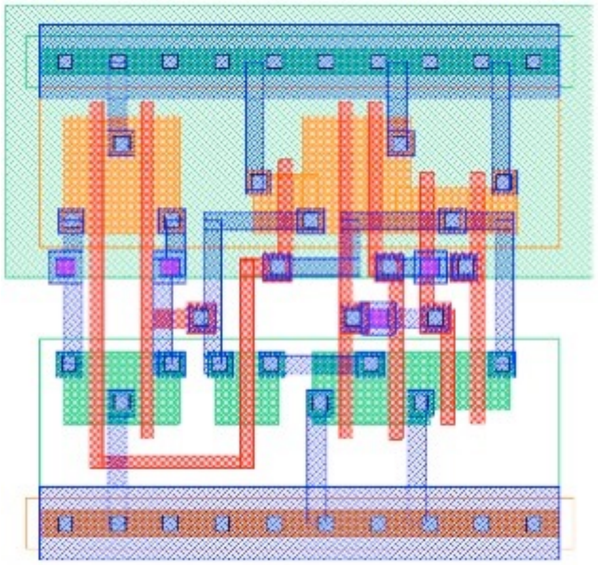
C M O S NAND LAYOUT



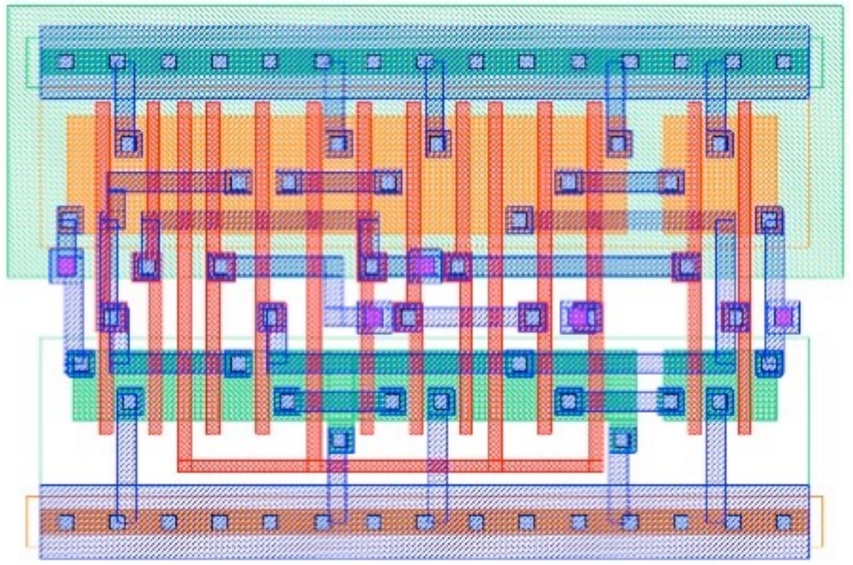


Motorola 6809 NMOs

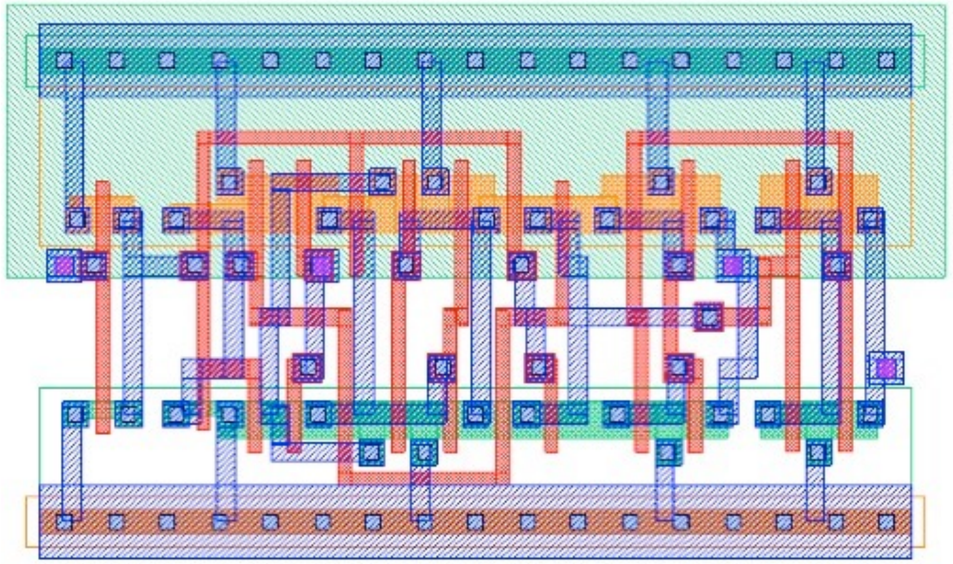
ASTRAN Layouts



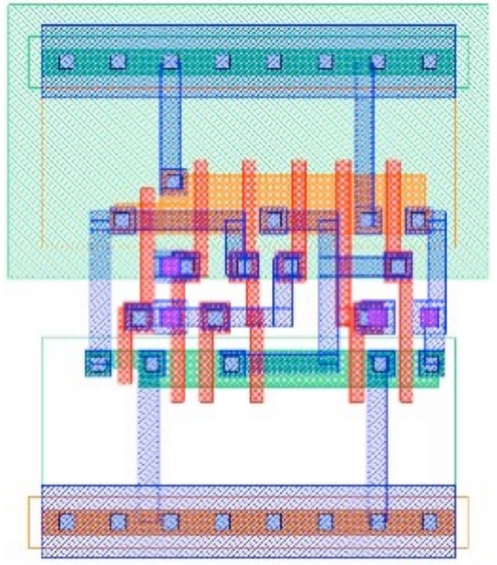
ADD22



ADD32

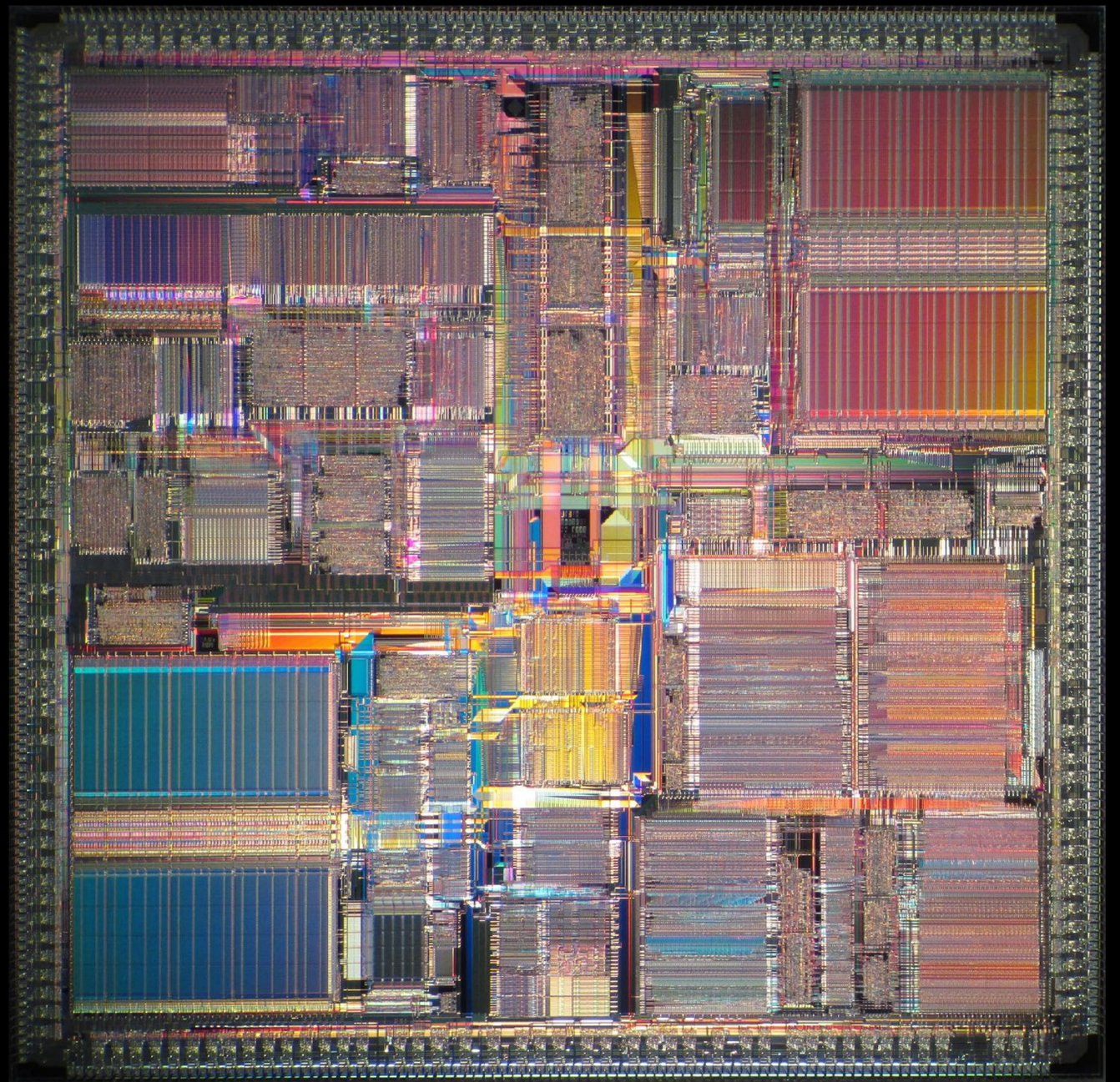


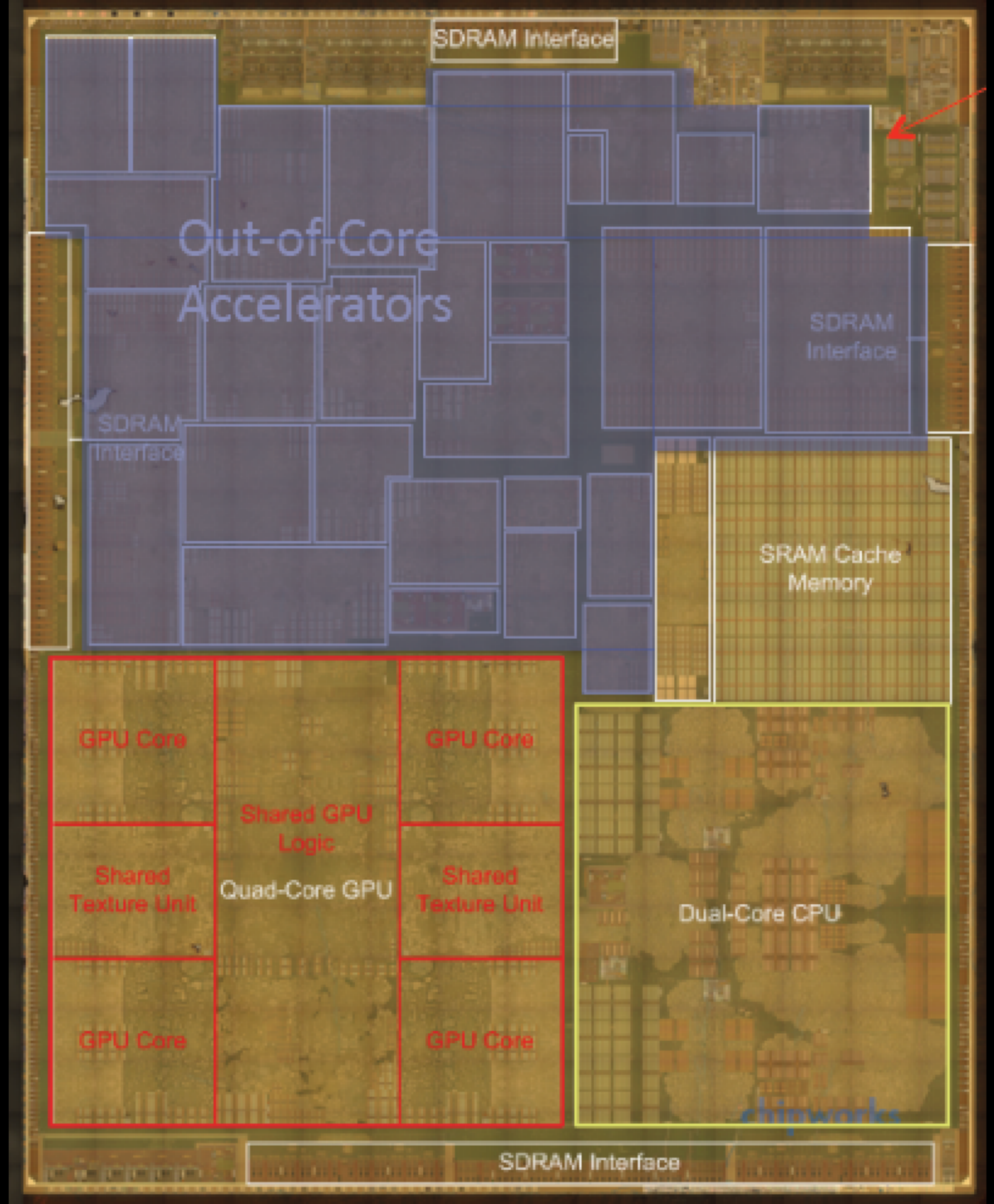
DF1



MUX21

Sun Super Sparc 2



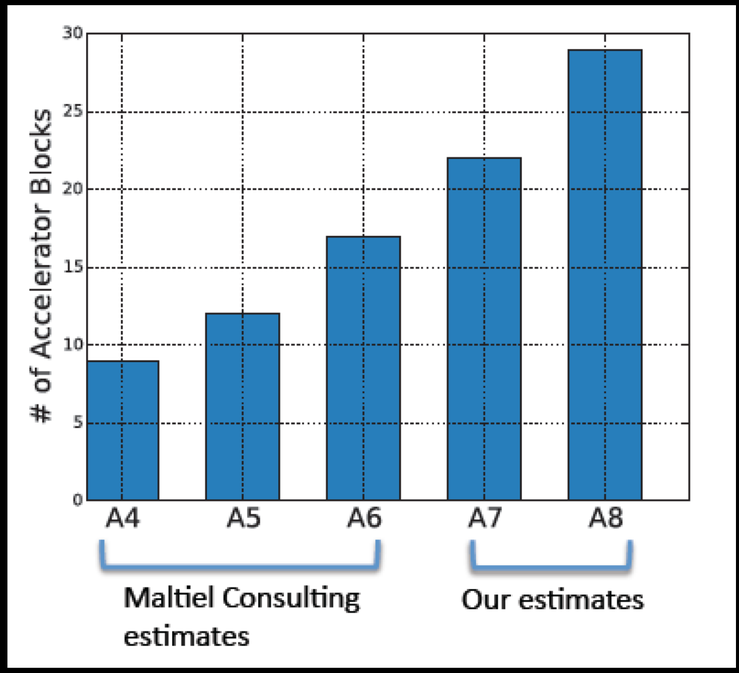


APPLE8

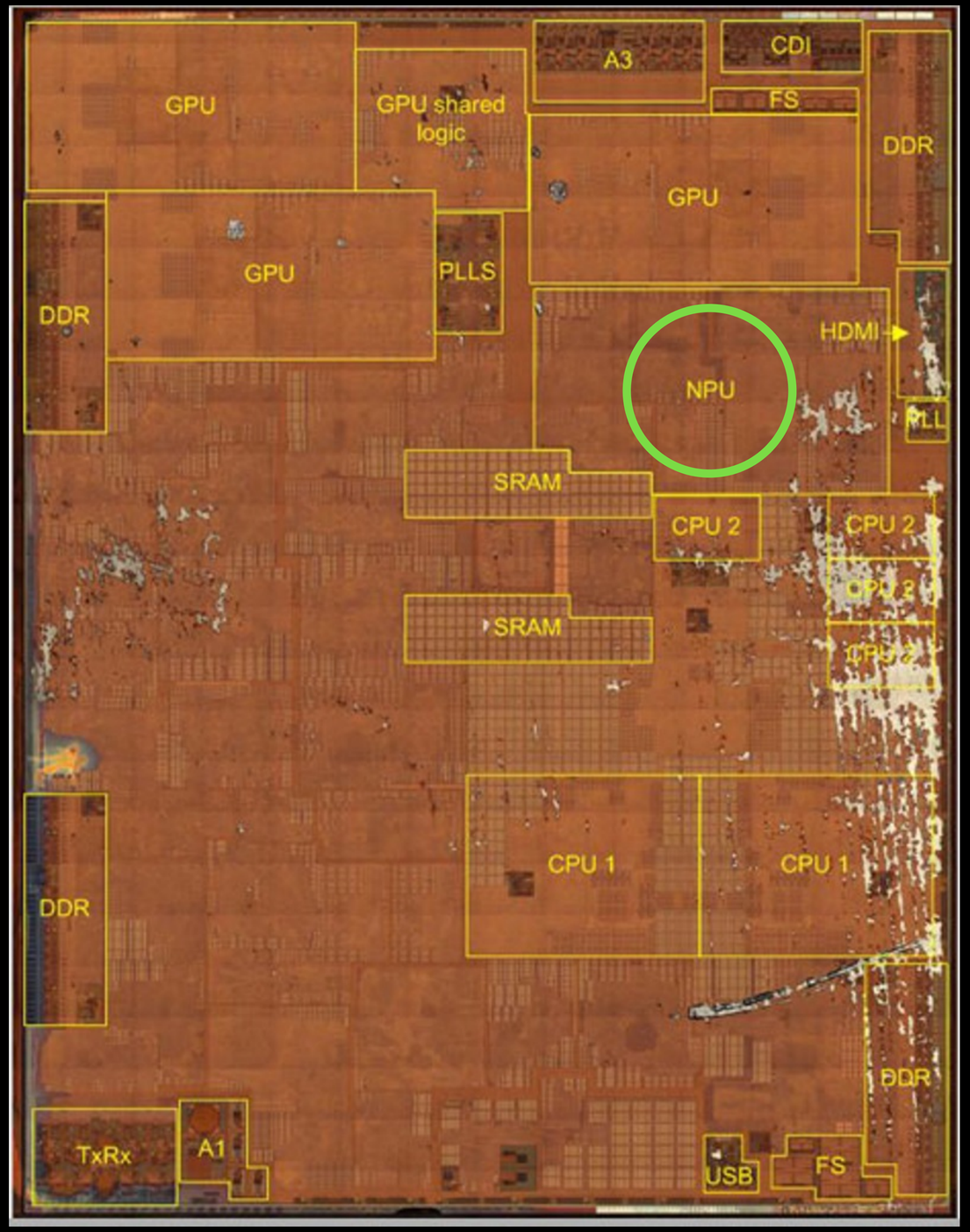
2 Billions of transistors

TSMC 20 nm

89 mm²



FromDavidBrooks,Harvard,2014



APPLE I I

4.3 Billions of transistors

TSMC 10 nm

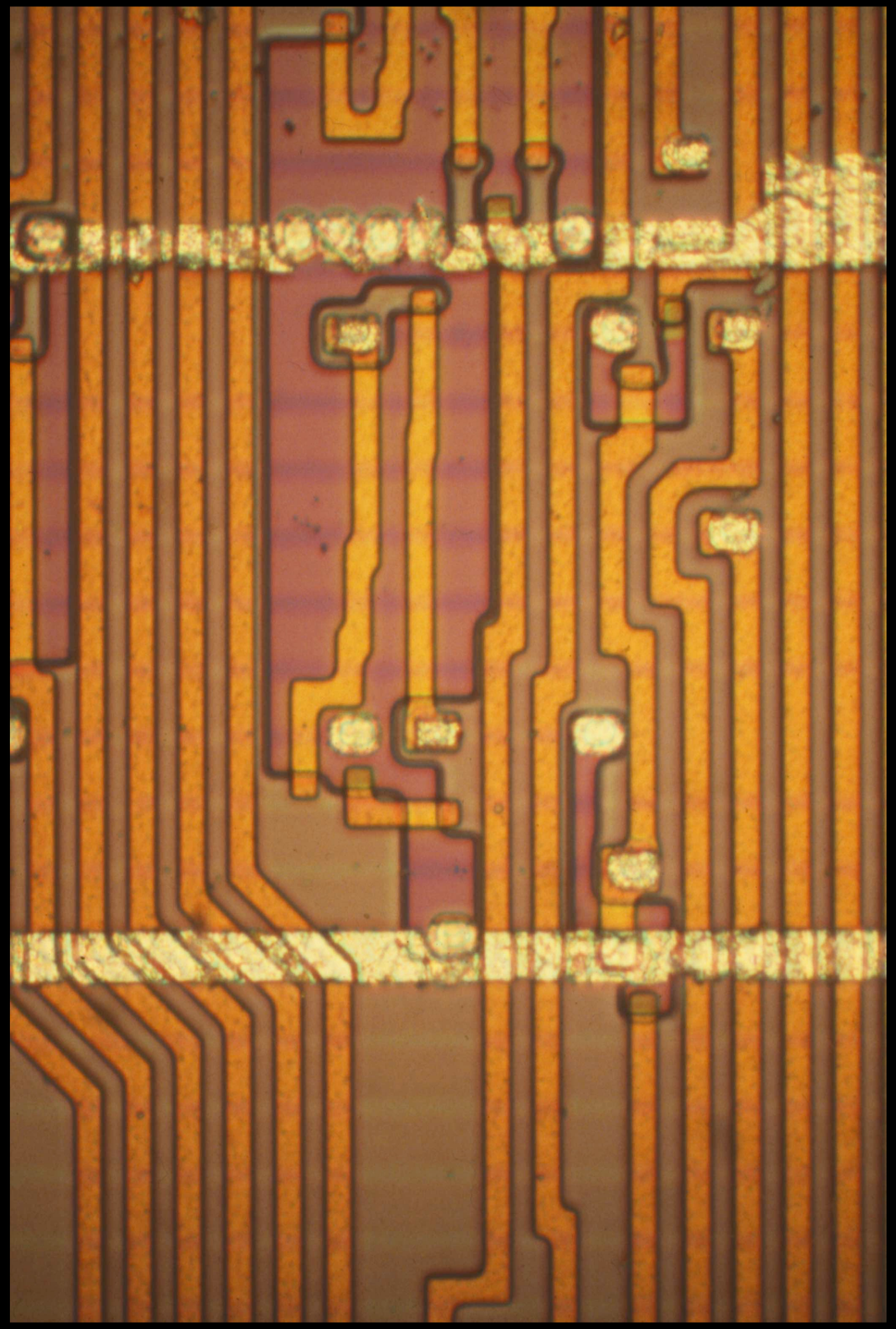
87,66 mm²

NPU- Neural Processing Unit

The neural network hardware can perform up to 600 billion operations per second

6 CPUs
3 GPU

And lots of Hardware Accelerators

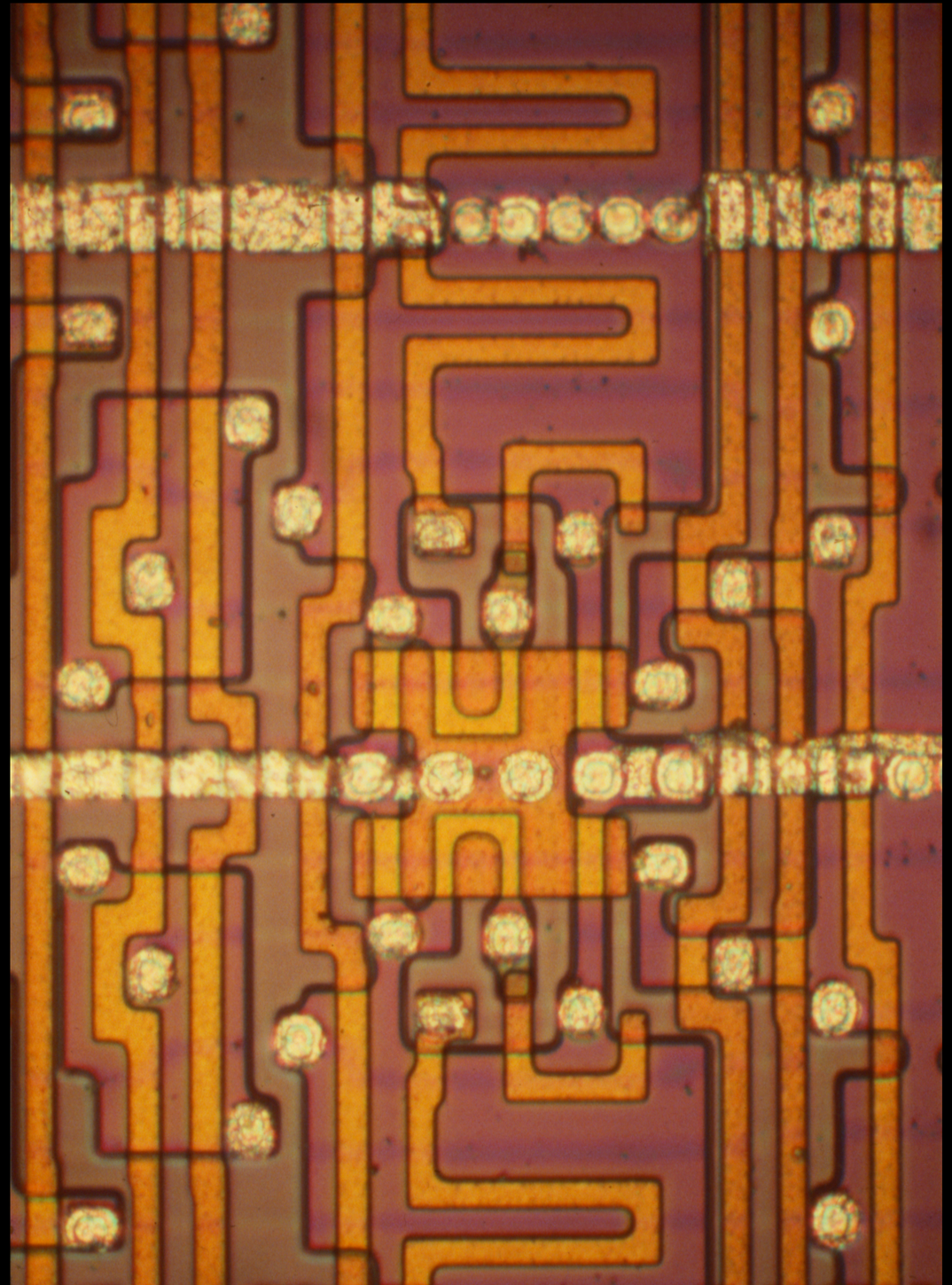


M6809

Detail of the M6809. The orange lines (polysilicon) crossing a wine/purple zone (diffusion) defines the channel of a transistor. The technology used was a NMOS.

The metal layer was taken out before doing the photo, but it still remains metal spots in the contact locations and the metals related to VCC and Ground lines.

by Ricardo Reis

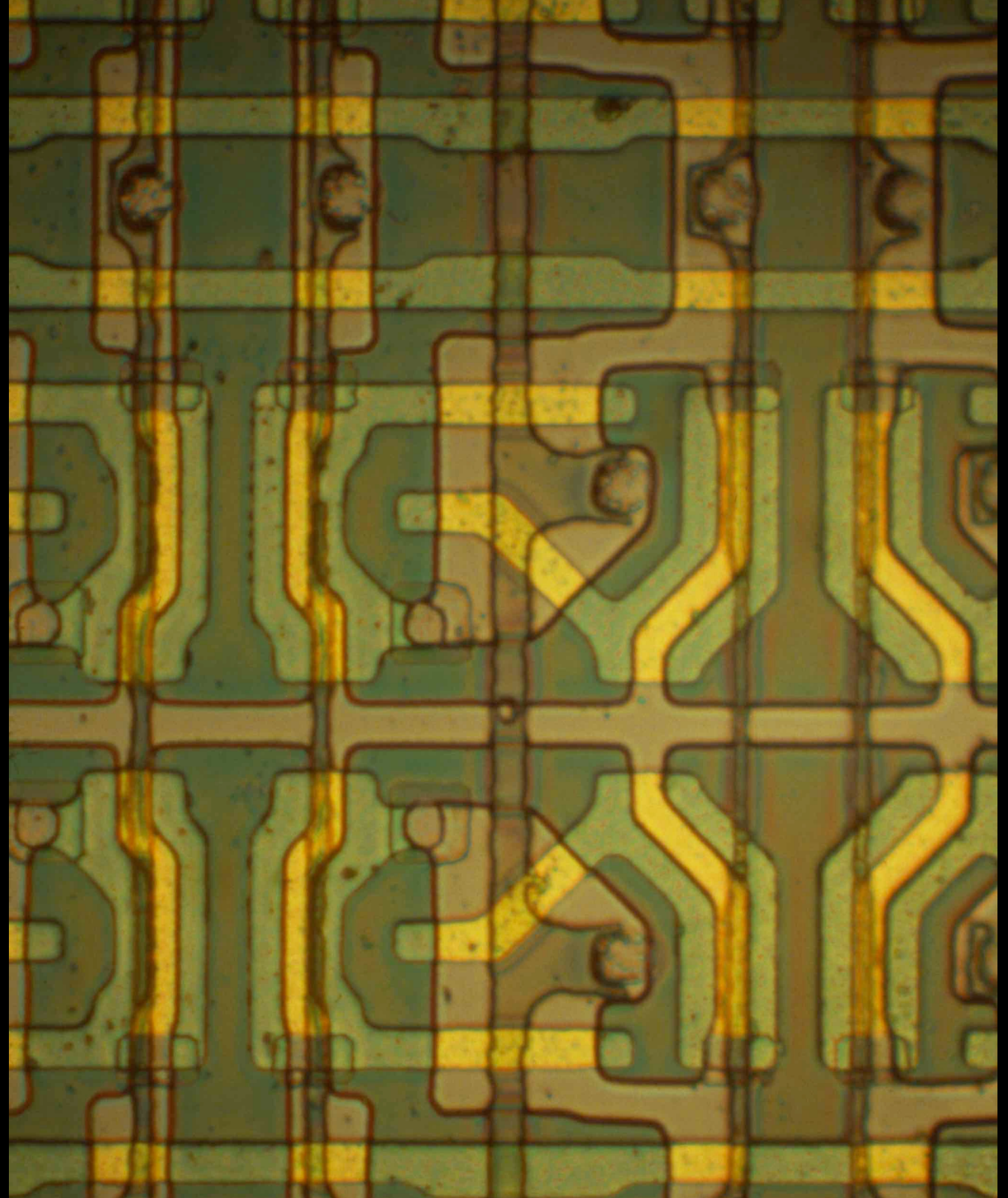


M6809

Detail of the M6809 Register File. Each memory cell has 6 transistors. The orange lines (polysilicon) crossing a wine/purple zone (diffusion) defines the channel of a transistor. The technology used was a NMOS with charge transistors connected to VDD.

The metal layer was taken out before doing the photo, but it still remains metal spots in the contact locations and the metals related to VCC and Ground lines.

by Ricardo Reis

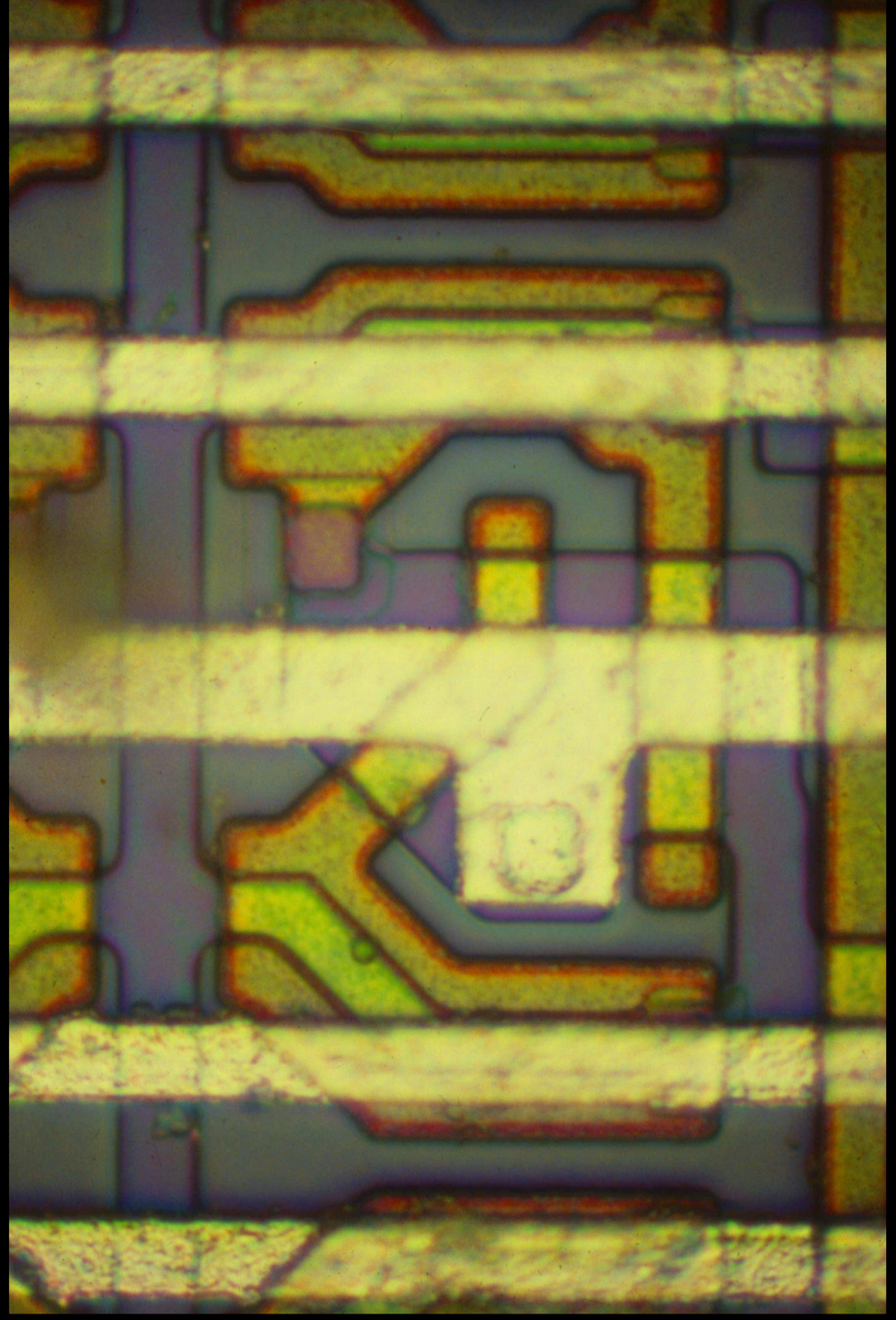


Z80

A detail of the Z80 Register File. Each Memory Cell has 6 Transistors (two of them to do the connection with each one of the data lines).
Each row corresponds to a Register.
The yellow line (Polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor.

The metal layer was taken out before doing the photo.

by Ricardo Reis



Z80

A detail of the Z80 Register File. Each Memory Cell has 6 Transistors (two of them to do the connection with each one of the data lines).

Each row corresponds to a Register.

The green line (Polysilicon) crossing a grey/violete zone (diffusion) defines the channel of a transistor.

by Ricardo Reis

Z8000

A detail of the Z8000 Register File. Each Memory Cell has 6 Transistors (two of them to do the connection with each one of the data lines).

Each column corresponds to a Register.

The metal layer was taken out before doing the photo.

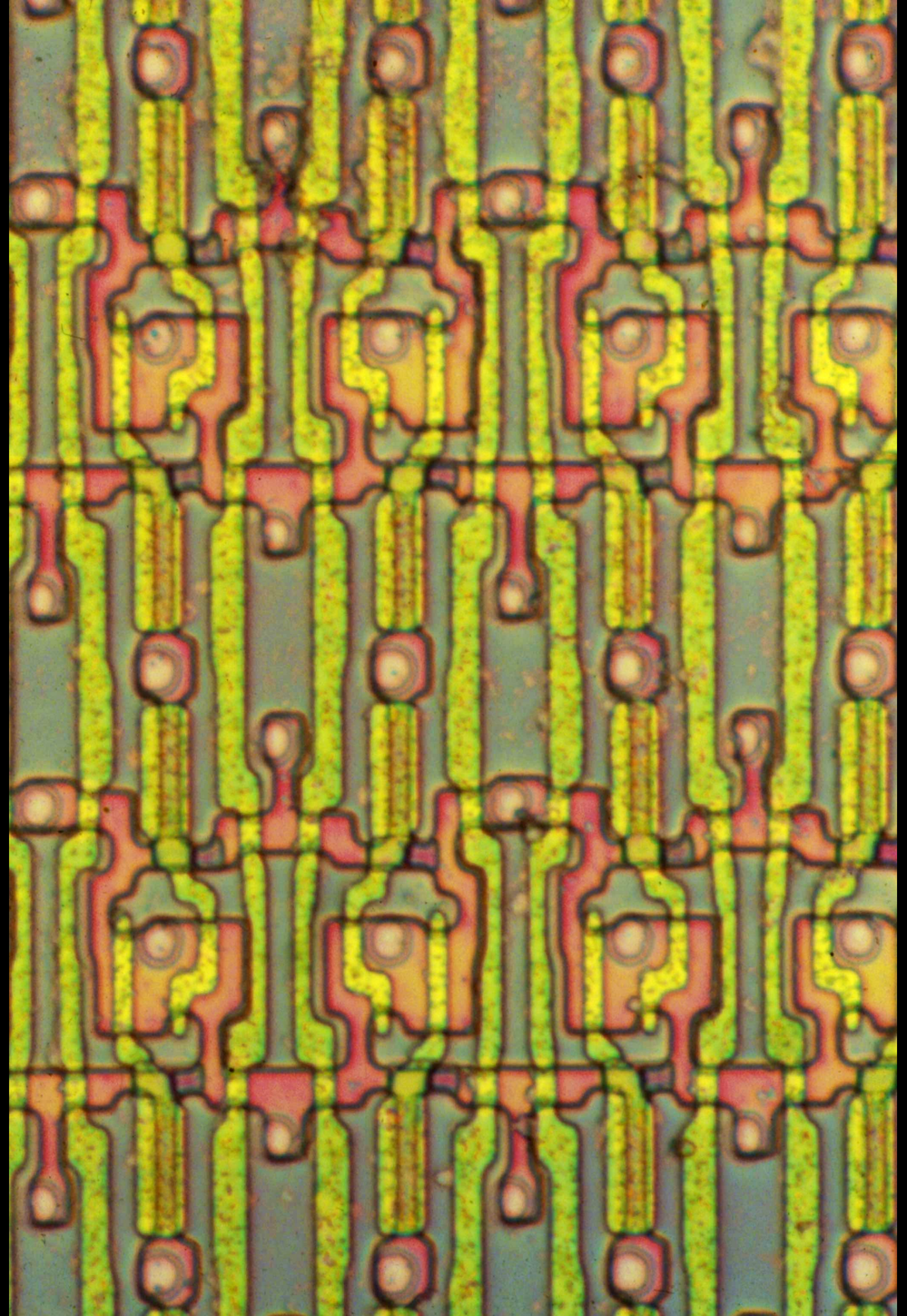
by Ricardo Reis

M68000

Detail of the M68000 Register File. The rose zones are diffusion ones. Polysilicon is mainly green. Substrate is grey. It is a NMOS one metal technology.

The metal layer was taken out before doing the photo.

by Ricardo Reis

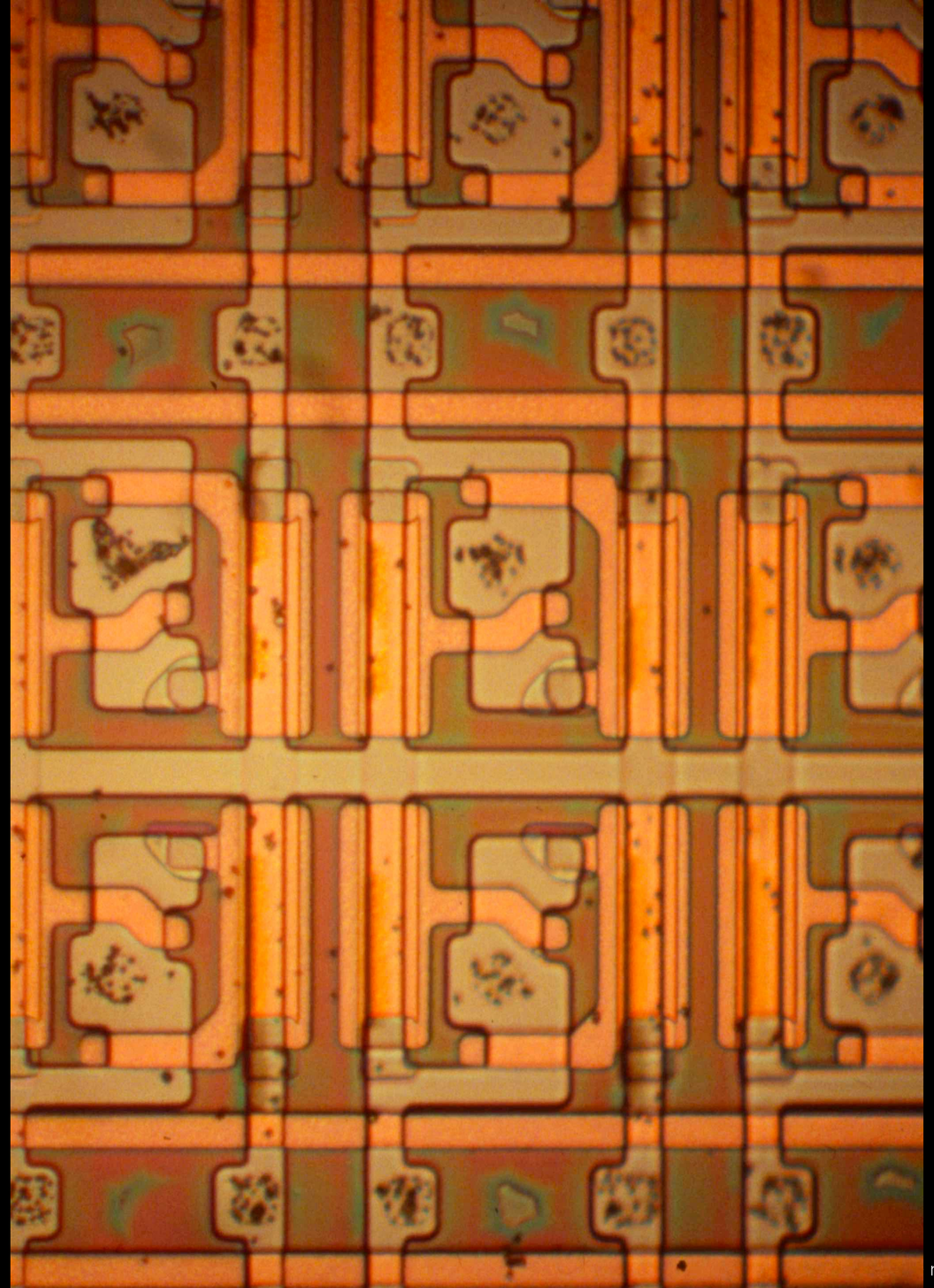


M68000

Detail of the M68000 Register File. The rose zones are diffusion ones. Polysilicon is mainly green. Substrate is grey. It is a NMOS one metal technology.

The metal layer was taken out before doing the photo. The round spots are the contacts with metal.

by Ricardo Reis

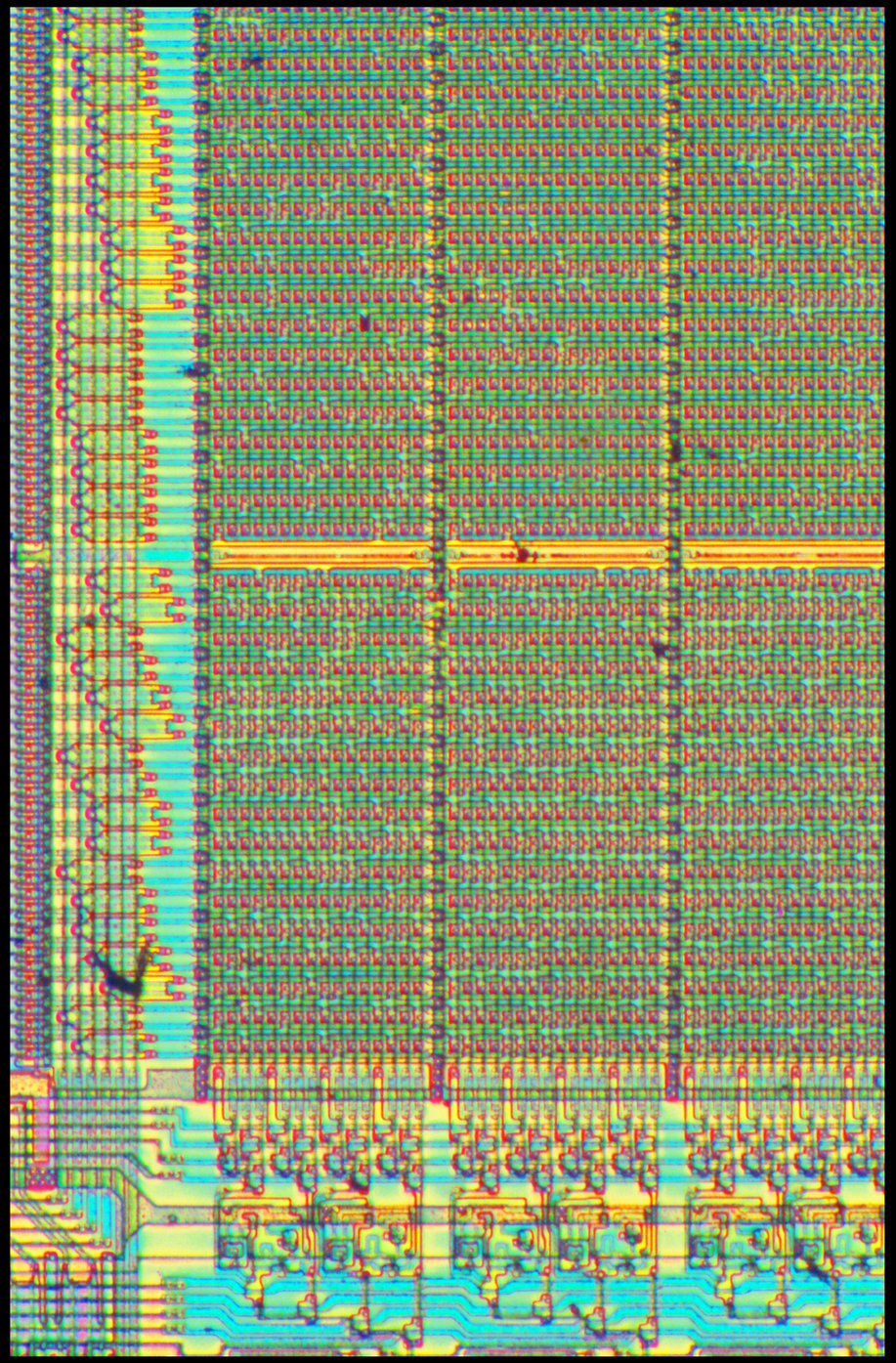


I8070

Detail of the I8070 Register File. Each memory cell has 6 transistors. The orange lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is brown. The technology used was a NMOS.

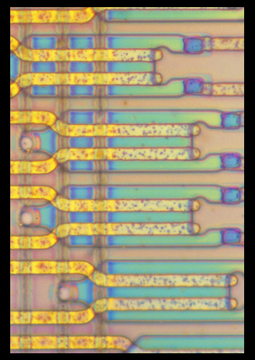
metal layer was taken out before doing the photo.

by Ricardo Reis



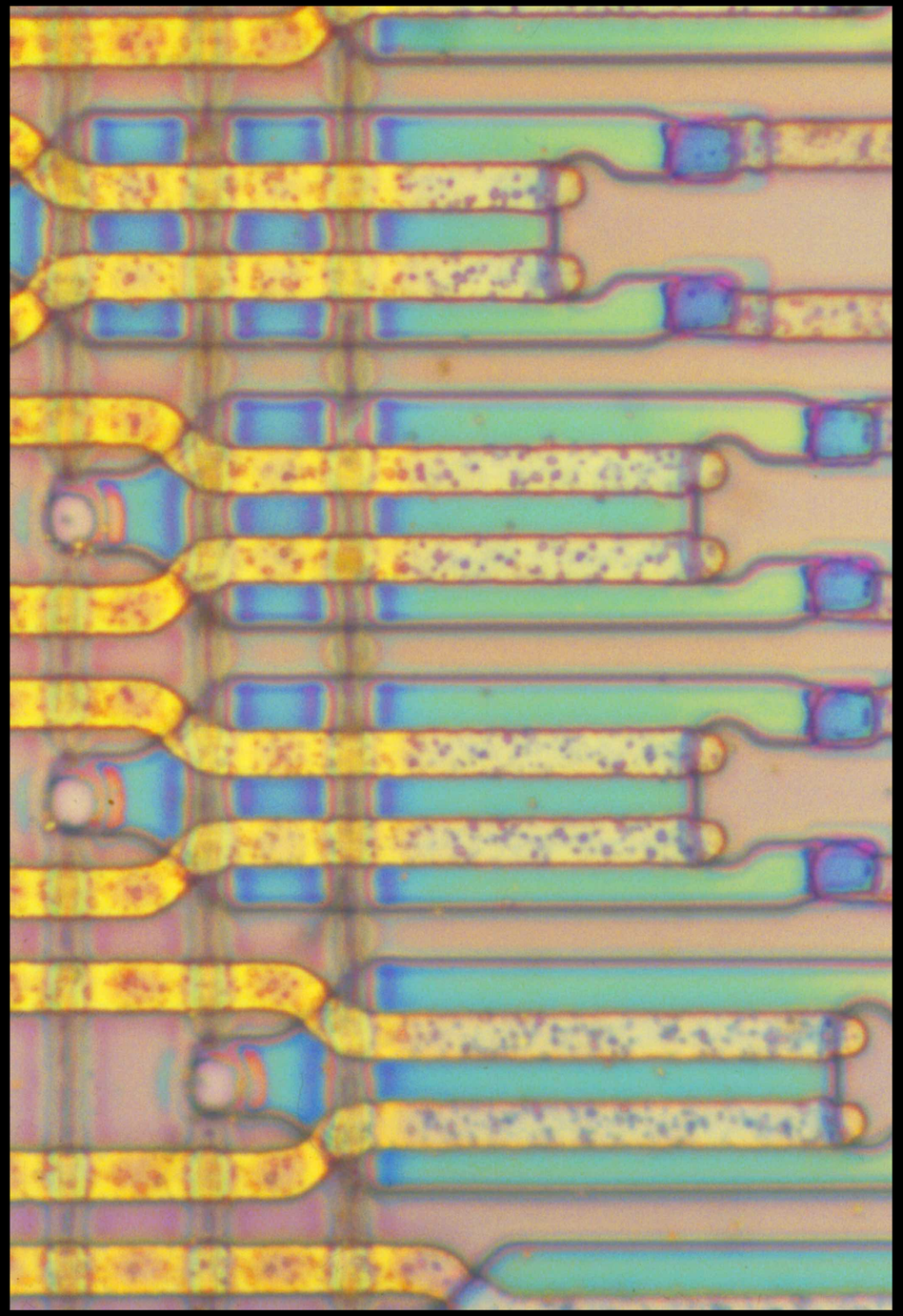
M68000

A detail of the M68000 ROM Memory. The column on the left is part of the line address decoder. The 3 main columns on the right are part of the right ROM Memory Bank. The circuits under these 3 columns are the multiplexors that do the bit selection.



The metal layer was taken out before doing the photo.

by Ricardo Reis

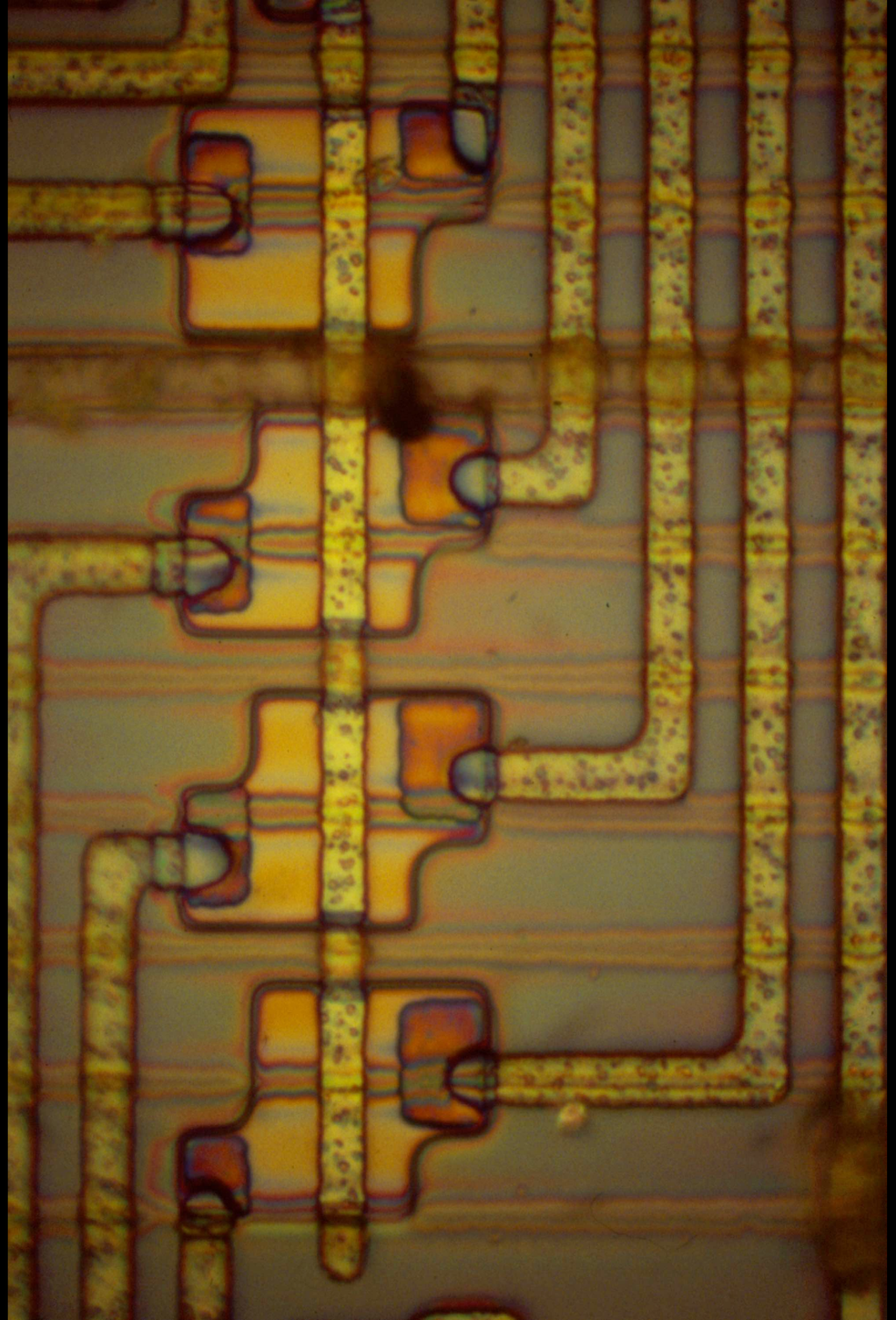


M68000

Detail of the M68000 ROM Memory Line Decoder. The yellow line (polysilicon) crossing a Blue/Turquoise zone (diffusion) defines the channel of a transistor. The dark blue spots correspond to the diffusion/polysilicon contacts.

The metal layer was taken out before doing the photo.

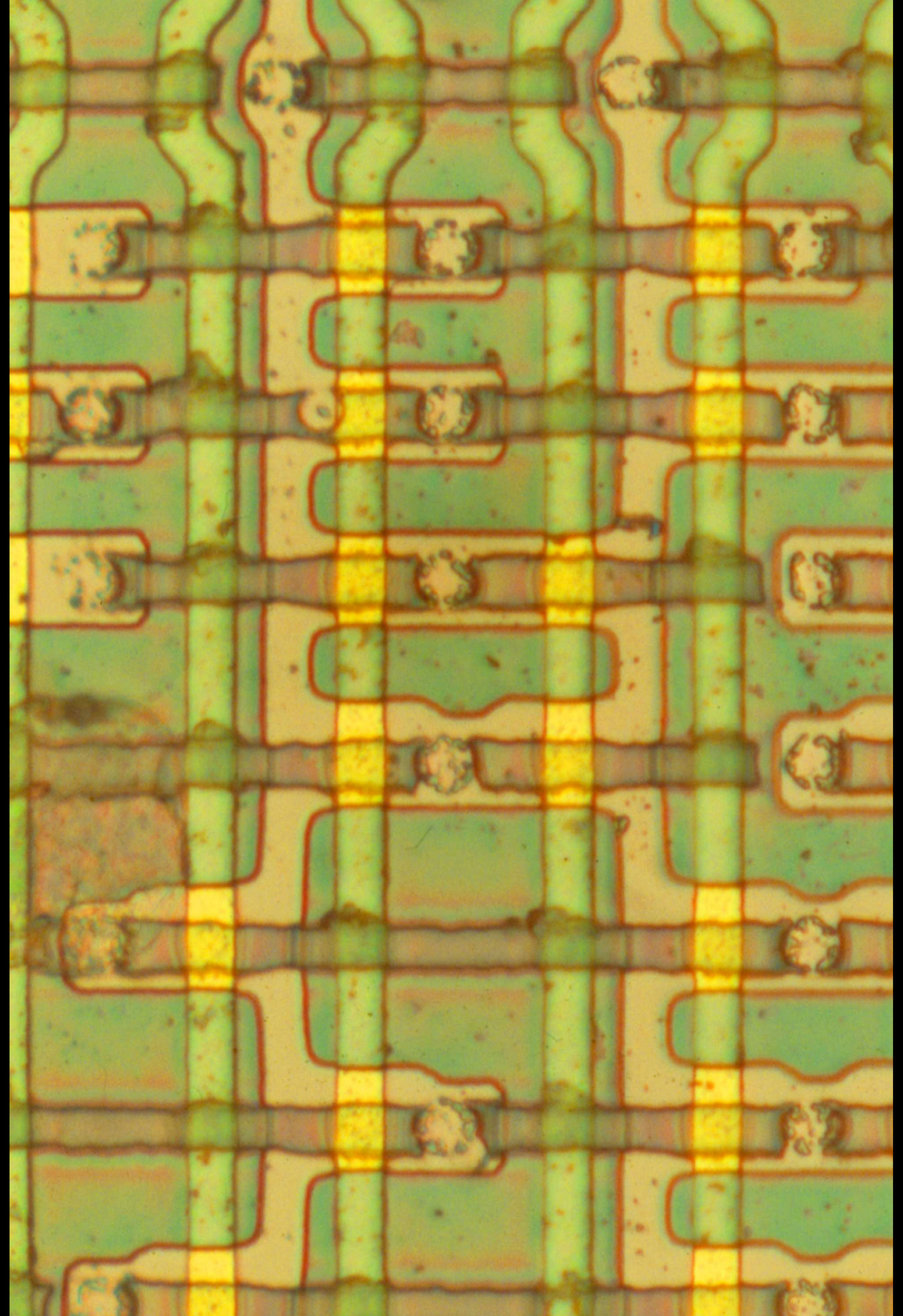
by Ricardo Reis



M68000

Detail of the M68000. The orange zones are diffusion ones. Polysilicon is mainly green. Substrate is grey.

by Ricardo Reis

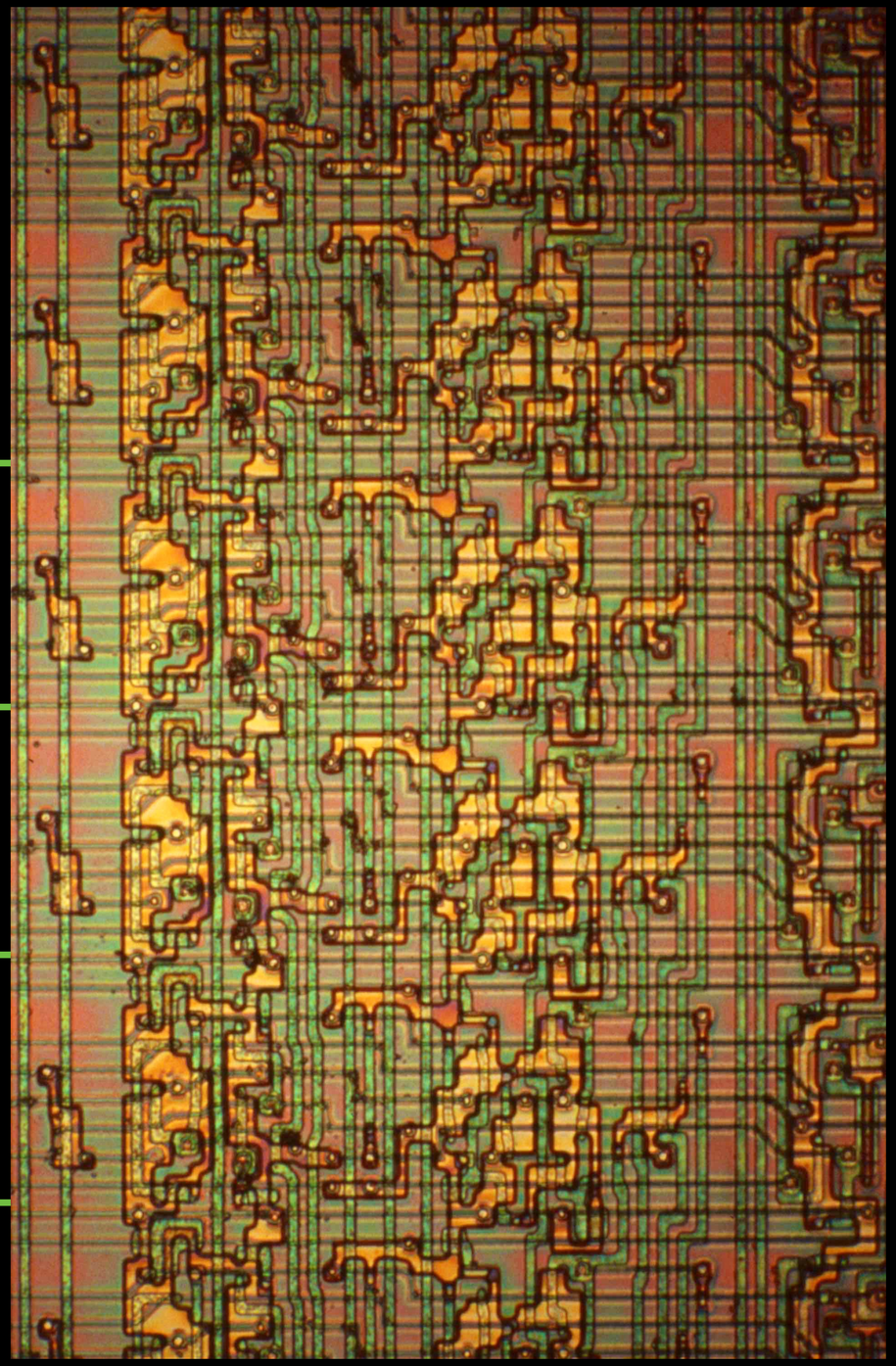


Z80

A detail of the Z80 PLA. The light grey zones are diffusion ones. Polysilicon is mainly green/ yellow (vertical lines). It is a NMOS one metal technology.

The metal layer was taken out before doing the photo. Some brown lines (horizontal ones) are silicon oxide that were under the metal lines. With this it is possible to know where the metal lines were.

by Ricardo Reis

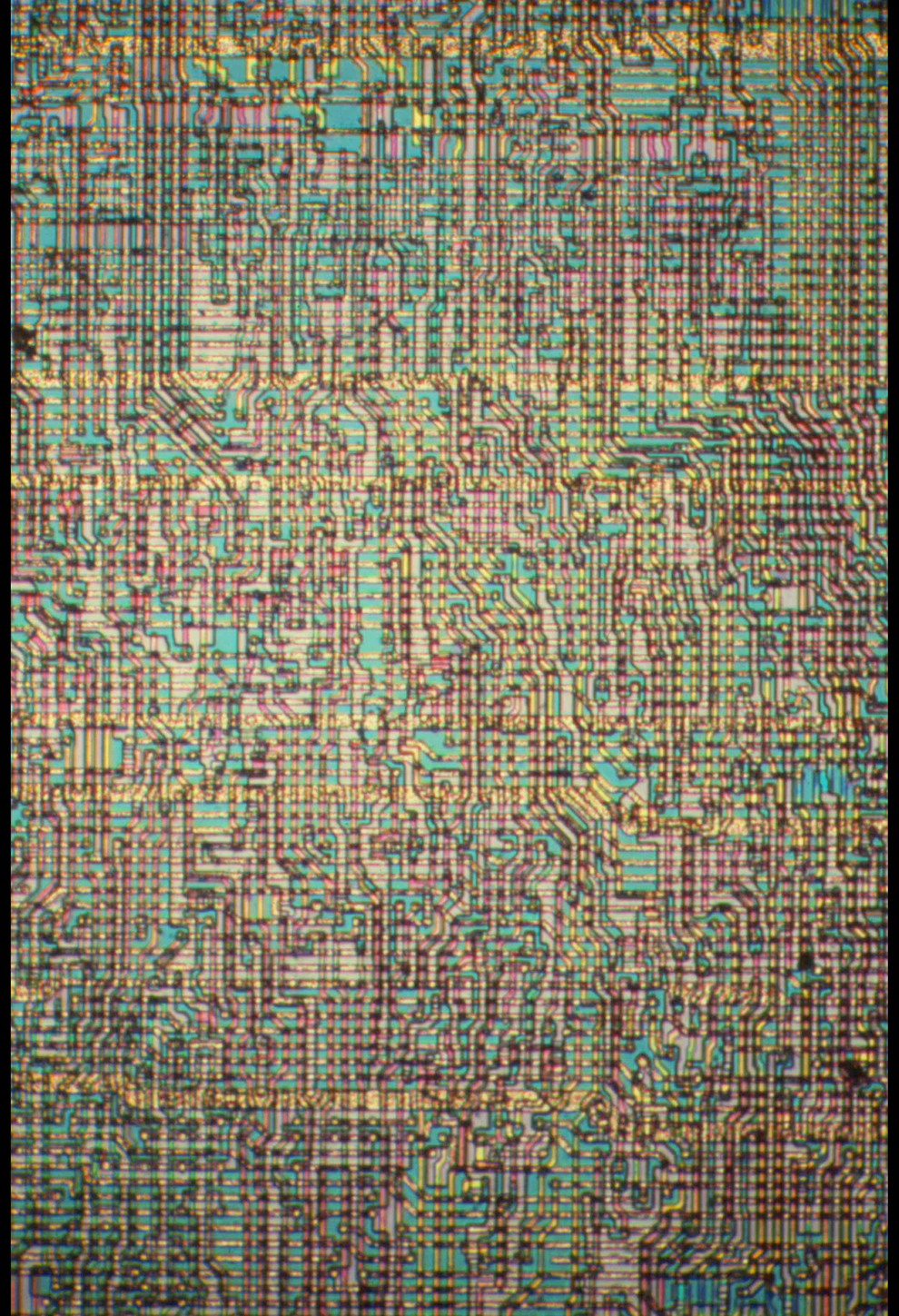


M68000

Detail of the M68000 Data Path. A set of 5 pass transistors can be seen on the left column. Each one of these pass transistor is in a data path bit slice. The orange zones are diffusion ones. Polysilicon is mainly green.

The metal layer was taken out before doing the photo.

by Ricardo Reis



Z8000

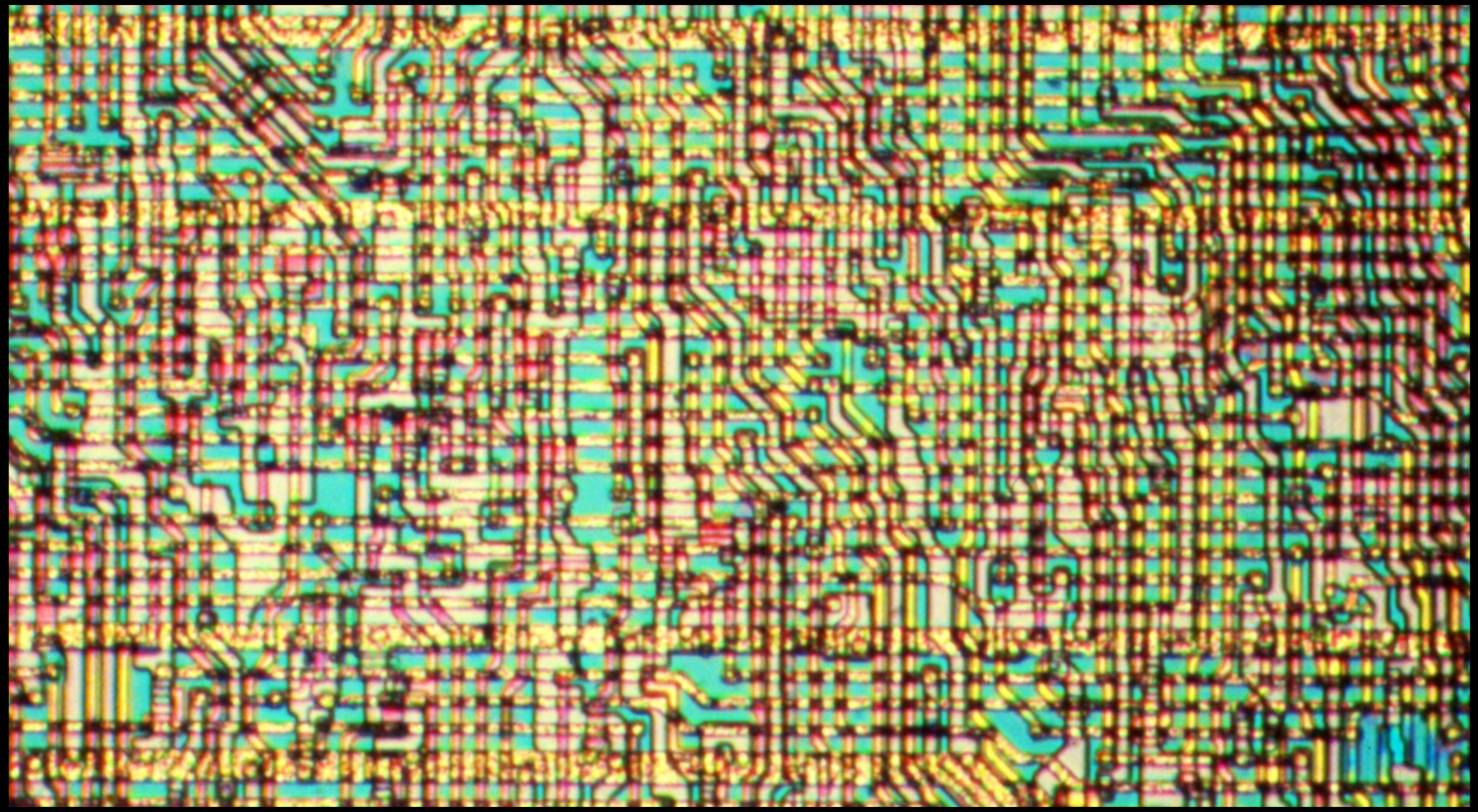
Detail of the Z8000 control part in random logic. The rose/green lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is green.

The metal layer was taken out before doing the photo.

by Ricardo Reis

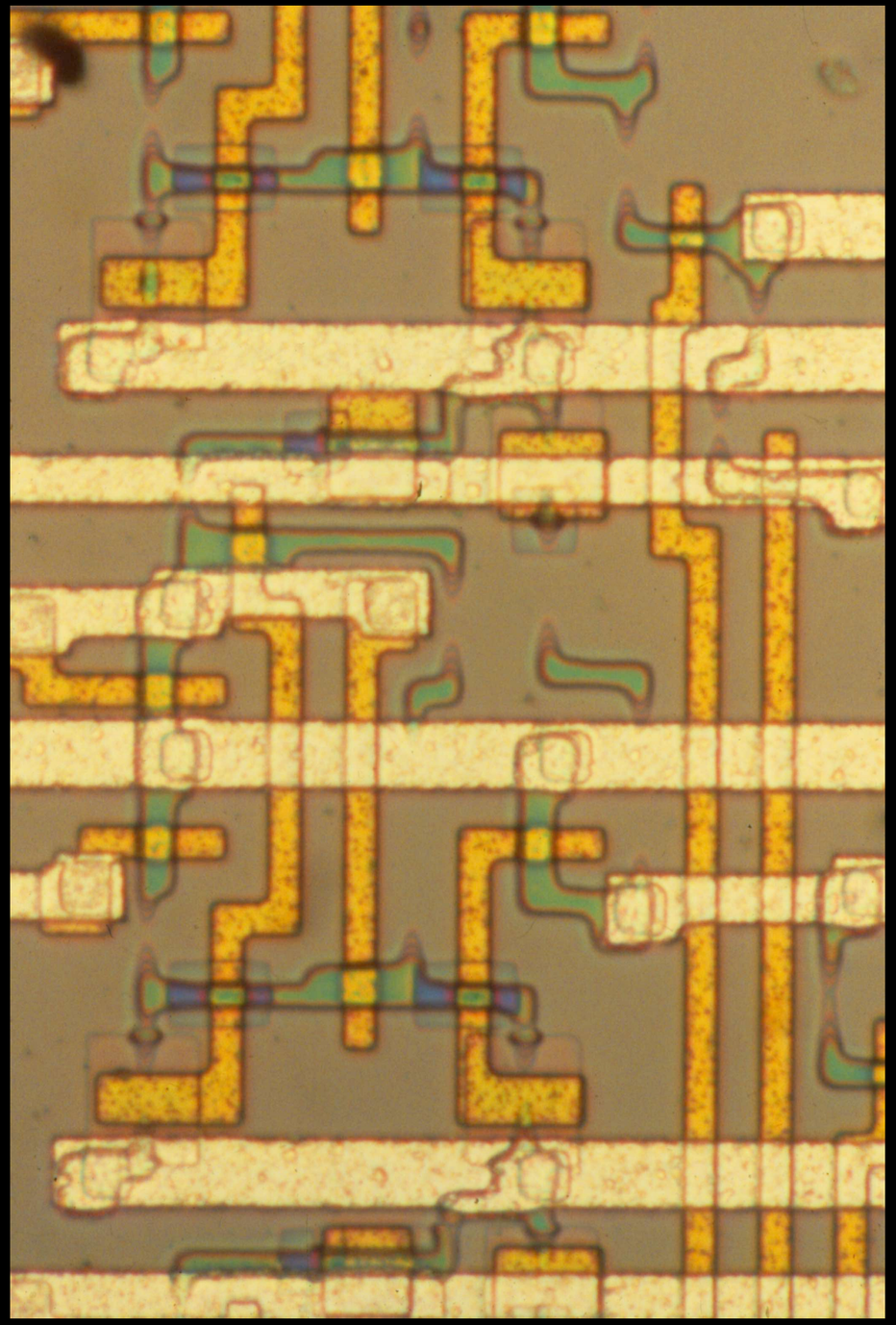
Z8000

Detail of the Z8000 control part in random logic. The rose/green lines (polysilicon) crossing a grey zone (diffusion) defines the channel of a transistor. Substrate is dark green.



The metal layer was taken out before doing the photo.

by Ricardo Reis



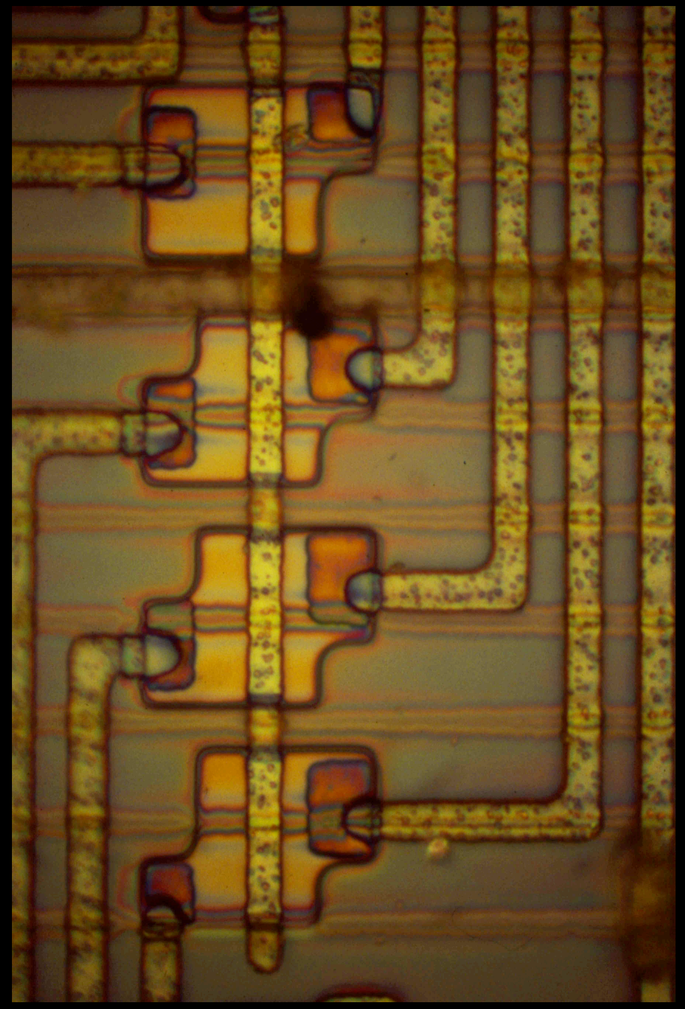
Process Fail

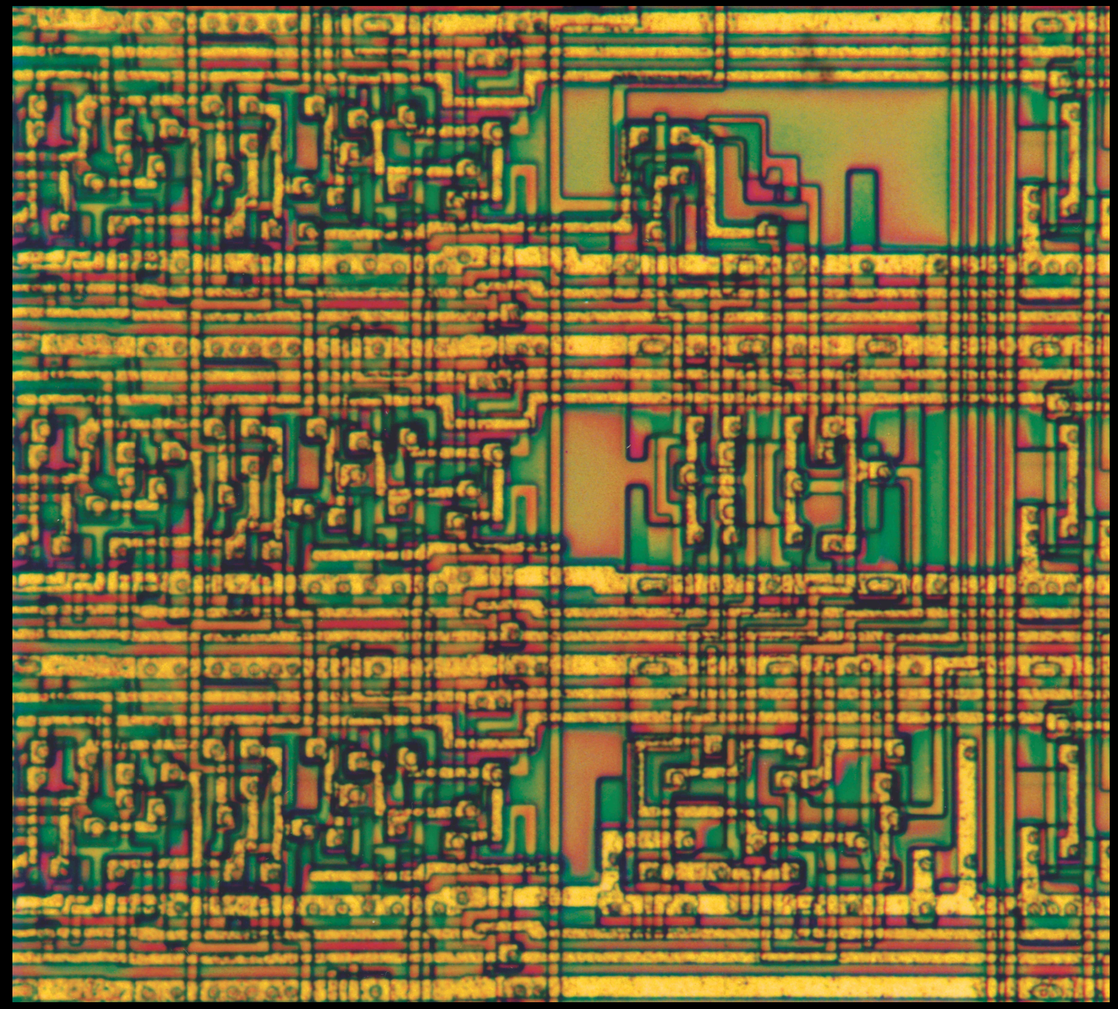
This MOS technology process had a fail in the diffusion step. The diffusion lines are the green ones. It is possible to identify the big interruptions in the diffusion zones. Yellow is polysilicon and white lines are the metal ones.

by Ricardo Reis

DAC ART SHOW 2018

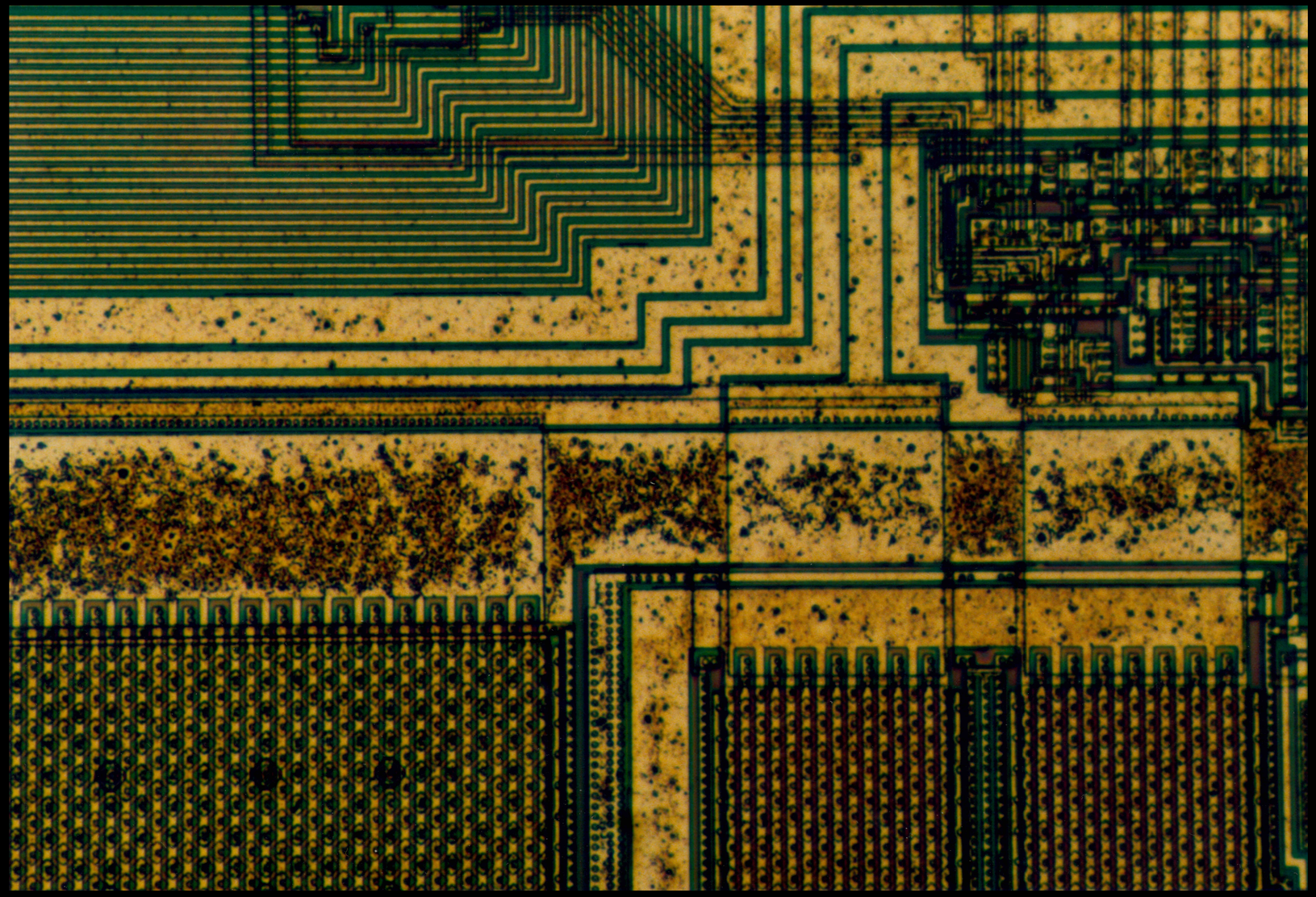
São Francisco, USA, 24 a 28 de Junho





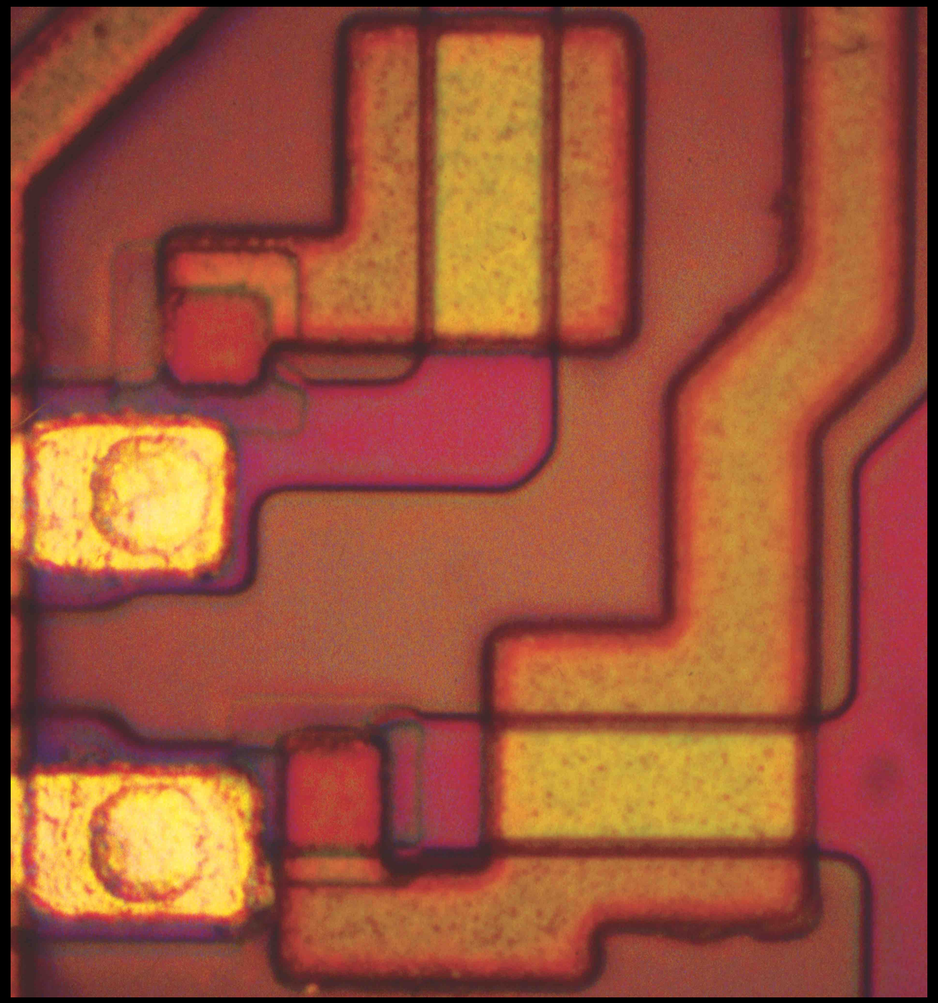
DAC ART SHOW 2018

São Francisco, USA, 24 a 28 de Junho



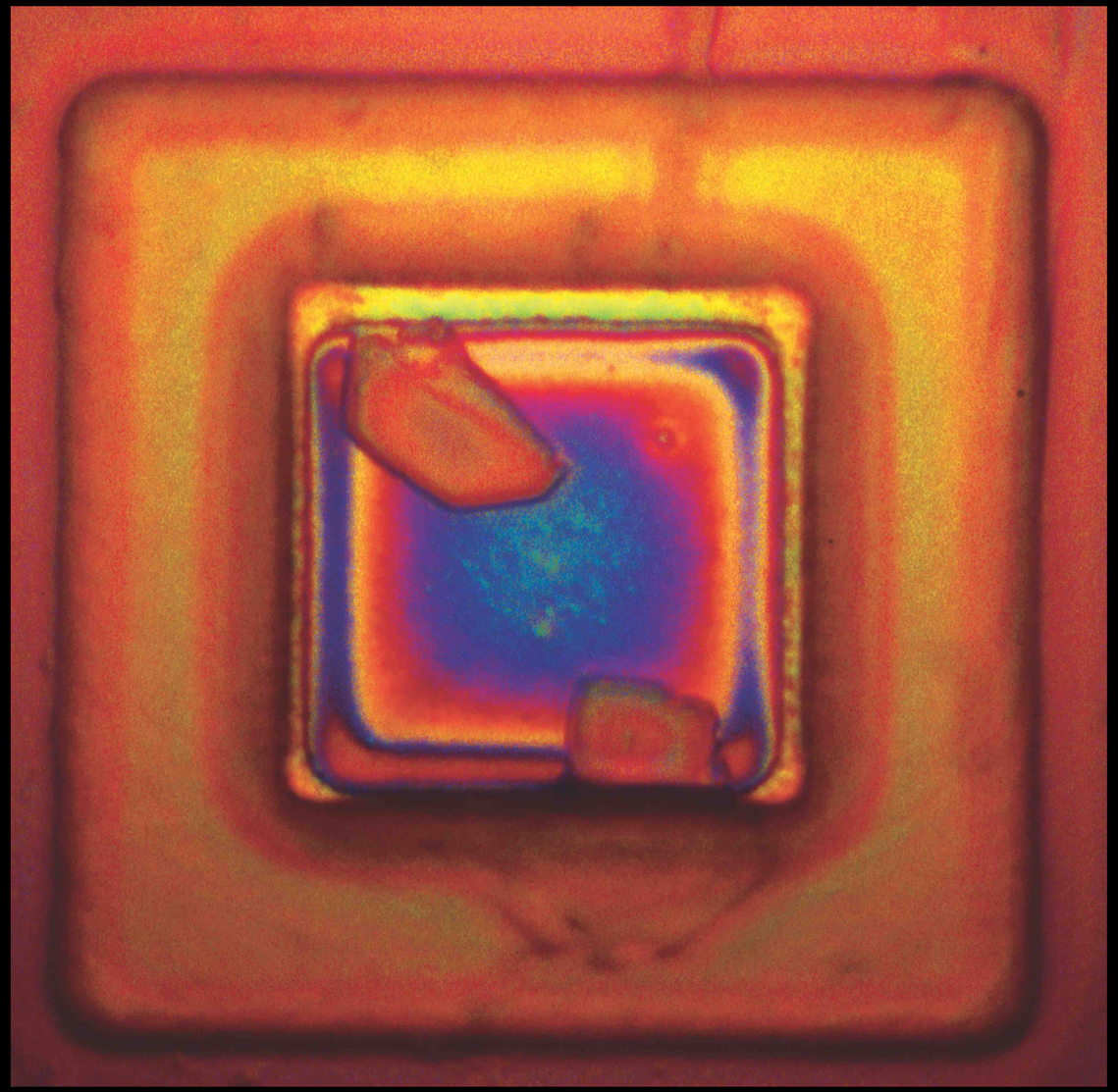
DAC ART SHOW 2018

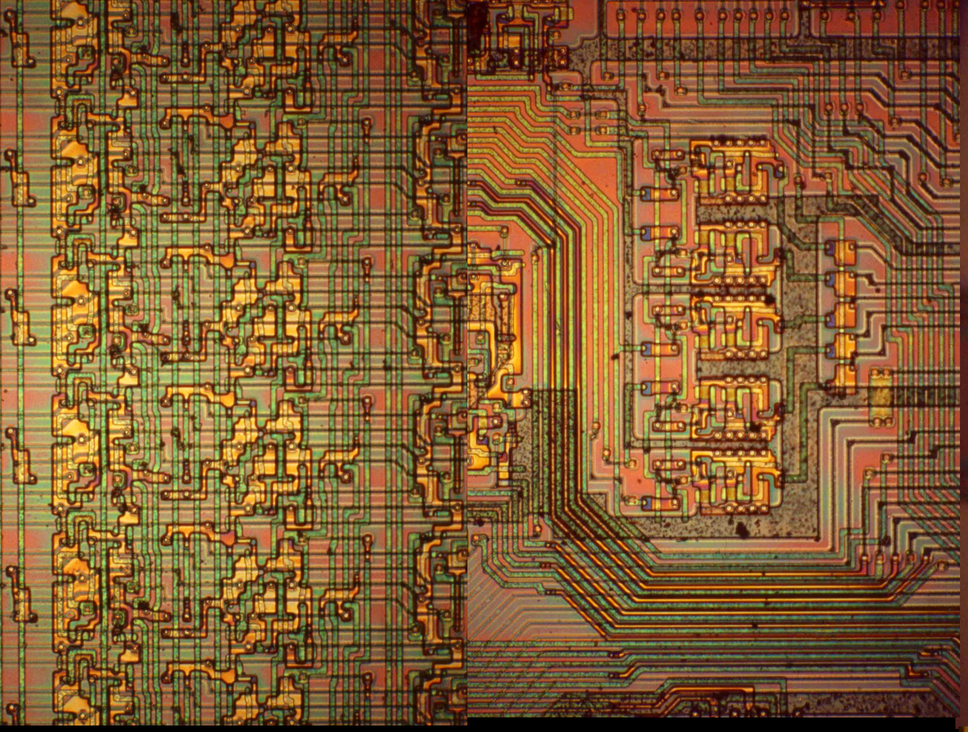
São Francisco, USA, 24 a 28 de Junho

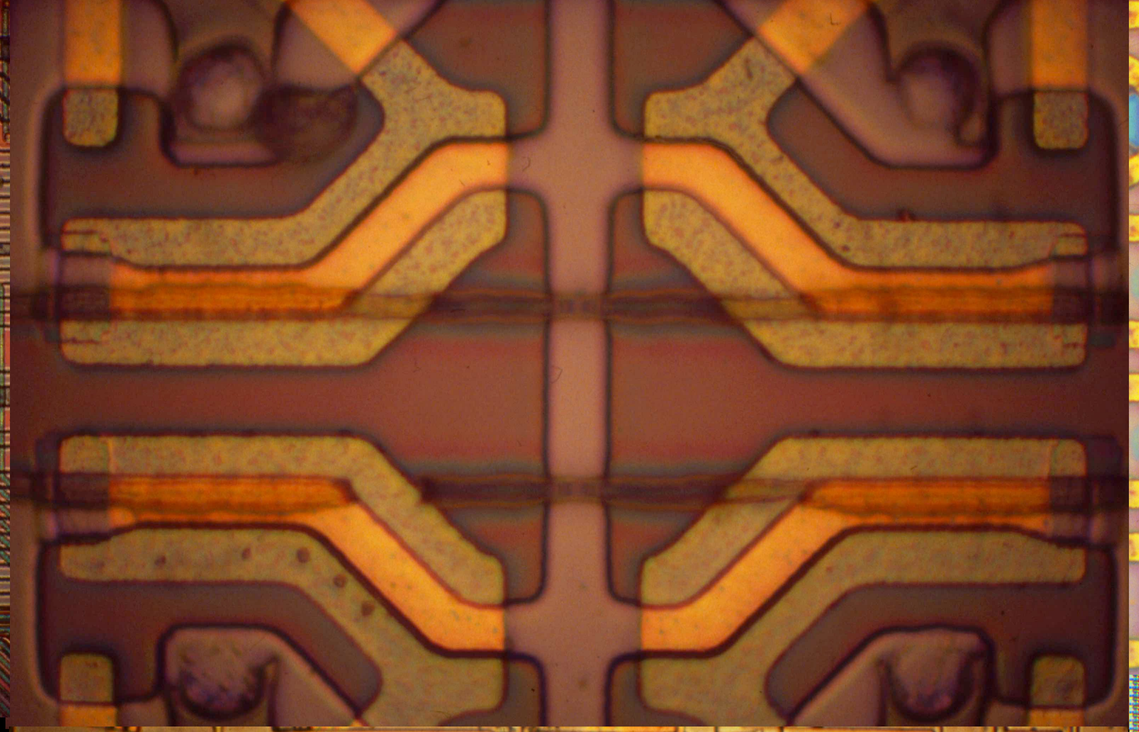


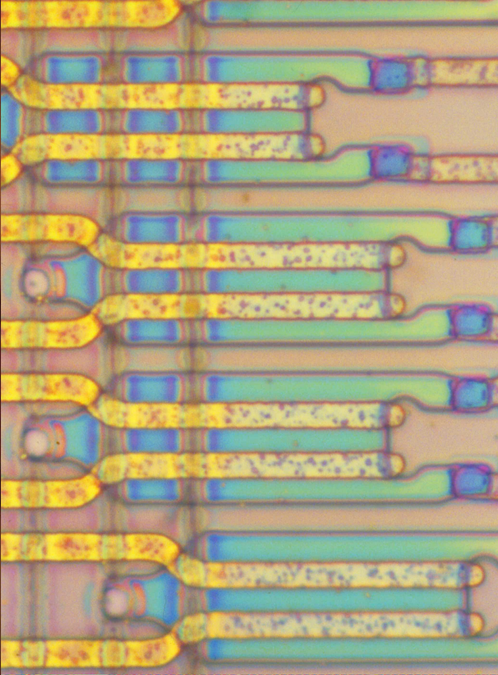
DAC ART SHOW 2018

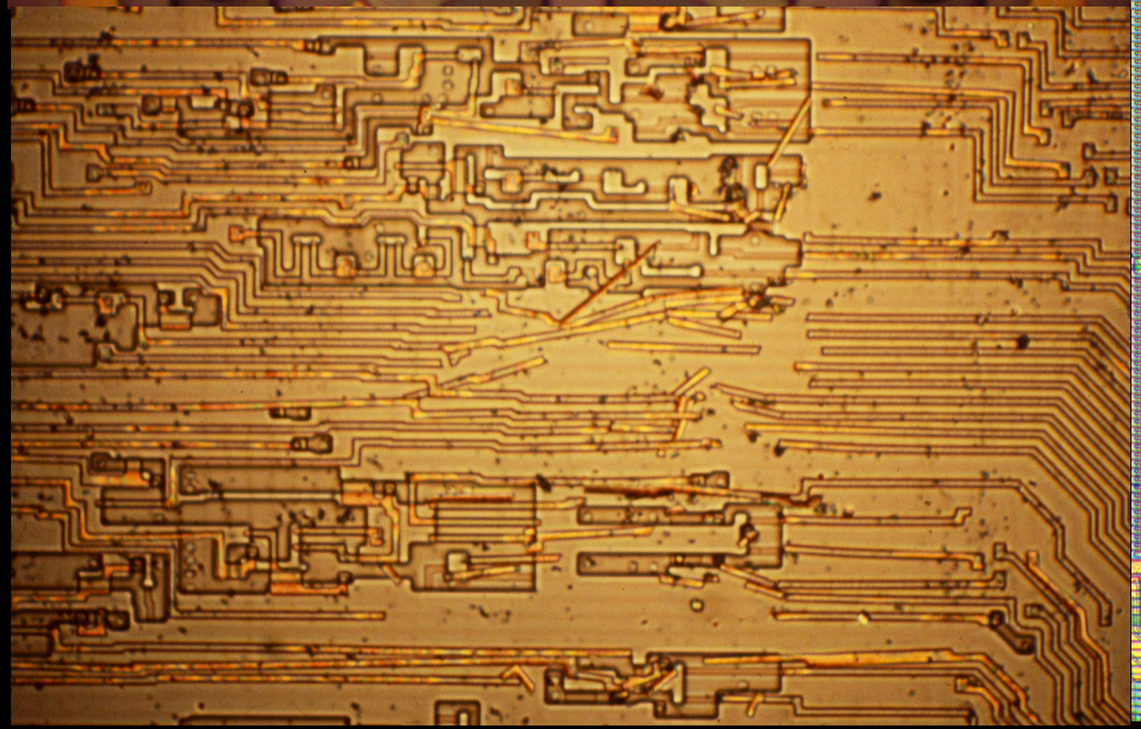
São Francisco, USA, 24 a 28 de Junho

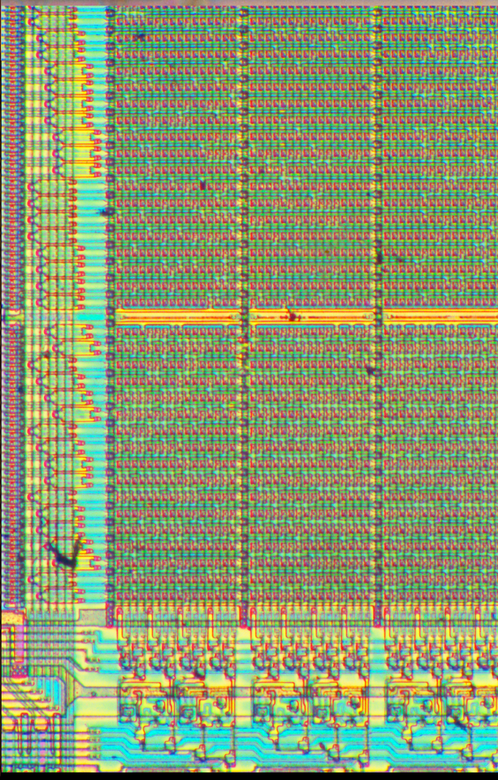








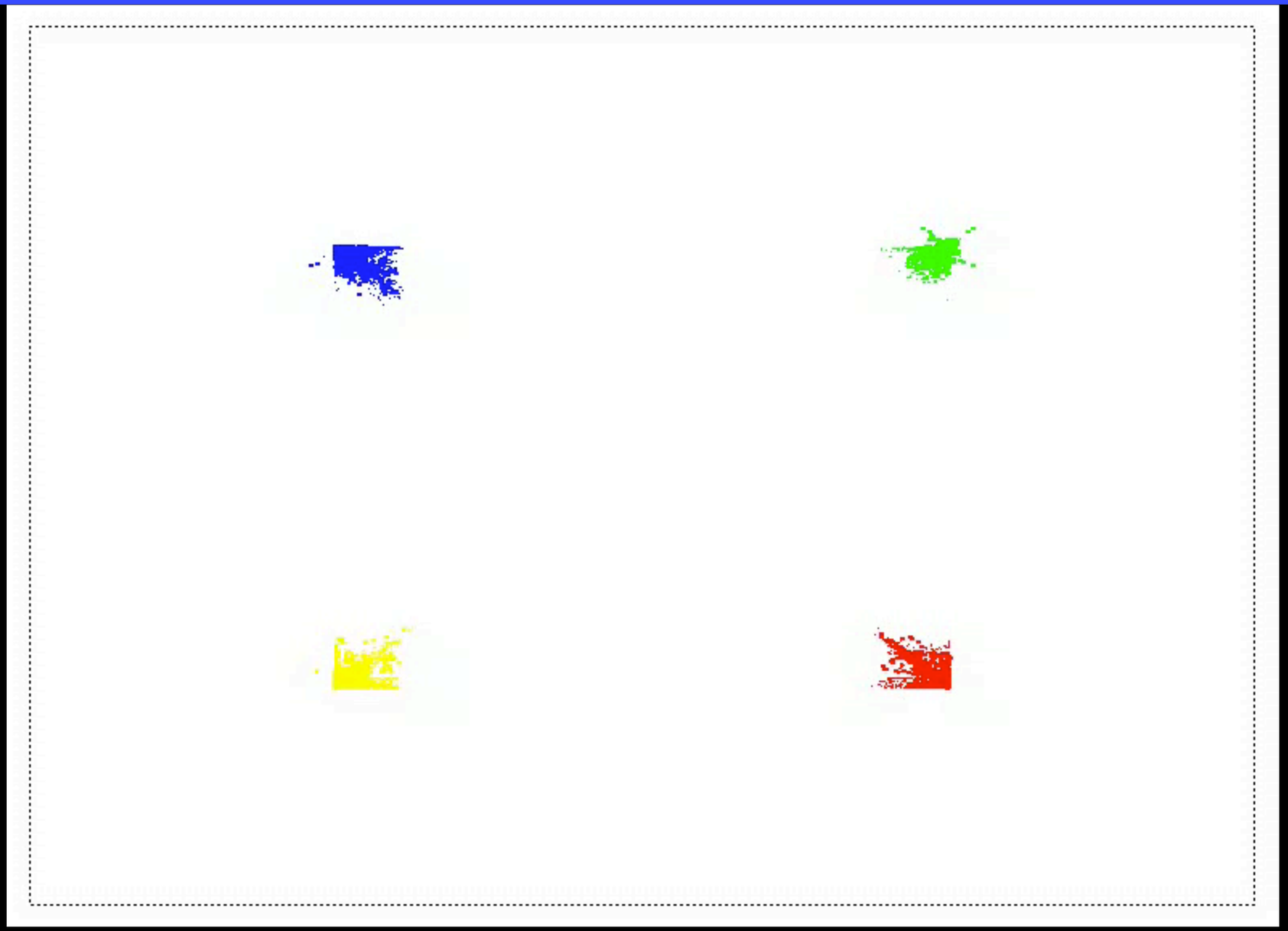




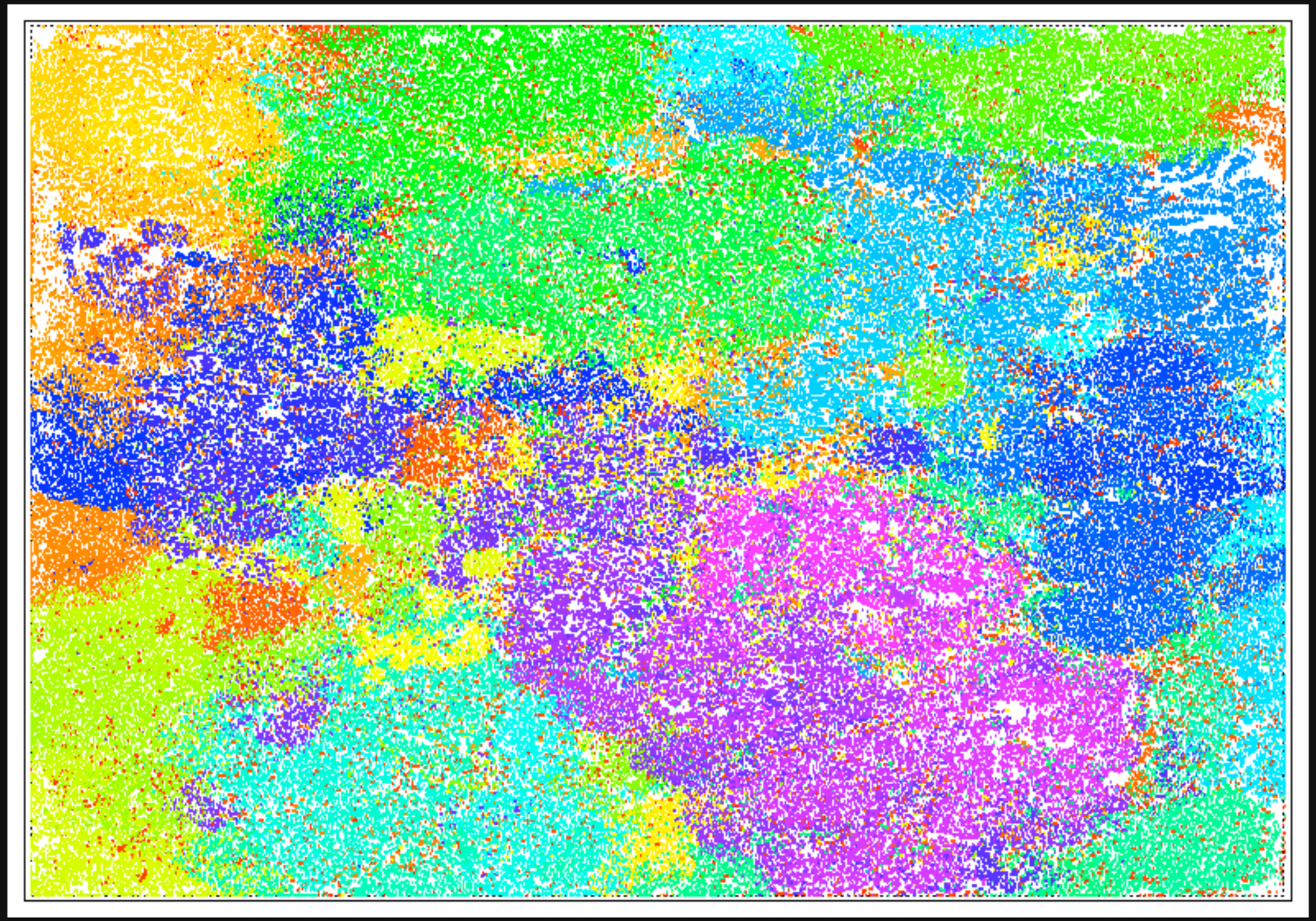
more photos at:
facebook.com/artchips1

Ricardo Reis

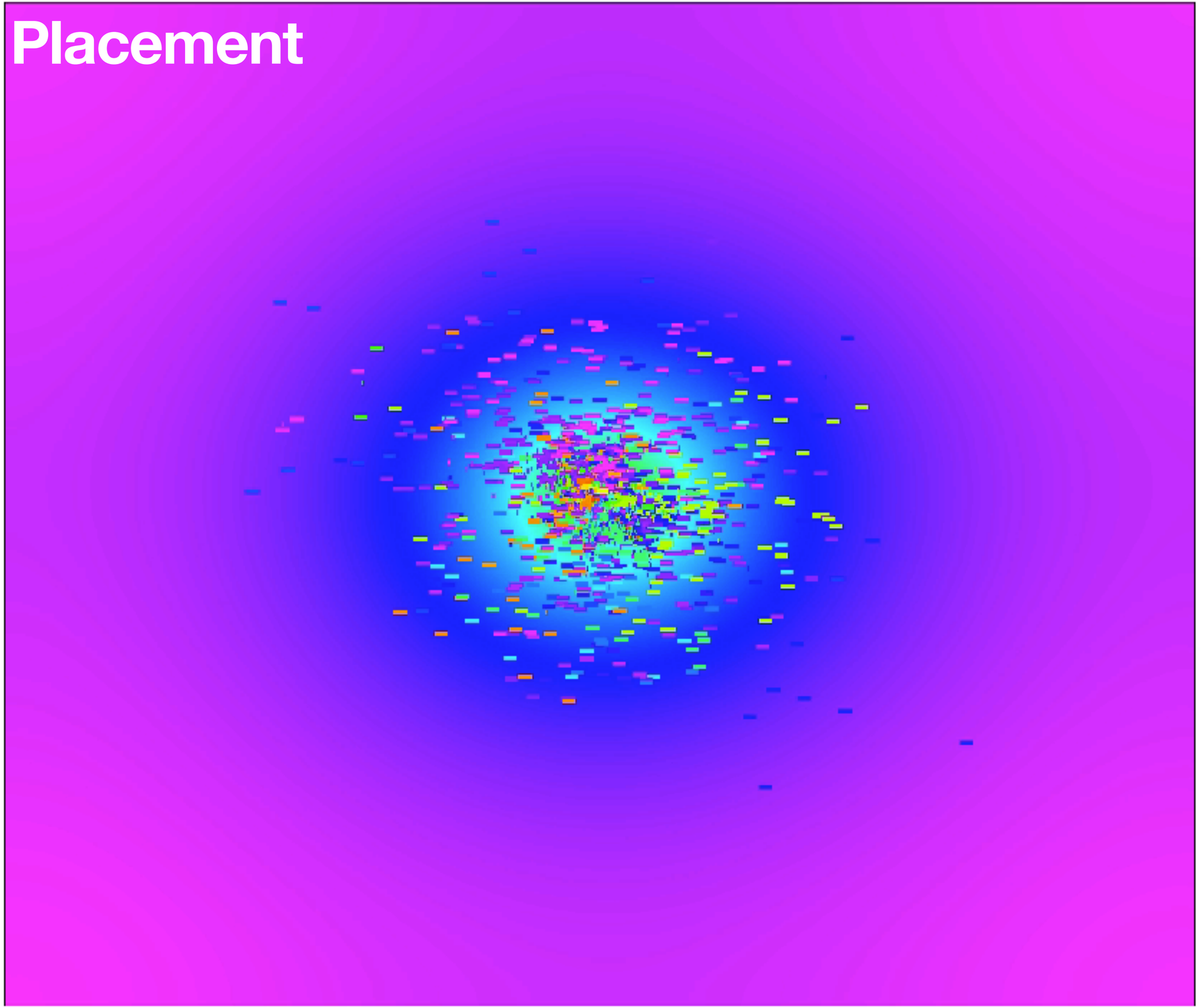
Placement using PlaceDL



Placement of the IBM18 circuit using UFRGS tools
> 200 thousand logic cells

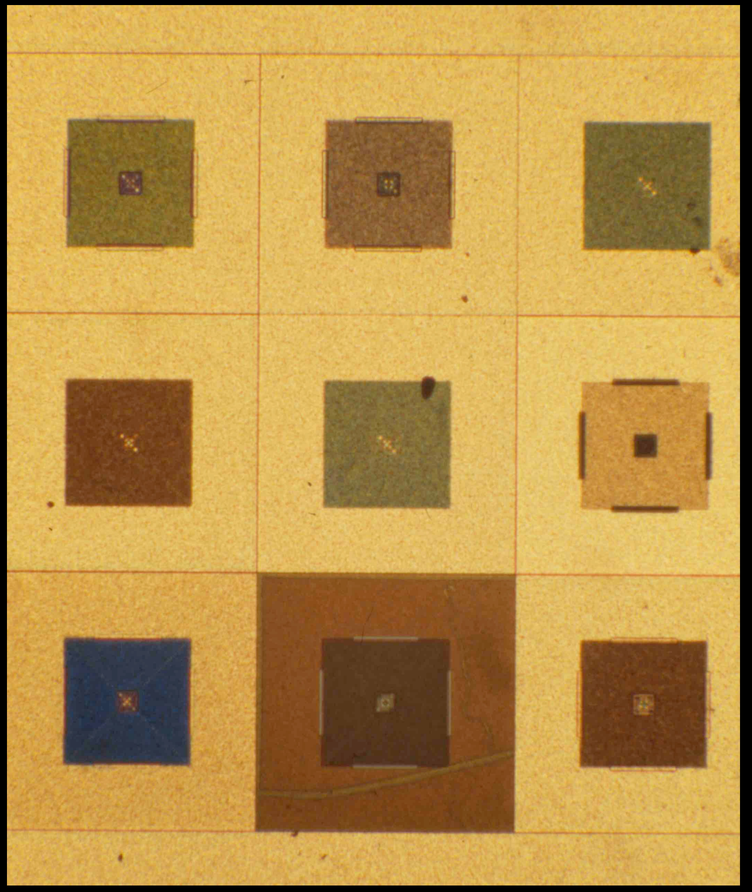


Placement



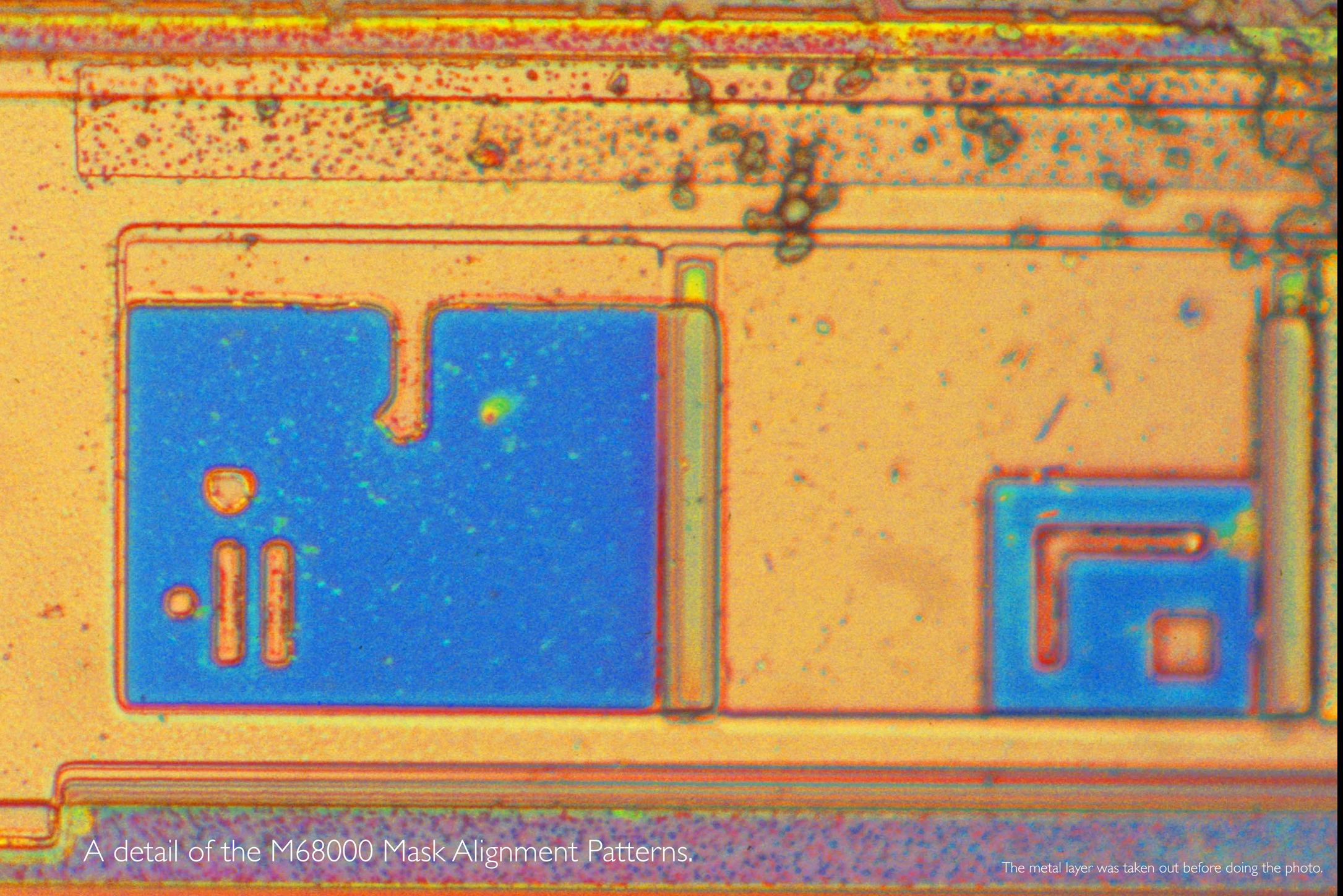
M6801

Detail of the M6801
Mask Alignment Patterns.



by Ricardo Reis

M68000

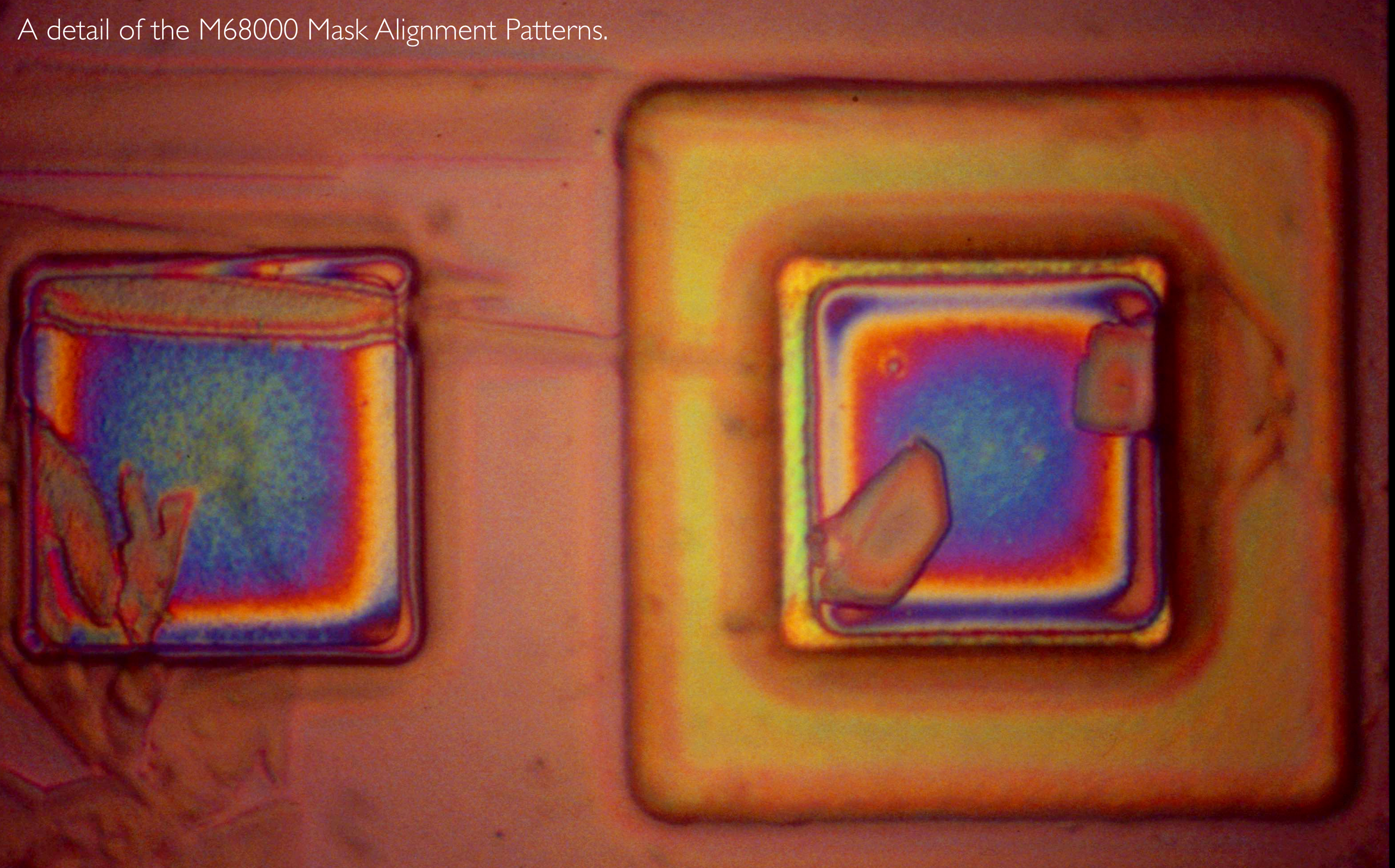


A detail of the M68000 Mask Alignment Patterns.

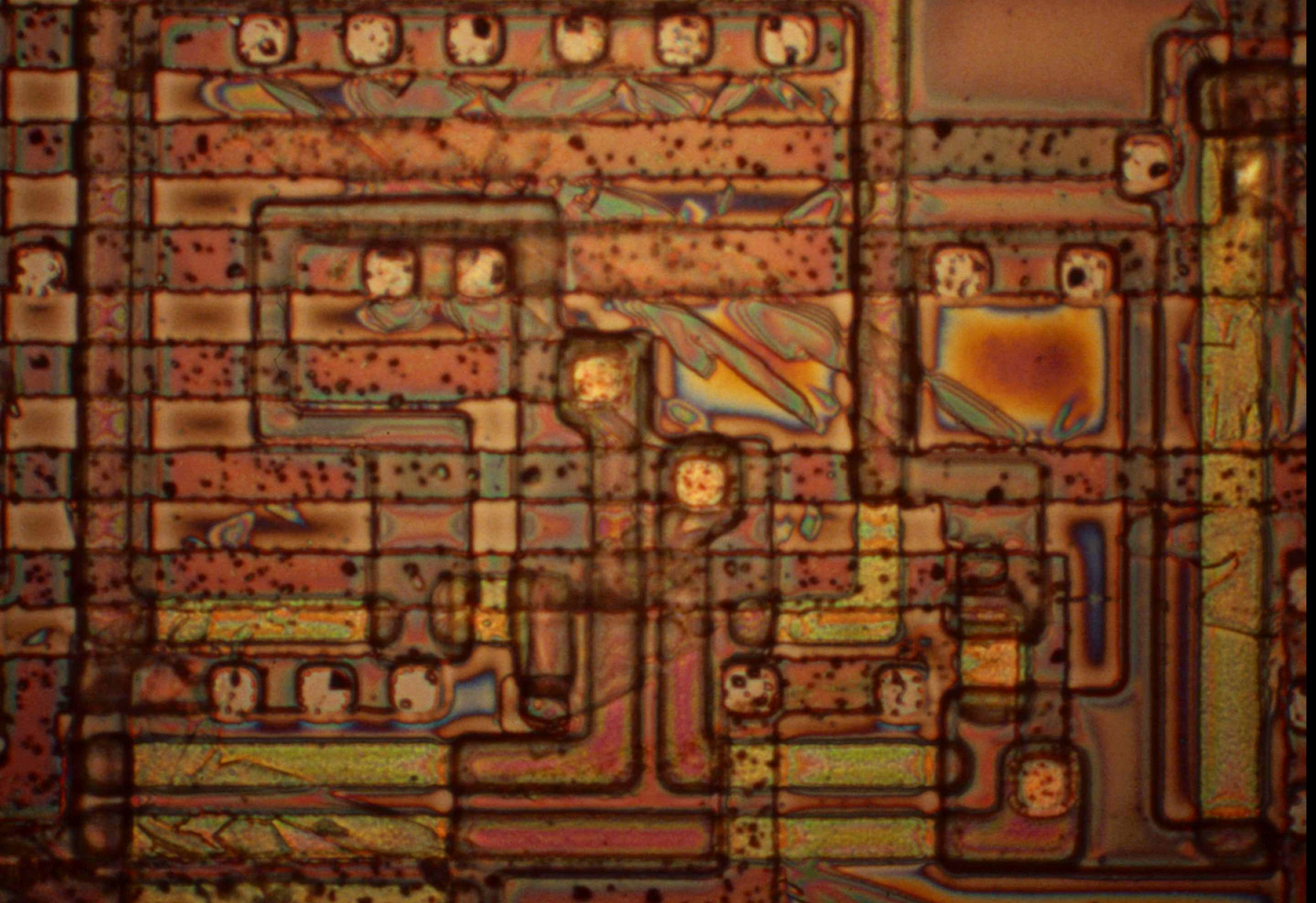
The metal layer was taken out before doing the photo.

by Ricardo Reis

A detail of the M68000 Mask Alignment Patterns.

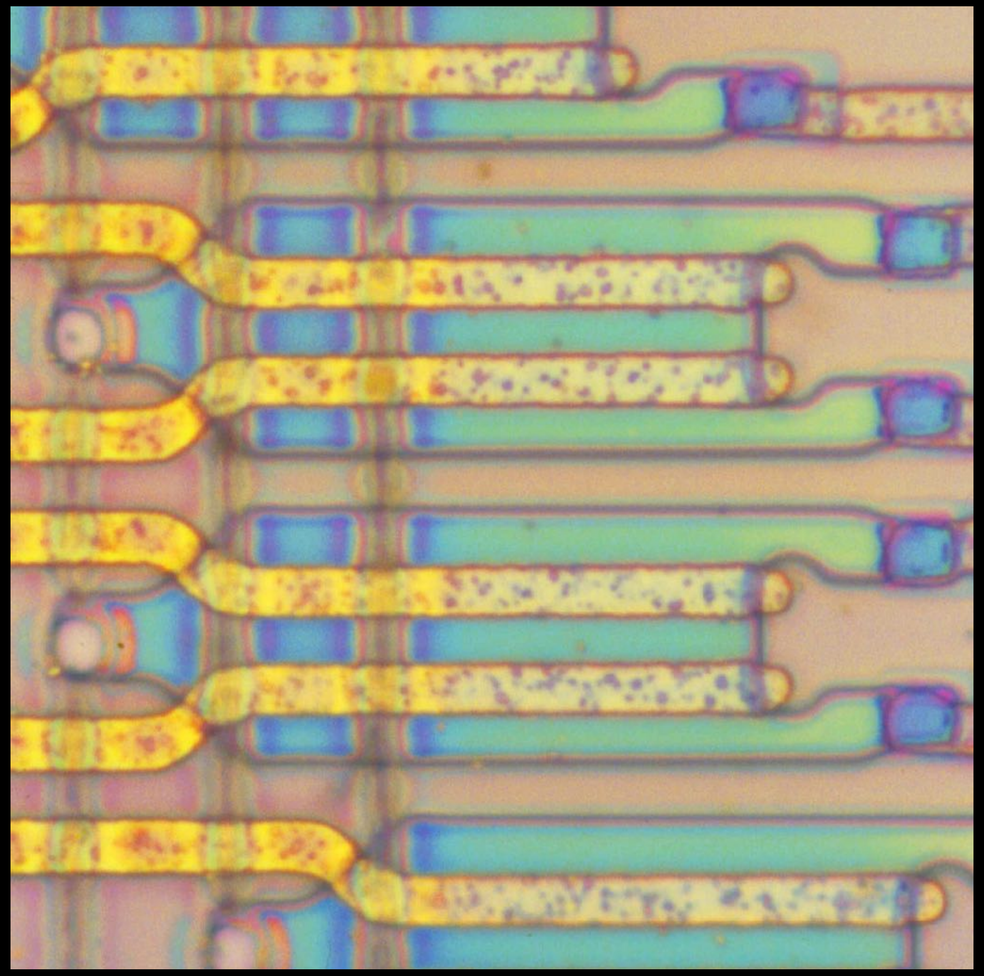


by Ricardo Reis



Detail of the M68000.

by Ricardo Reis



Traveling Inside a Chip

Ricardo Reis reis@inf.ufrgs.br

UFRGS

Something More

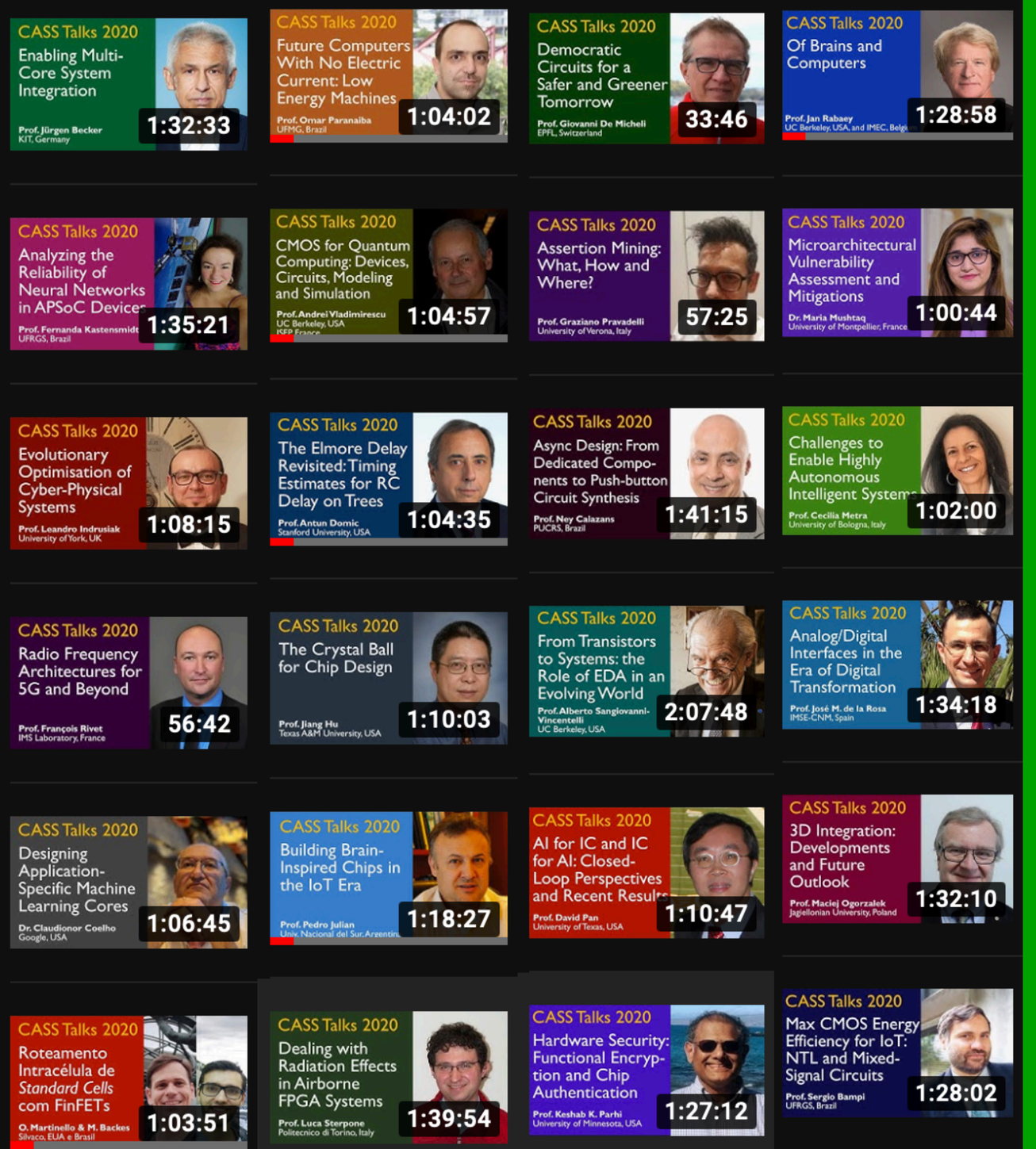
IEEE CASS Talks

from 2020 to 2023

Recorded Sessions at

www.youtube.com/cassriograndedosul

+ much more



UFRGS · INF Instituto de Informática UFRGS · UFRGS PGMICRO · Escola de Engenharia · IEEE · CAS IEEE Circuits and Systems Society

IEEE CASS Talks by CASS Rio Grande do Sul Chapter

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY

Some of the 2023 CASS TALKS

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

July 14, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Chi-ying Tsui, Hong Kong University of Science and Technology

SRAM-based Computing-in-Memory Design

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

July 21, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Georgios Sirakoulis, Democritus University of Thrace (DUTh), Greece

Quantum Computing and Memristors: How to Advance their Symbiosis

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

July 7, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Tobias Gemmeke, IDS, RWTH Aachen University, Germany

Time-domain Computing: Fundamentals and Prospects

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

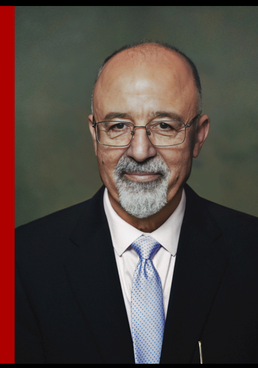
IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

March 17, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Mohamad Sawan, School of Engineering, Westlake University, Hangzhou, China

Closed-Loop AI-based Neuromodulation for the Diagnosis and Treatment of Brain Disorders

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul



IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

April 28, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Alberto Bosio,
Ecole Centrale de Lyon, France

Reliable and Efficient Hardware for Trustworthy Deep Neural Networks

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

June 30, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Laleh Behjat, University of Calgary, Canada

Application of Physical Design Algorithms in Other Domains

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

January 27, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Luca Carloni, Columbia University in the City of New York, USA

ESP: An Open-Source Platform for Heterogeneous Computing

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

February 3, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Mehdi B. Tahoori, KIT, Germany

Design Automation and Computing based on Additive Printed Electronics

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

April 14, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Paolo Crovetti, Politecnico di Torino, Italy

The First Ten Years of the Digital-Based Operational Transconductance Amplifier

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

March 24, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Diana Göhringer, TU Dresden, Germany

Adaptive Computing for Autonomous Systems

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

June 9, 2023, 1:30 PM (Brasilia Time, GMT-3)

Dr. Elena-Ioana Vatajelu, TIMA Laboratory, Grenoble, France

Versatility of Emergent Memory Technologies: Friend or Foe?

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

May 26, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Ayse K. Coskun,
Boston University, USA

Modeling and Optimizing Chip Cooling via Machine Learning

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

More than a 150 talks in the CASS Rio Grande do Sul YouTube Channel including Industrial Talks

IEEE CASS RS Talks 2023
UFRGS, Porto Alegre, Brazil

July 21, 2023, 1:30 PM (Brasilia Time, GMT-3)

Prof. Georgios Sirakoulis, Democritus University of Thrace (DUTh), Greece

Quantum Computing and Memristors: How to Advance their Symbiosis

YouTube Live @ IEEE CASS Rio Grande do Sul Chapter
https://www.youtube.com/cassriograndedosul

LASCAS2024

Punta del Este, Uruguay

February 27 - March 1, 2024

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY






LASCAS2025

Bento Gonçalves, Brazil

25- 28 February, 2025

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY





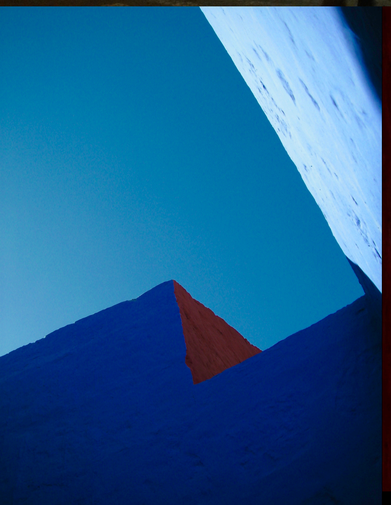

LASCAS2026

Arequipa, Peru

24-27 February, 2026

CAS
IEEE CIRCUITS AND SYSTEMS SOCIETY




SBCCI2023

40 years

36th SYMPOSIUM ON INTEGRATED CIRCUITS AND SYSTEMS DESIGN

August 21 to 25, 2023, Rio de Janeiro, BRAZIL

CHIP in RIO

Call for Papers

www.sbcci.org.br




Paper Submission Deadline: April 23, 2023

Notification of Acceptance: May 26, 2023
Camera-Ready Deadline: June 16, 2023

Sponsored by:
SBC - BRAZILIAN COMPUTER SOCIETY
SBMicro - BRAZILIAN MICROELECTRONICS SOCIETY
IEEE CIRCUITS & SYSTEMS SOCIETY
ACM SIGDA
IEEE CEDA - Council on EDA

Co-Sponsored by:
IFIP WG10.5 - International Federation for Information Processing

The 9th IEEE World Forum on the Internet of Things (IoT)

12–27 October 2023 // Aveiro, Portugal

Aveiro Congress Center

Hybrid: In-Person and Virtual

The Blue Planet: A Marriage of Sea and Space

Sponsored by the IEEE IoT Technical Community

wfiot2023.iot.ieee.org

OUR IEEE SPONSORING SOCIETIES AND COUNCILS

IEEE ComSoc IEEE Communications Society
CEDA IEEE Council on Electronic Design Automation
CAS IEEE CIRCUITS AND SYSTEMS SOCIETY
IEEE Reliability Society
IEEE Signal Processing Society
CSS
EDS
IES
MTT-S IEEE MICROWAVE THEORY & TECHNOLOGY SOCIETY
IEEE PES Power & Energy Society®
pels IEEE POWER ELECTRONICS SOCIETY Powering a Sustainable Future
SSCS IEEE SOLID-STATE CIRCUITS SOCIETY IC Innovation

PROPOSALS

Industry Forums
5 May 2023

Workshops
5 May 2023

Special Sessions
5 May 2023

Tutorials
July 23rd, 2023

Vertical and Topical Track
18 June 2023

SUBMISSIONS

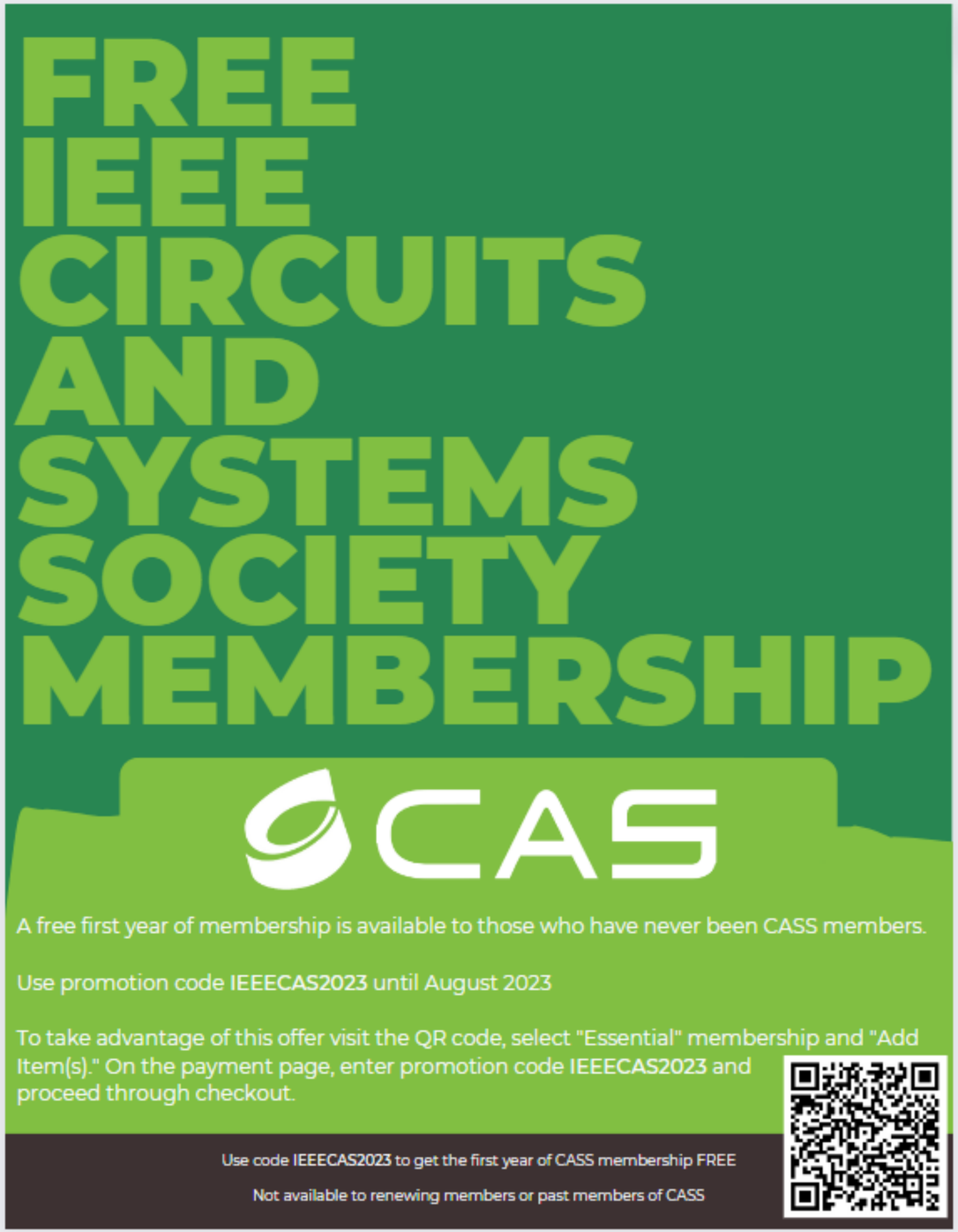
Peer-Reviewed Technical Papers
July 30, 2023

Special Session papers
18 June 2023

Workshop papers
18 June 2023

Vertical and Topical Track papers
18 June 2023

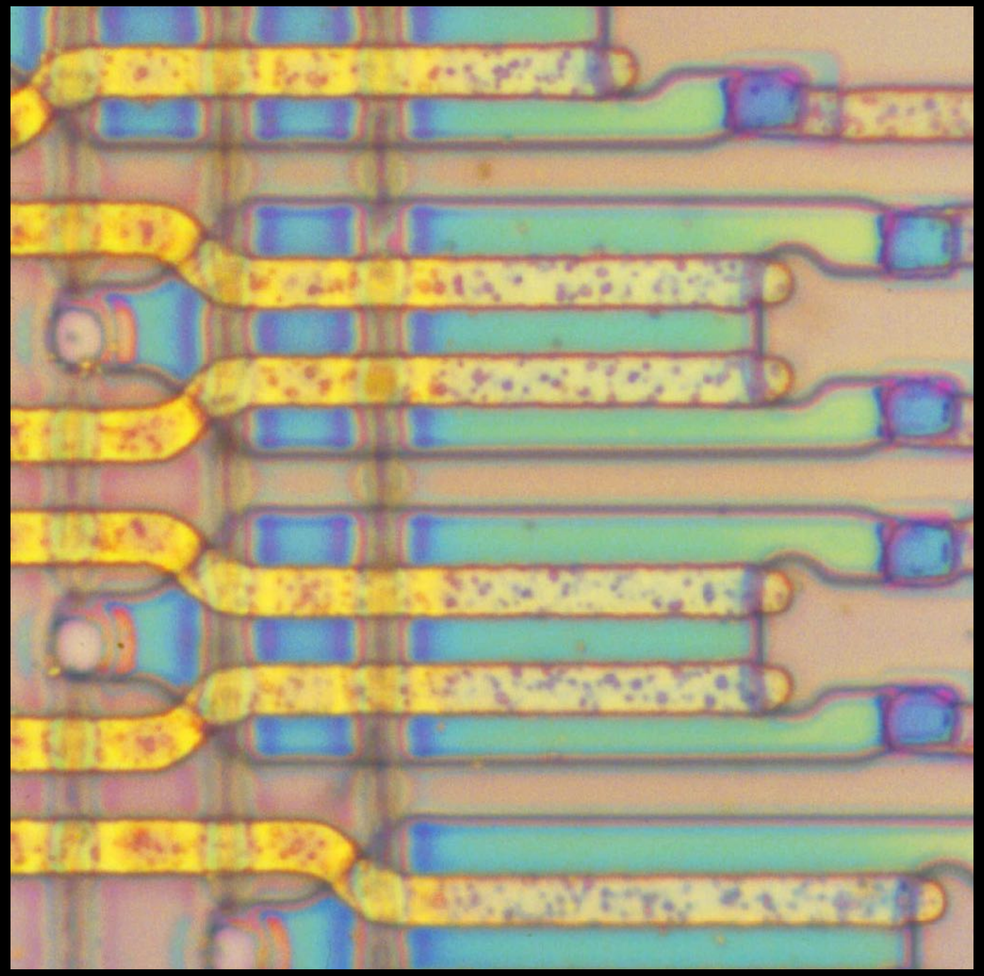
PhD/Master Forum papers
July 23rd, 2023



Promotion code IEEECAS2023 until August 2023

To take advantage of this offer visit the QR code, select "Essential" membership and "Add Item(s)." On the payment page,enter promotion code IEEECAS2023 and proceed through checkout.

Use code IEEECAS2023 to get the first year of CASS membership FREE.
Not available to renewing members
or past members of CASS



Traveling Inside a Chip

Ricardo Reis reis@inf.ufrgs.br

UFRGS