Heterogeneous 3D Integrated Circuits Current Problems

Maciej Ogorzałek

Department of Information Technologies

Faculty of Physics, Astronomy and Applied Computer Science

Jagiellonian University. Kraków , Poland

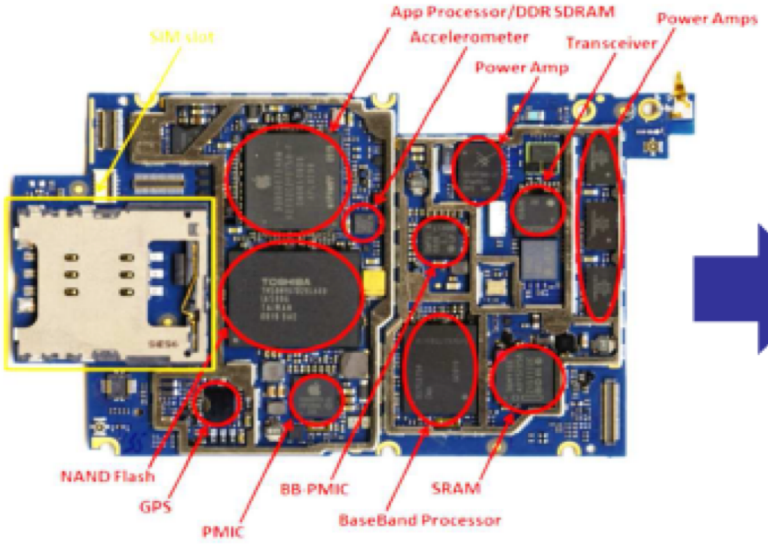
Jagiellonian University, established in **1364** is the oldest university in Poland and second (after Prague) in Central Europe.

Best known alumnus: Nicolaus Copernicus

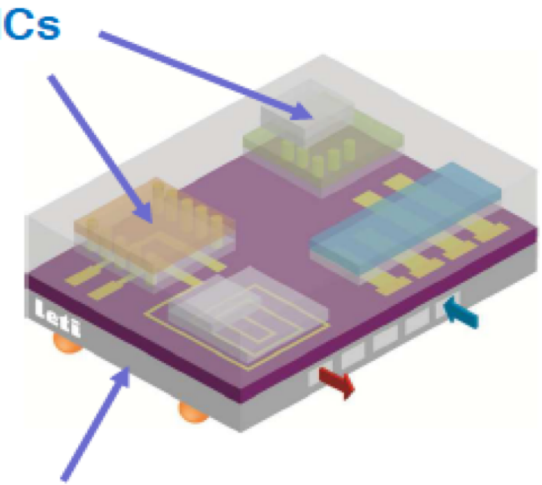
Motivation for electronic engineer

Build circuits/systems that are smaller, more powerful, faster, with improved functionality, serving more/new applications =

how to put more devices/ blocks on-chip?



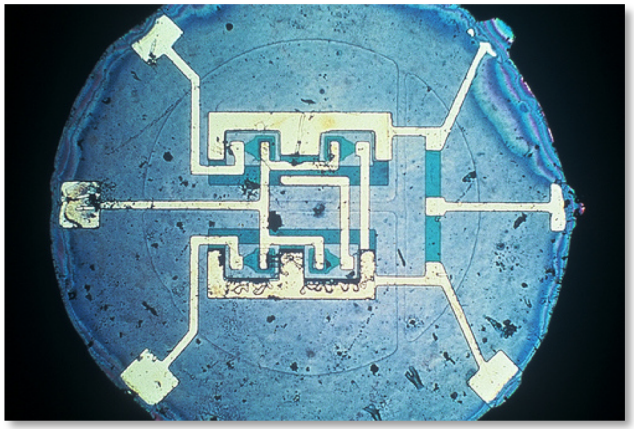
System on board
(Smatphone PCB)



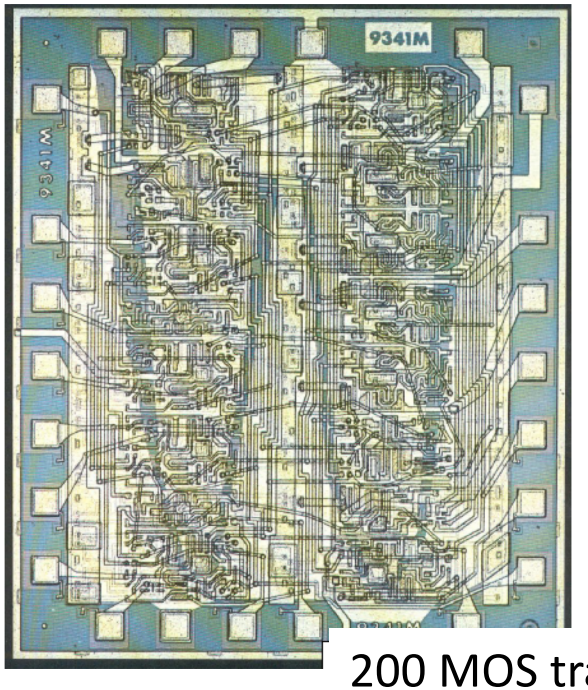
A silicon interposer

With very heterogeneous dice on it (various substrates, various technologies co-existing, various chip makers…).

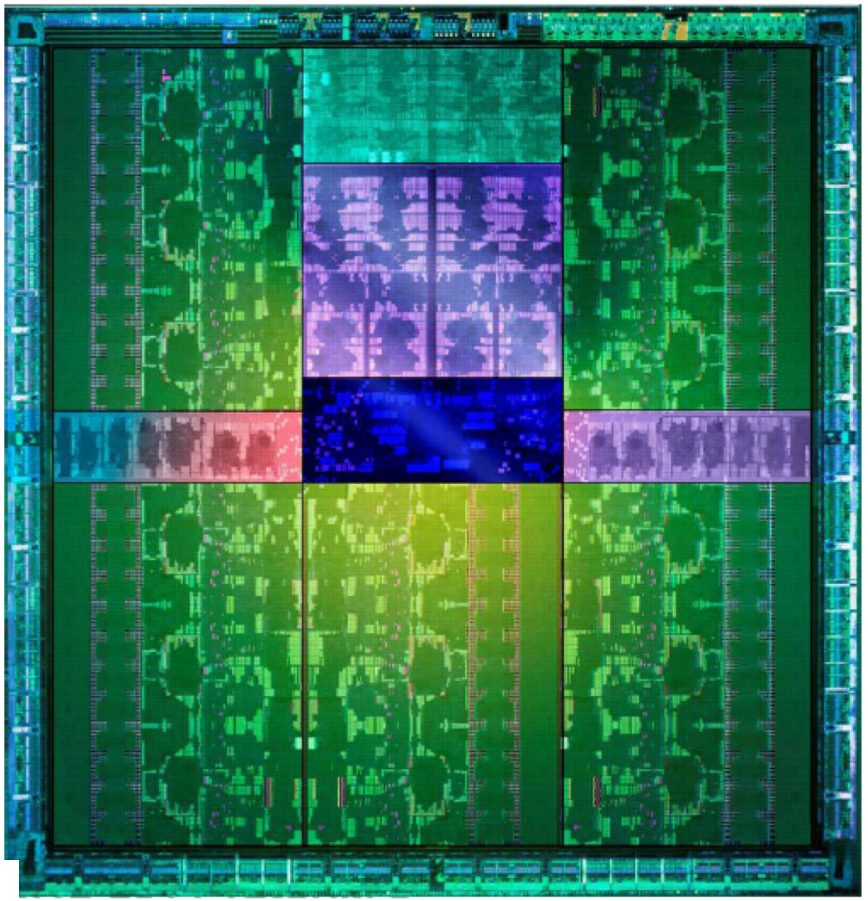
IC Evolution



4 bipolar transistors in 1959



200 MOS transistors in 1969 !



NVIDIA Kepler 7.080 Billion /2013

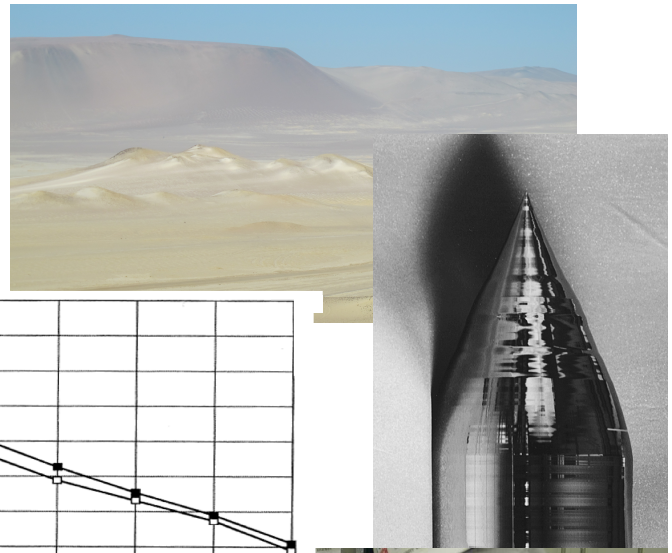
Why silicon?

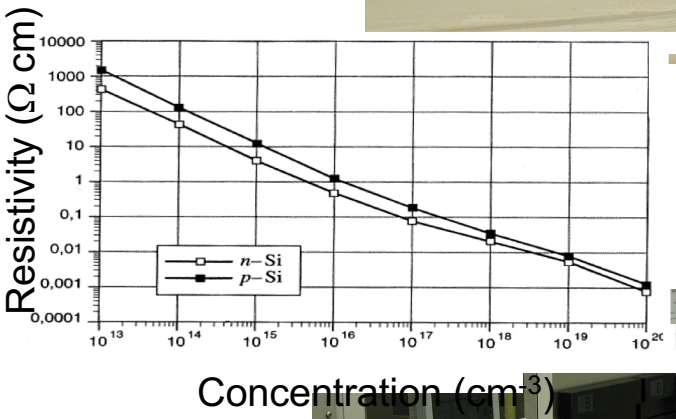
Although first working transistors and integrated circuits where based on Ge, the IC technology was build on Si !!

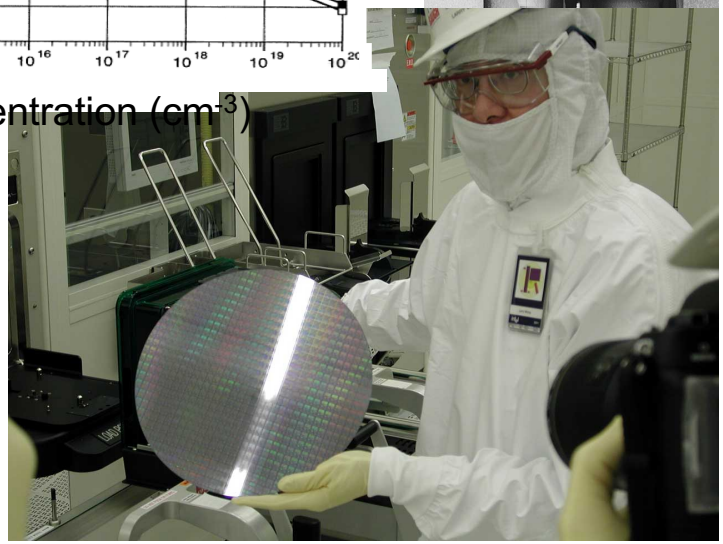
Si is a “wonder” material
- Abundant element
- Semiconductor properties
  - P and N type by doping
  - Resistivity can be tuned

Si can be oxidized into SiO_2
- Stable material (>< Ge)
- SiO_2 is good dielectric
  - Gate dielectric
  - Good Si/SiO_2 interface properties

Can be grown in large crystals
- Typically cilindrical ingots that are sawed into wafers
- Flat and rigid substrates





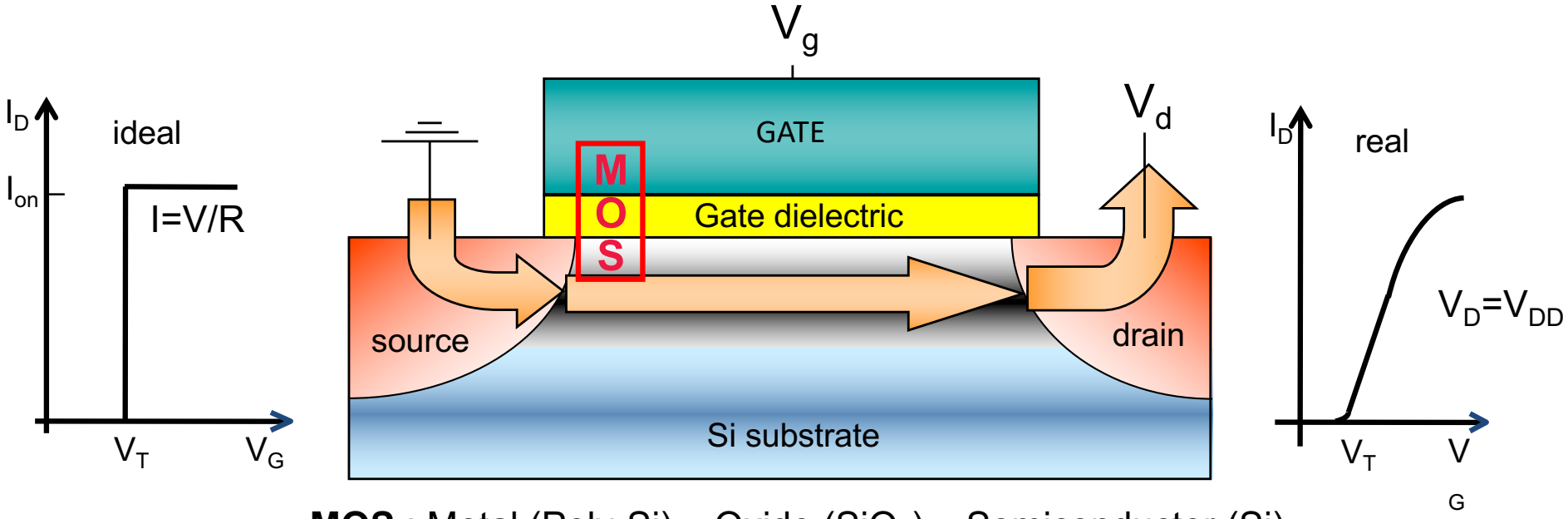


MOSFETs:
The building blocks of electronics

CMOS transistor in digital CMOS circuit is a *SWITCH* with *GAIN*

MOSFET: three terminal device that consists of two *pn*-junctions and one capacitor structure

- metal/oxide/semiconductor or MOS-capacitor structure
  - – no current flow, only voltage applied
- source and drain contacts to silicon
  - – passing current "under" the oxide from source to drain (voltage and current)

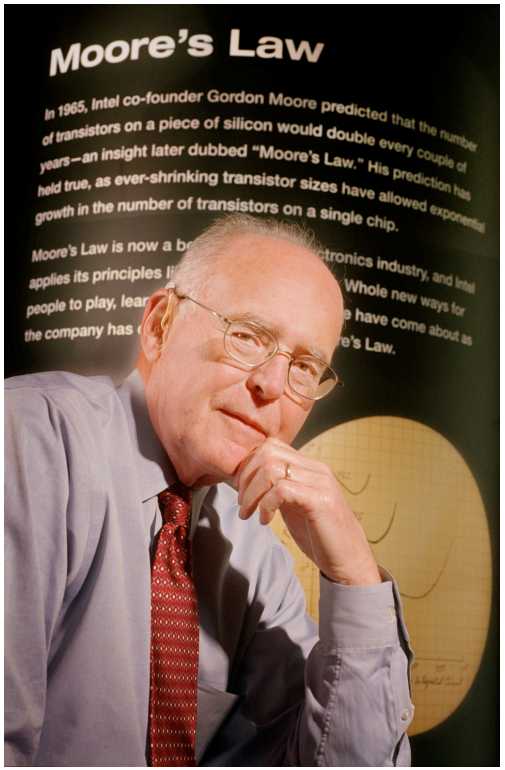


MOS : Metal (Poly-Si) – Oxide (SiO_2) – Semiconductor (Si)

Number of transitors/processor

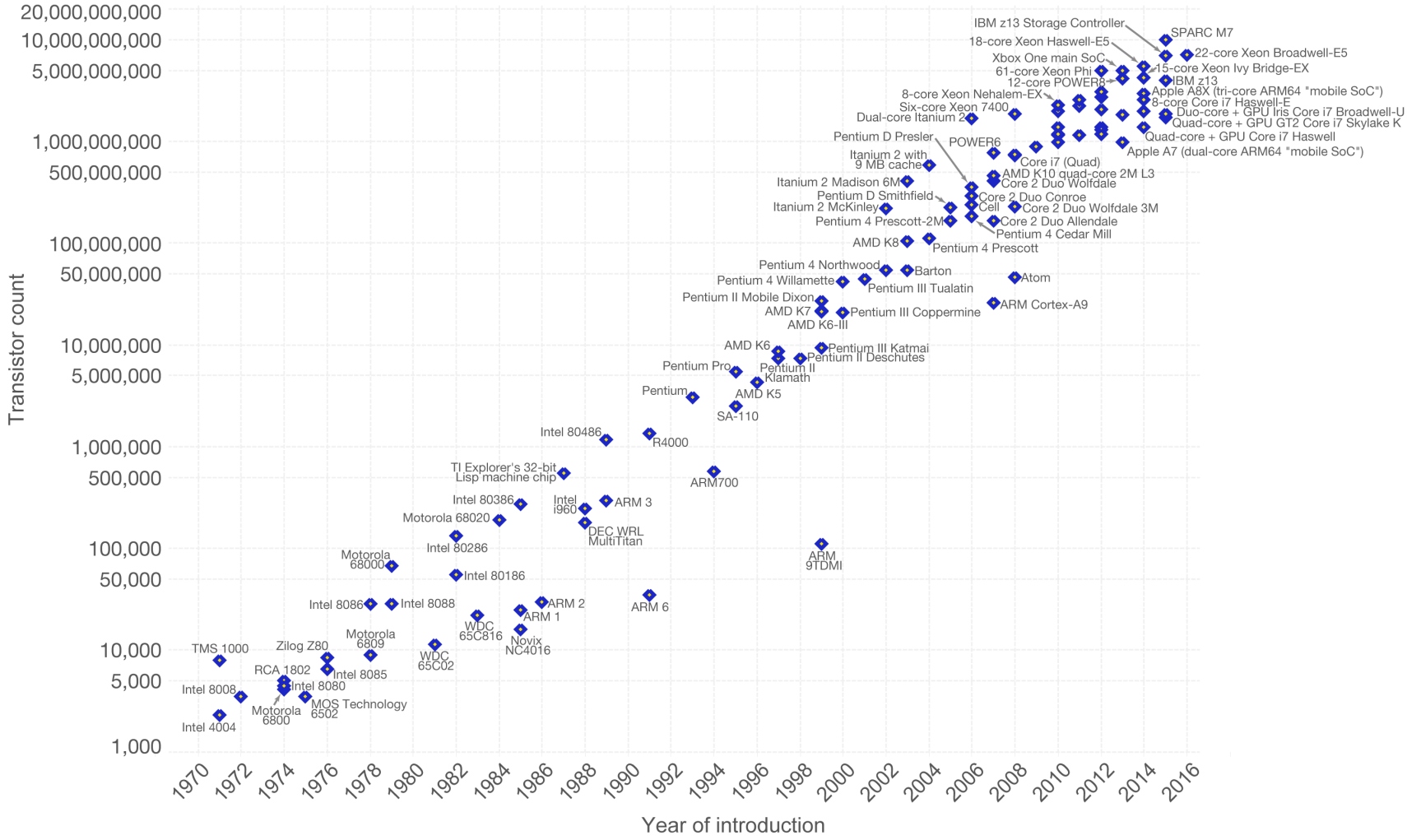
Gordon E. Moore (1965). "Cramming more components onto integrated circuits". Electronics

Zilog Z80 - 8500 transistors
Intel 8086 – 29000 - Intel 80286 - 134 000 - Intel 80486 - 1 180 000
Pentium II - 7 500 000
Pentium III - 9 500 000
AMD K7 - 22 000 000
Pentium IV - 42 000 000
AMD K8 - 105 900 000
Core i7 - 732 000 000
Six-Core Xeon 7400 1,900,000,000
Quad-Core Itanium Tukwila 2,000,000,000 699 mm²
8-Core Xeon Nehalem-EX 2,300,000,000
10-Core Xeon Westmere-EX2,600,000,000 (32nm)
Six-core zEC12 2,750,000,000 2012 IBM 32nm 597 mm²
8-Core Itanium Poulson 3,100,000,000 2012 Intel 32 nm 544 mm²
62-Core Xeon Phi 5,000,000,000 2012 Intel 22 nm
Xbox One Main SoC 5,000,000,000 2013 Microsoft 363 mm²
12-core POWER8 4,200,000,000 2013 IBM 22 nm 650 mm²
Apple A7 (dual-core ARM64 "mobile SoC") 1,000,000,000 2013 Apple 28 nm 102 mm²
15-core Xeon Ivy Bridge-EX 4,310,000,000[25] 2014 Intel 22 nm 541 mm²
Apple A8 (dual-core ARM64 "mobile SoC") 2,000,000,000 2014 Apple 20 nm 89 mm²
SPARC M7 >10,000,000,000 announced 2014 Oracle 20 nm
Apple A8X (tri-core ARM64 "mobile SoC") 3,000,000,000 2014 Apple 20nm



Moore’s Law – The number of transistors on integrated circuit chips (1971-2016)

Moore's law describes the empirical regularity that the number of transistors on integrated circuits doubles approximately every two years. This advancement is important as other aspects of technological progress – such as processing speed or the price of electronic products – are strongly linked to Moore's law.



Data source: Wikipedia (https://en.wikipedia.org/wiki/Transistor_count)
The data visualization is available at OurWorldinData.org. There you find more visualizations and research on this topic.

Simon Fraser University - May 7th, 2018
Maciej Ogorzałek

Current leaders

IBM z133, 990,000,000 2015 IBM22 nm678 mm²

IBM z13 Storage Controller7, 100,000,000 2015 IBM 22 nm 678 mm²

22-core Xeon Broadwell-E57, 200,000,000 2016 Intel14 nm 456 mm²

Qualcomm Snapdragon 835 (octa-core ARM64 "mobile SoC")3,000,000,000, 2016, Qualcomm 10 nm

10-core Core i7 Broadwell-E 3,200,000,000 2016 Intel 14 nm 246 mm²

Apple A10 Fusion (quad-core ARM64 "mobile SoC")3,300,000,000 2016 Apple16 nm125 mm²

Apple A11 Bionic (hexa-core ARM64 "mobile SoC") 4,300,000,000 2017 Apple10 nm 89 mm²

8-core Ryzen4,800,000,000 2017 AMD 14 nm 192 mm²

IBM z146, 100,000,000 2017 IBM 14 nm 696 mm²

Xbox One X (Project Scorpio) main SoC7,000,000,000 2017 Microsoft/AMD16 nm 360 mm²

POWER9 8,000,000,000 2017 IBM14 nm 695 mm²

IBM z14 Storage Controller 9,700,000,000 2017 IBM 14 nm 696 mm²

Centriq 2400 18,000,000,000 2017 Qualcomm10 nm 398mm^2

32-core AMD Epyc 19,200,000,000 2017 AMD14 nm 4× 192 mm^2

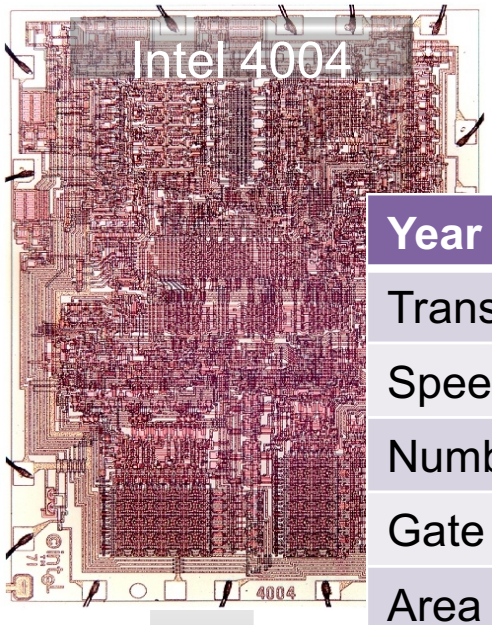
GPU and FPGA complexity

G80 681,000,000 NVIDIA
Radeon RV770 956,000,000 AMD
GeForce GT200 1,400,000,000 NVIDIA
RV870 2,154,000,000 AMD
Cayman 2,640,000,000 AMD
GF100 3,000,000,000 NVIDIA (40nm)
GK104 Kepler 3,540,000,000 2012 NVIDIA 28 nm 294 mm^2
Tahiti RV1070 4,312,711,873 2011 AMD 28 nm 365 mm^2
GK110 Kepler 7,080,000,000 2012 NVIDIA 28 nm 561 mm^2

Virtex ~70,000,000 (1997)
Virtex-4 1,000,000,000 XILINX
Virtex-5 1,100,000,000 XILINX
Stratix IV 2,500,000,000 Altera
Stratix V 3,800,000,000 Altera 2011 (28nm)
Virtex-7 6,800,000,000 2011 Xilinx 28 nm
Virtex-Ultrascale XCVU440 20,000,000,000+ 2014 Xilinx 20nm

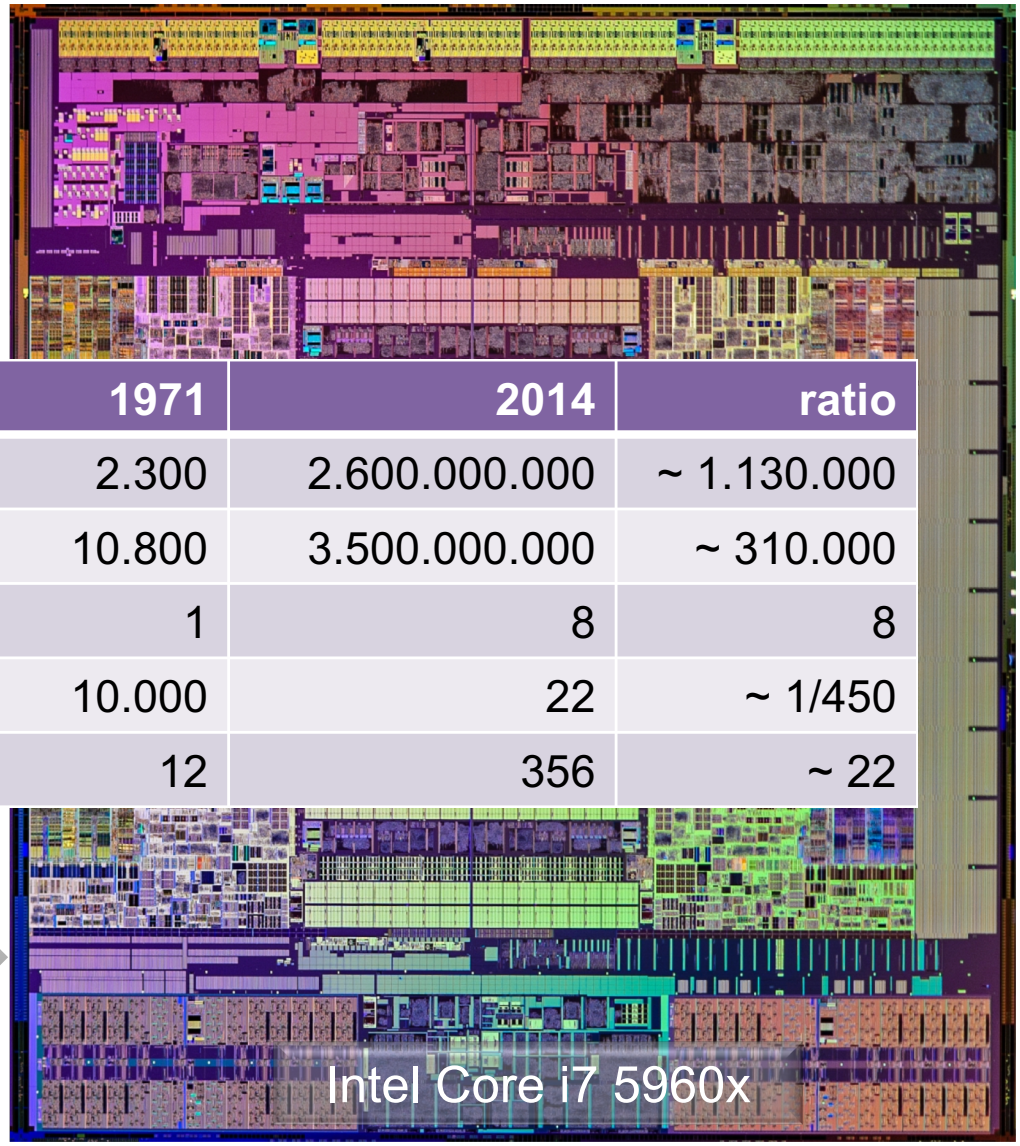
The power of scaling

Making things smaller ➔ more and faster transistors on chip



Year	1971	2014	ratio
Transistors	2.300	2.600.000.000	~ 1.130.000
Speed (Hz)	10.800	3.500.000.000	~ 310.000
Number of cores	1	8	8
Gate length (nm)	10.000	22	~ 1/450
Area (mm^2)	12	356	~ 22

Cost scaling
Performance

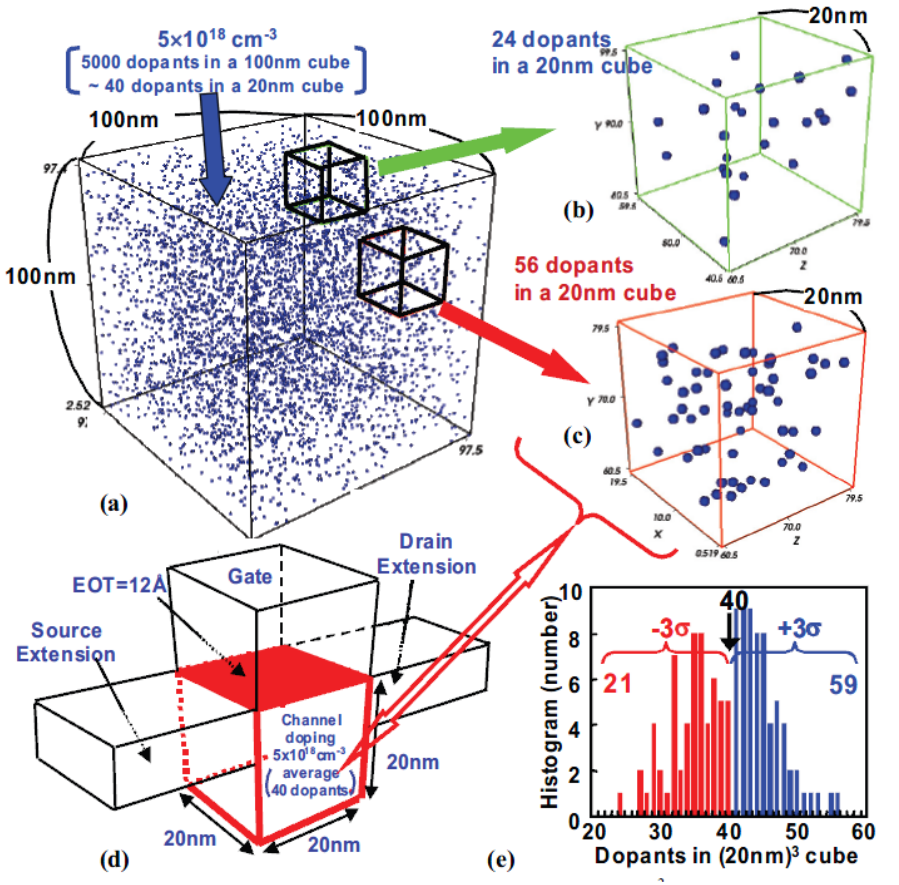


Why we go into new technologies?
Current technologies are approaching their limits!

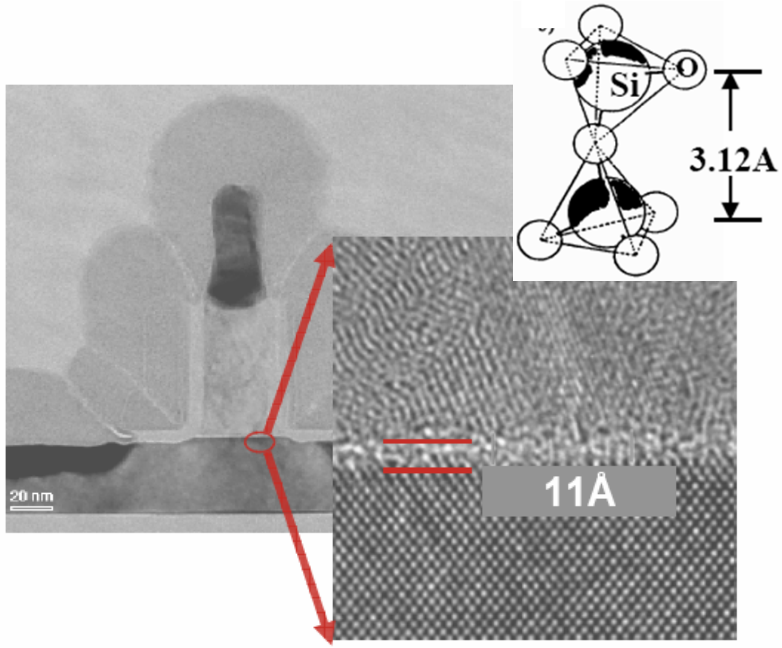
- Size of circuit footprint (500mm^2) – yield becomes low
- Chip area limits – cost grows exponentially
- Silicon technologies approaching the limits:
  - Feature size for transistor fabrication -14nm, 10nm, 7nm?
  - Width of interconnect paths + wire pitch constraint
  - Signal transfer delay limits (gate delay vs. wire delay)
  - Power efficiency
  - Power dissipation on the chip – power consumption explosion

CMOS scaling nearing atomic limits

Performance of MOSFETs has been increased by scaling the device dimensions, but limits of scaling are being approached.



Random dopant fluctuations



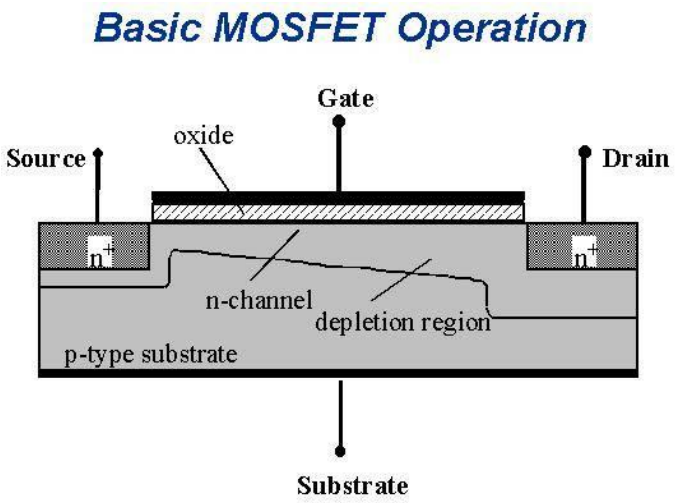
Gate oxide scaling

- Approaching atomistic and quantum-mechanical boundaries
- **Atoms are not scalable!**

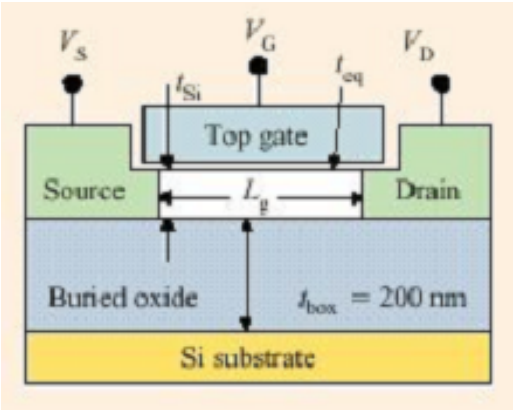
What are the solutions ?

1. Shrink the feature size in known technologies – how much further ?
2. Exploit new/3D geometries for transistors
3. Put elements and blocks in 3D stacks
4. Exploit new technologies
5. Invent new types of elements

Partial remedies - FinFETs



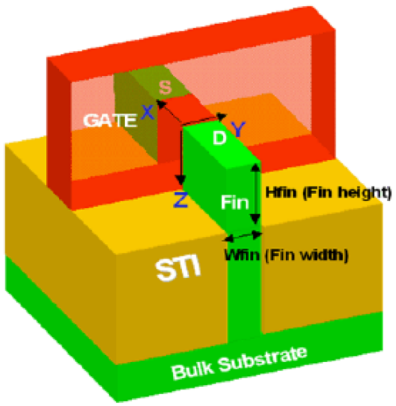
Bulk nmos

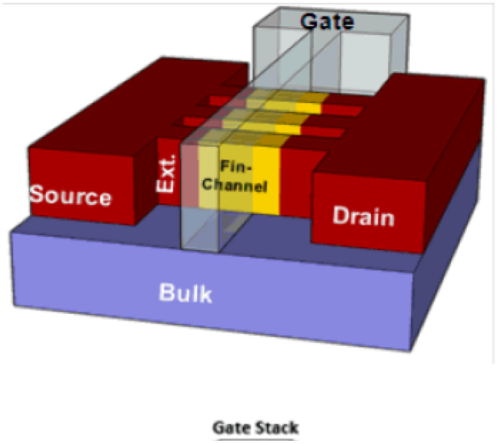


Silicon on insulator

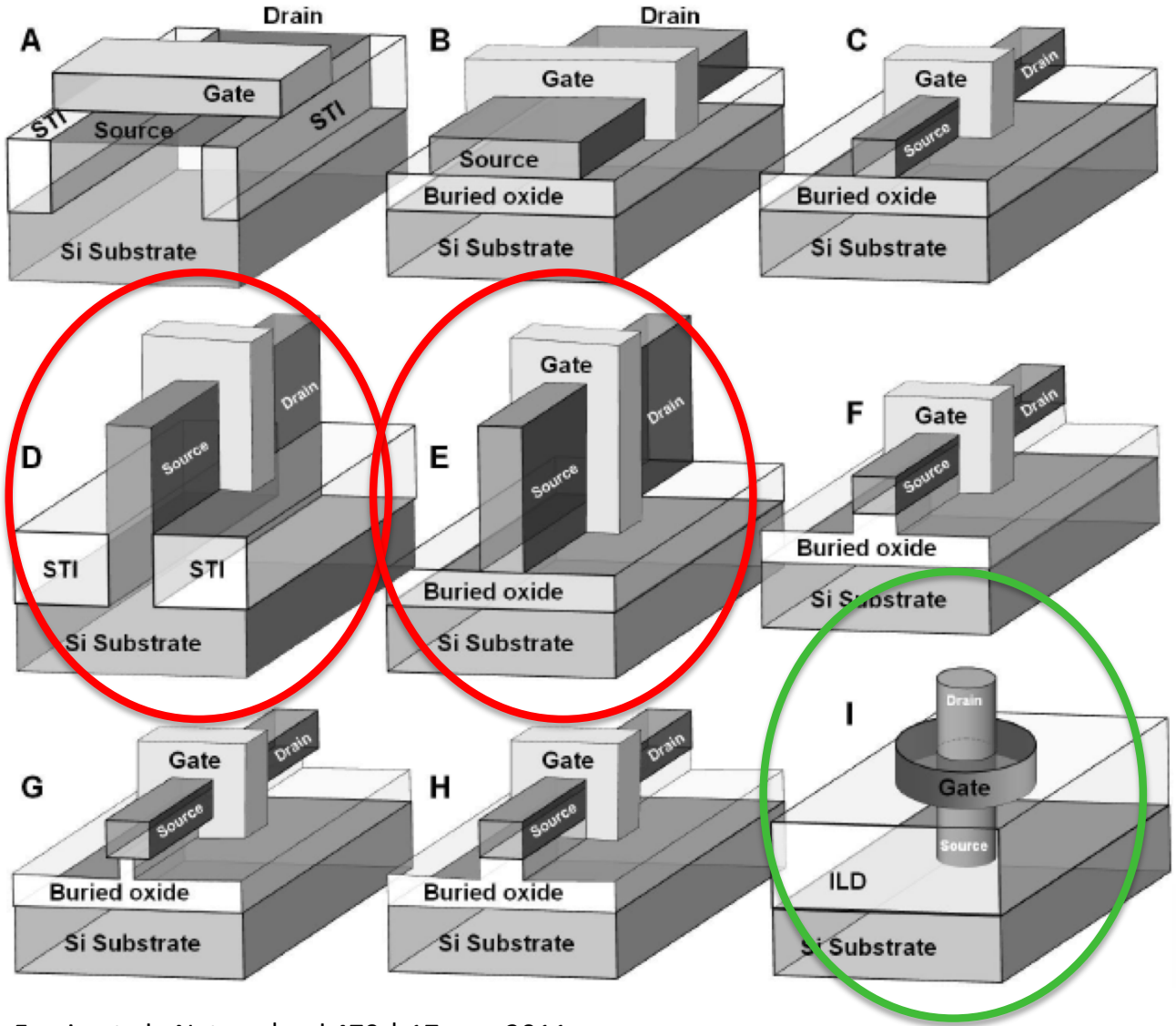
FinFet

This is a 3D structure!
Main gain – enlarged gate area!





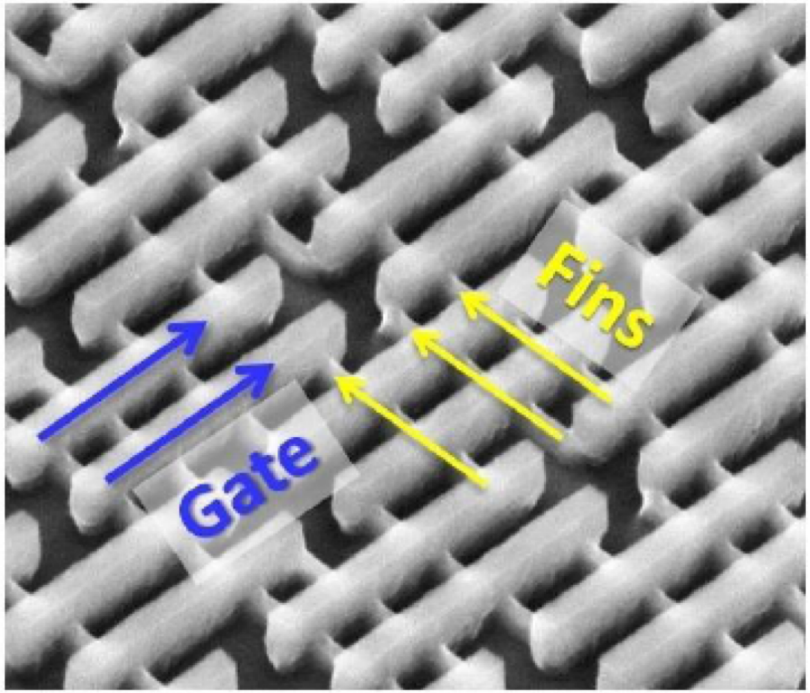
Evolution of Field Effect Transistors



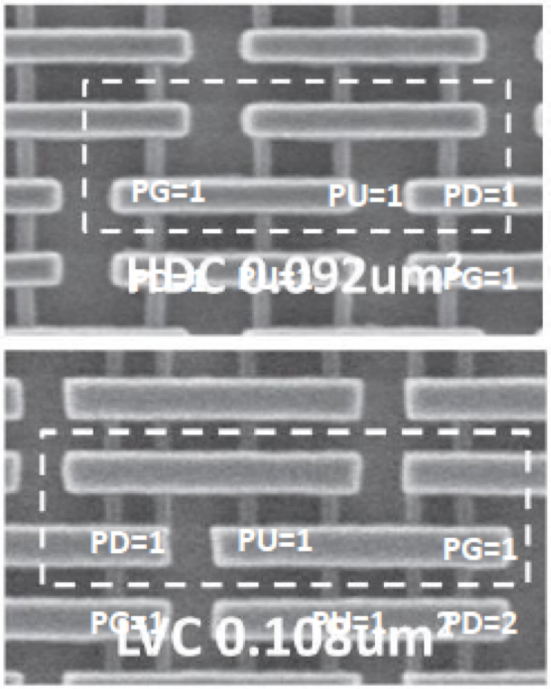
- A: Single-gate planar bulk MOSFET.
- B: Single-gate SOI MOSFET with mesa isolation.
- C: Triple-gate (trigate) SOI nanowire MOSFET with square cross section.
- D: Bulk trigate MOSFET with high aspect ratio (bulk FinFET).
- E: SOI trigate MOSFET with high aspect ratio (SOI FinFET).
- F: Π-gate SOI nanowire MOSFET.
- G: Ω-gate SOI nanowire MOSFET.
- H: Horizontal gate-all-around (GAA, quadruple-gate, quad-gate) nanowire MOSFET.
- I: Vertical gate-all-around (GAA) nanowire MOSFET.

I. Ferain et al., Nature | vol 479 | 17 nov. 2011

SRAM memory based on FinFETs



Ref: paper 13.1 (Intel), ISSCC, 2012



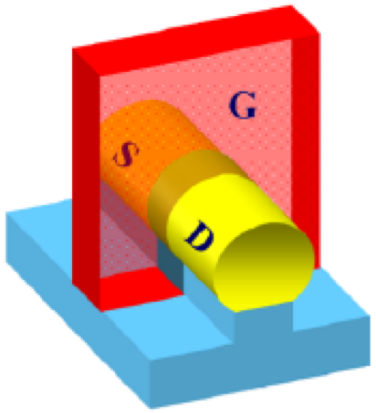
High Density (HDC):
0.092 um2
1:1:1 PU:PG:PD

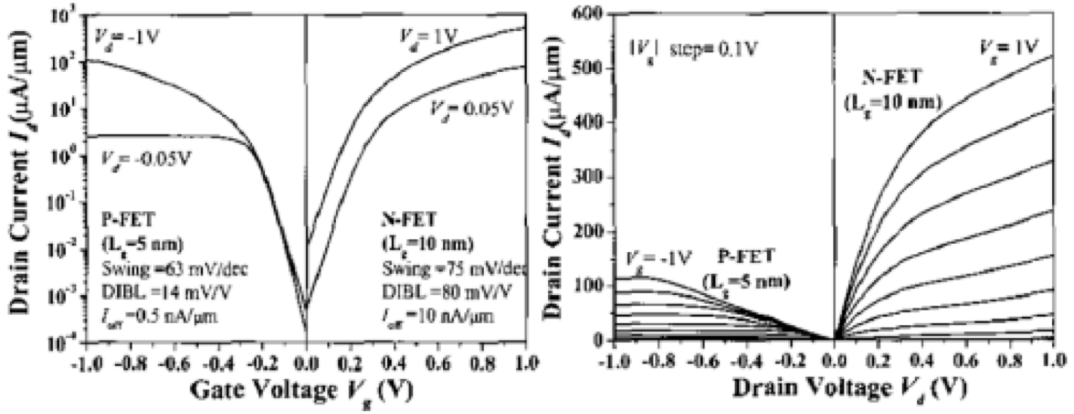
Low Voltage (LVC):
0.108 um2
1:1:2 PU:PG:PD

Where to go further?
New technologies = Nanowires!

Experimental "Omega-Gate " FET
L_G=**5nm**, 2004

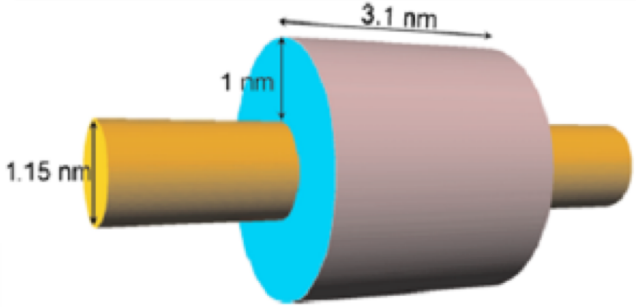
Fu-Liang Yang, et al., "5nm-gate nanowire FinFET" , Symposium on VLSI Technology. Digest of Technical Papers, pp. 196-7, 2004

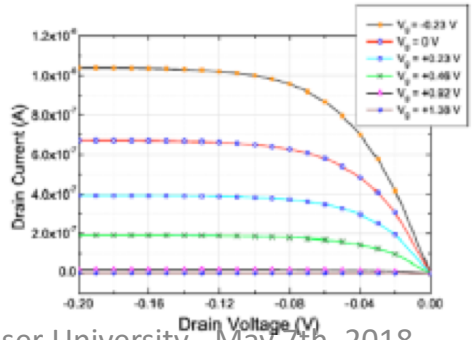


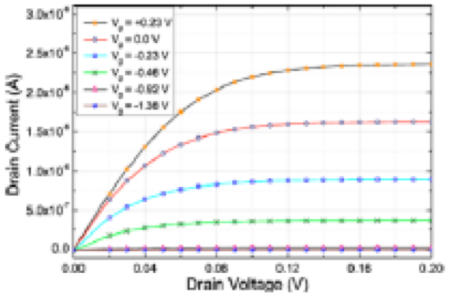


Ab-initio ***simulations*** of GAA FET
L_G=**3.1nm**, 2010

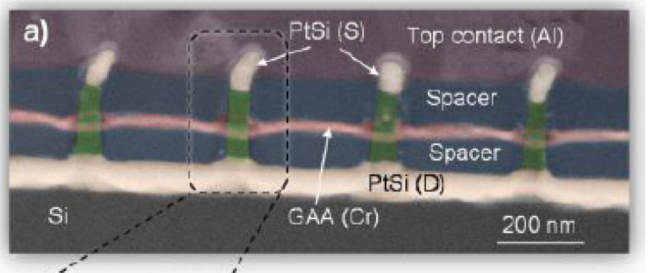
. **Ansari et al., "Simulation of junctionless Si nanowire transistors with 3 nm gate length"**, Applied Physics Letters **97, 062105 ,2010**



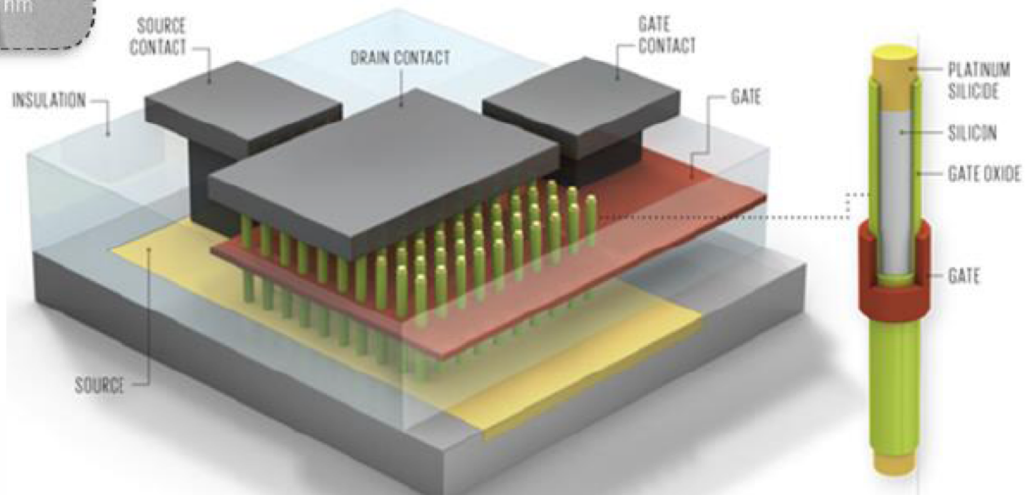




Vertical Nanowire transistors !!



G. Larrieu and X.-L. Han, "Vertical nanowire array-based field effect transistors for ultimate scaling", Nanoscale, Vol. 5, p. 2437 (2013)

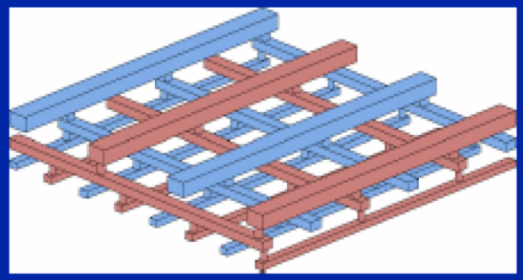


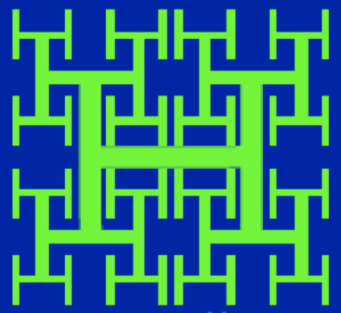
More challenges - Interconnects

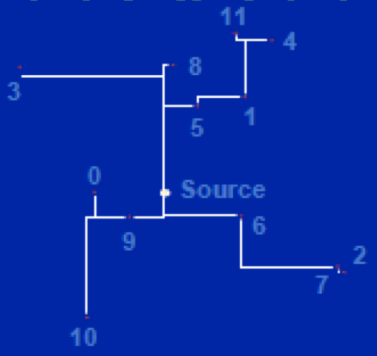
Interconnect Networks

- Power distribution networks
  - Consume about 30% on-chip metal
  - *IR*, *Ldi/dt* noise
  - *RLC* resonances
- Clock distribution networks
  - Consume up to 70% of the total power
  - Clock skew, jitter
- Signals with multiple fan-out
- Large global busses

- Interconnect networks have become increasingly complicated with greater integration
  - Accurate and efficient models are required

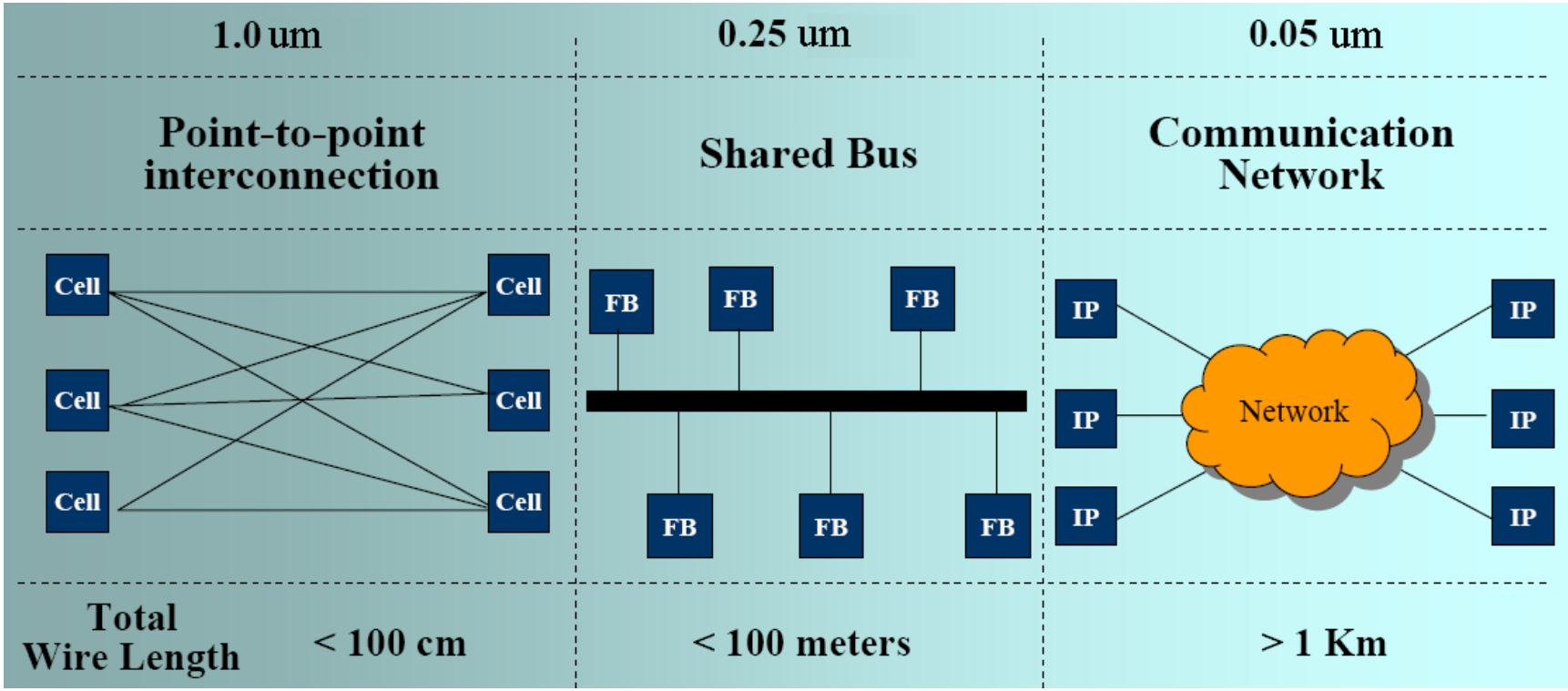






Source: prof. Eby Friedman

How the blocks communicate?



Current technologies - wire length > 10km

Solution: Network-on-chip

Next step – go 3D !!

2D interconnect performance

Operation	Delay (0.13um)	(0.05um)
32b ALU Operation	650ps	250ps
32b Register Read	325ps	125ps
Read 32b from 8KB RAM	780ps	300ps
Transfer 32b across chip (10mm)	1400ps	2300ps
Transfer 32b across chip (20mm)	2800ps	4600ps

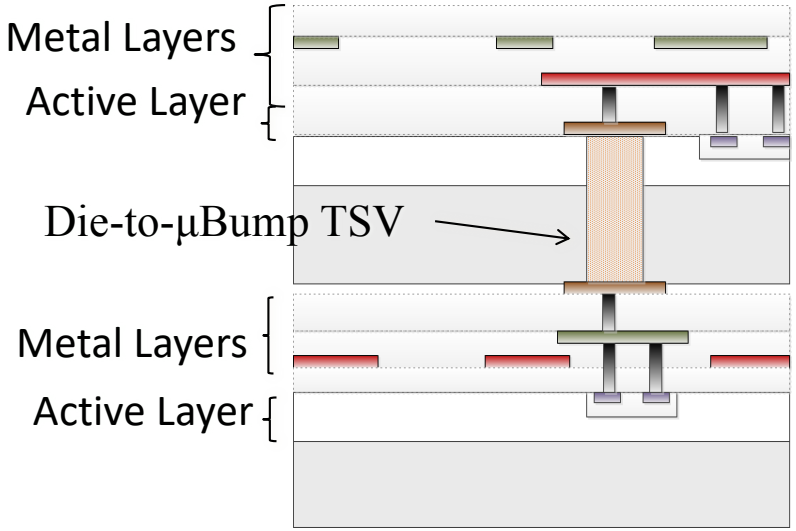
2:1 global on-chip comm to operation delay

9:1 in 2010

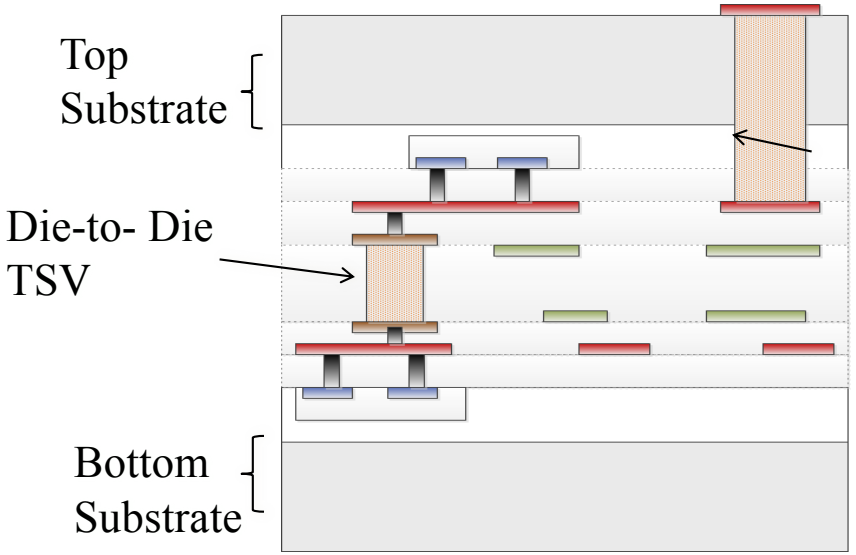
- Interconnect delay dominates gate delay
  - – Global interconnect delay continuously increasing – currently up to 2-3 orders of magnitude over gd
  - – Need multiple clock cycles to cross chip die
  - – Limits the performance of microprocessors

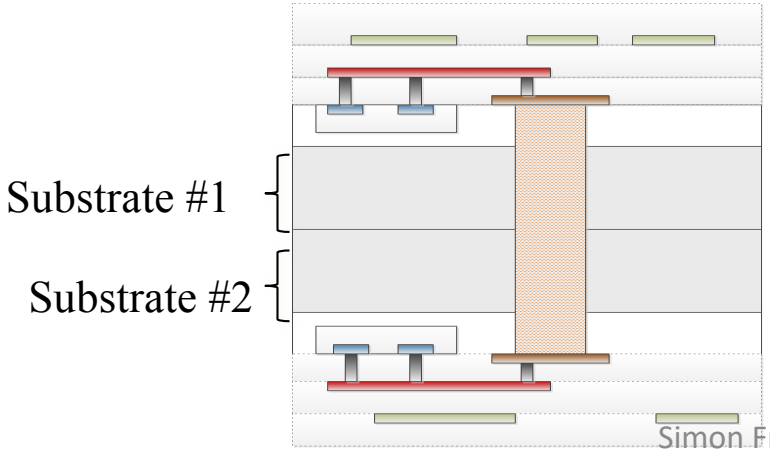
3D Stacking of silicon layers

Face-to-Back



Face-to-Face



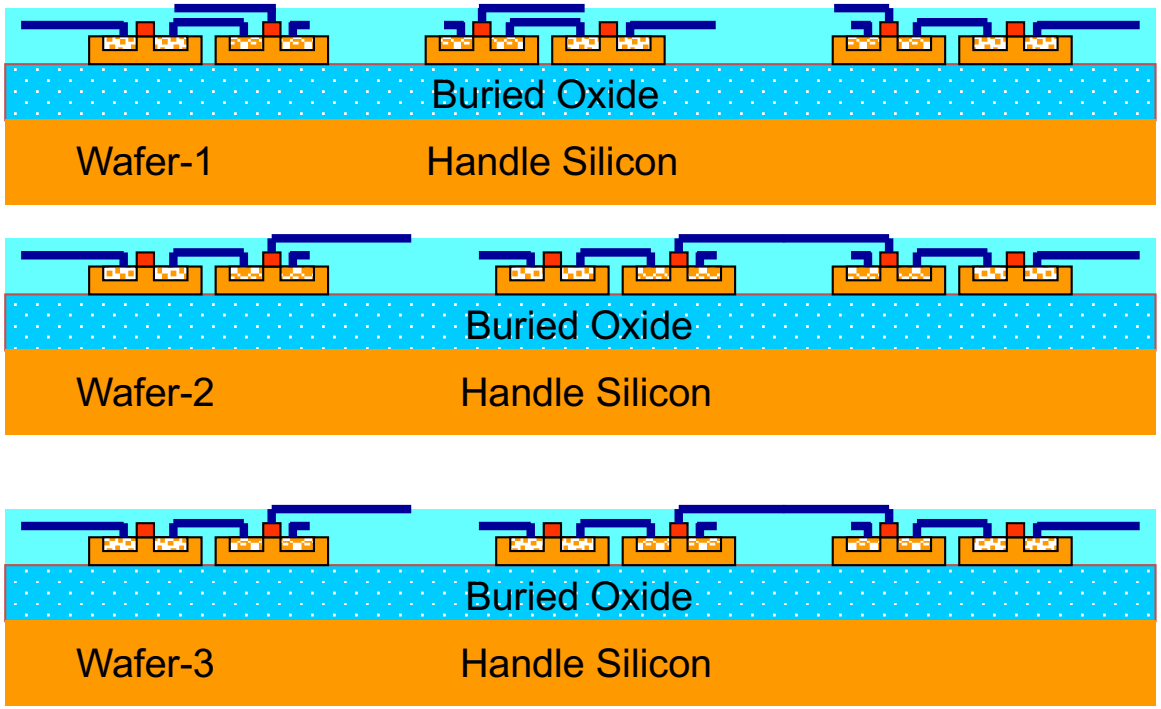


Back-to-Back

3-D Circuit Integration Flow-1

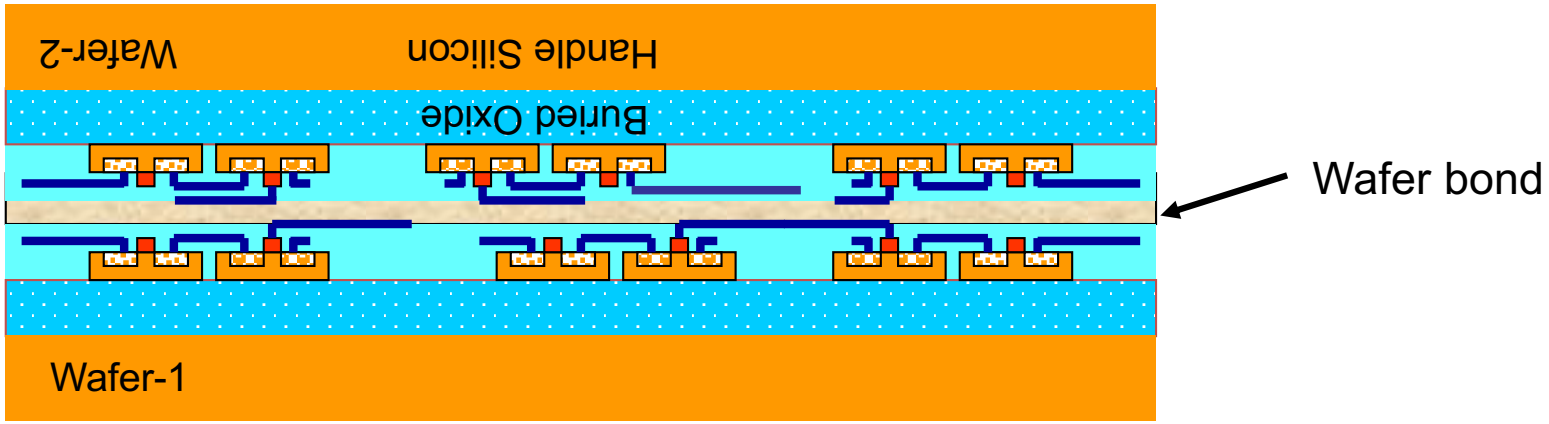
- Fabricate circuits on SOI wafers
  - SOI wafers greatly simplify 3D integration
- 3-D circuits of two or more active silicon layers can be assembled

Wafer-1 can be either Bulk or SOI

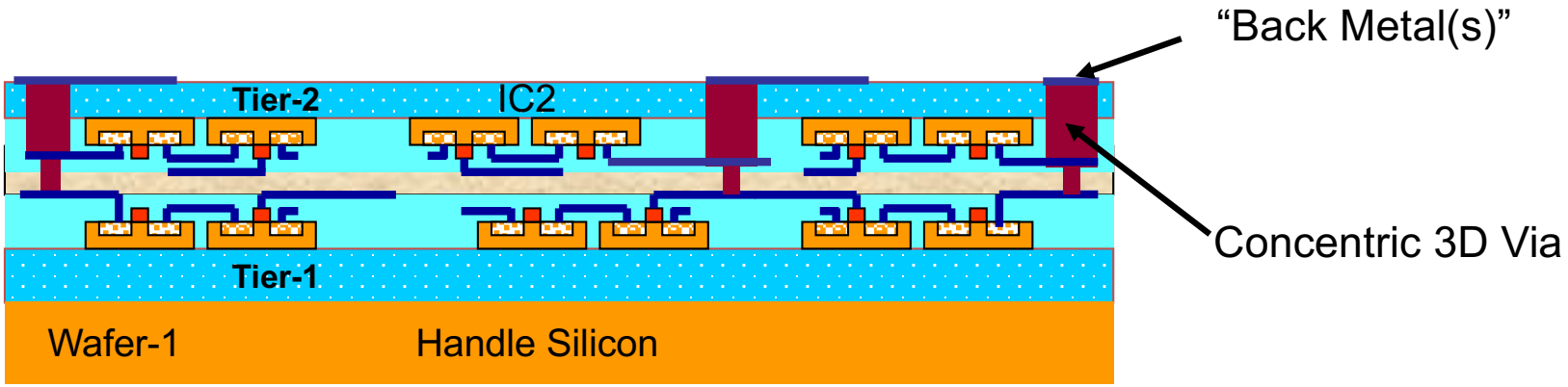


3-D Circuit Integration Flow-2

- Invert, align, and bond Wafer-2 to Wafer-1

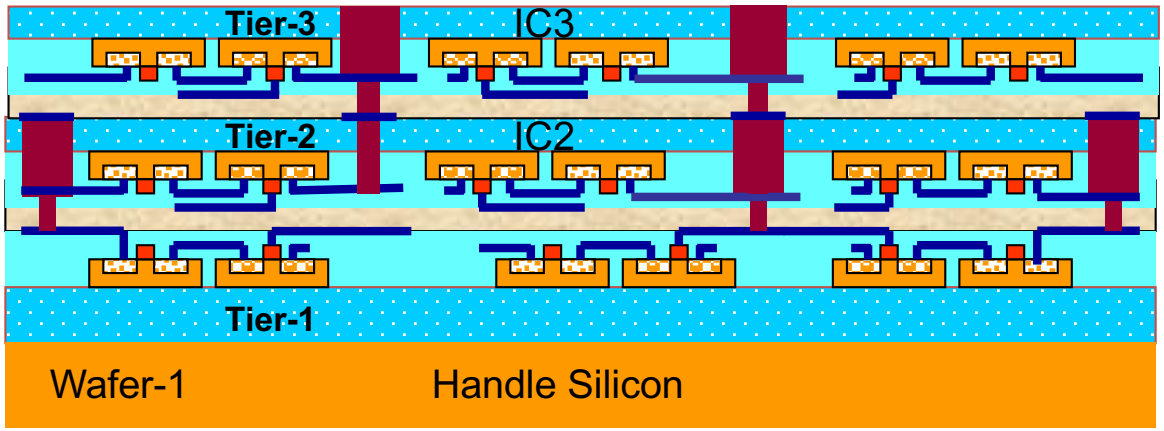


- **Remove handle silicon from Wafer-2, etch 3D vias, deposit and CMP damascene tungsten interconnect metal**

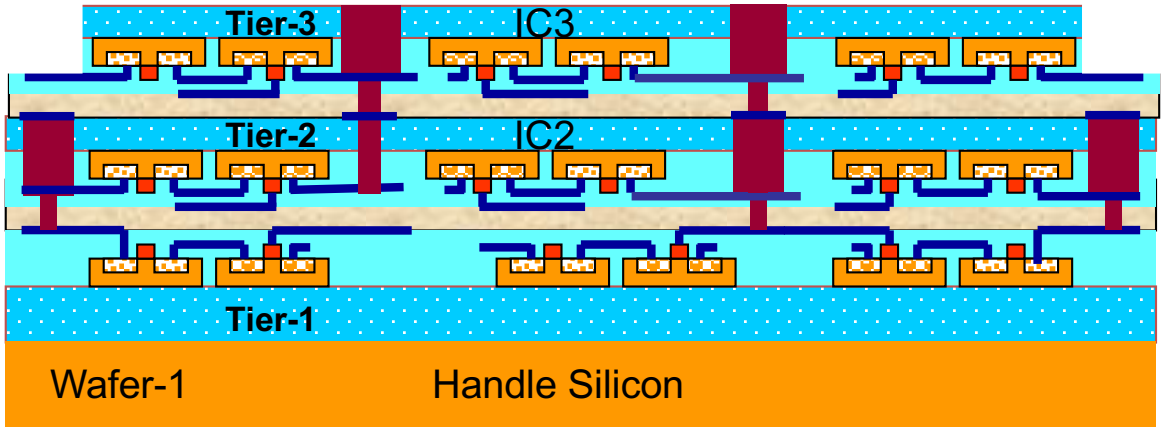


3-D Circuit Integration Flow-3

- Invert, align, and bond Wafer-3 to Wafer-2/1-assembly, remove Wafer-3 handle wafer, form 3D vias



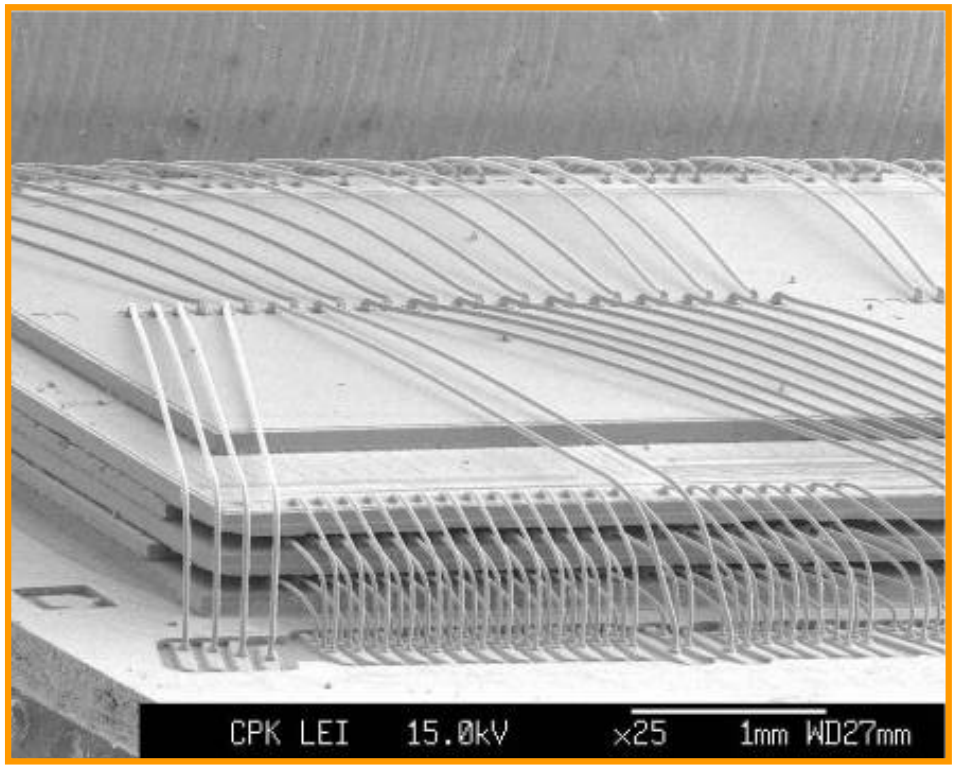
- **Etch Bond Pads**



IEEE Trans. on Electron Devices, Vol. 53, No. 10, October 2006

Pad-Level “3D Integration” *Die Stacking*

Stacked-Die Wire Bonding



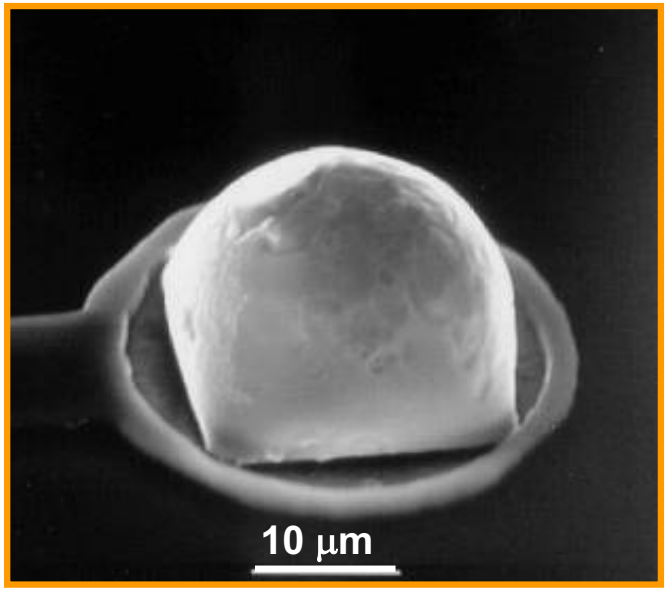
ChipPAC, Inc.

Stacked Chip-Scale Packages

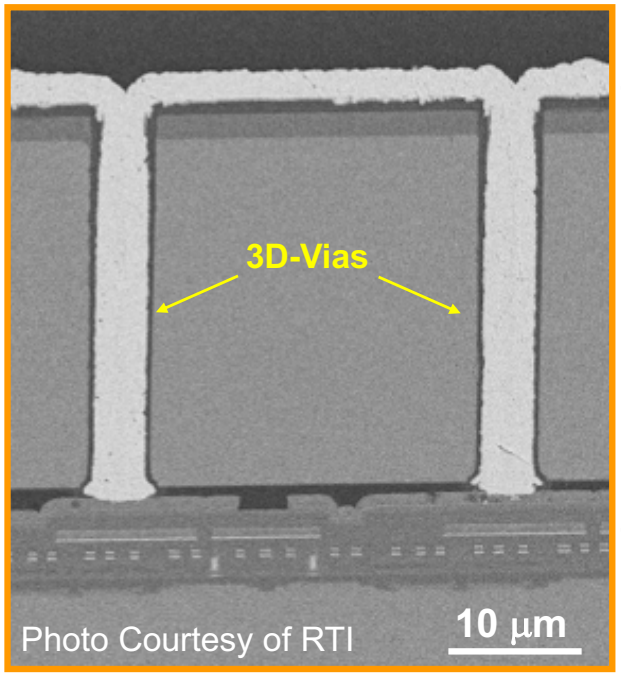
Tessera, Inc.

Approaches to High-Density 3D Interconnects

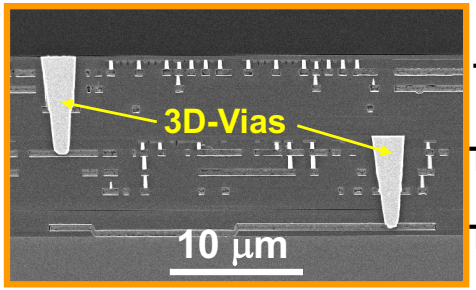
(Photos Shown to Scale)



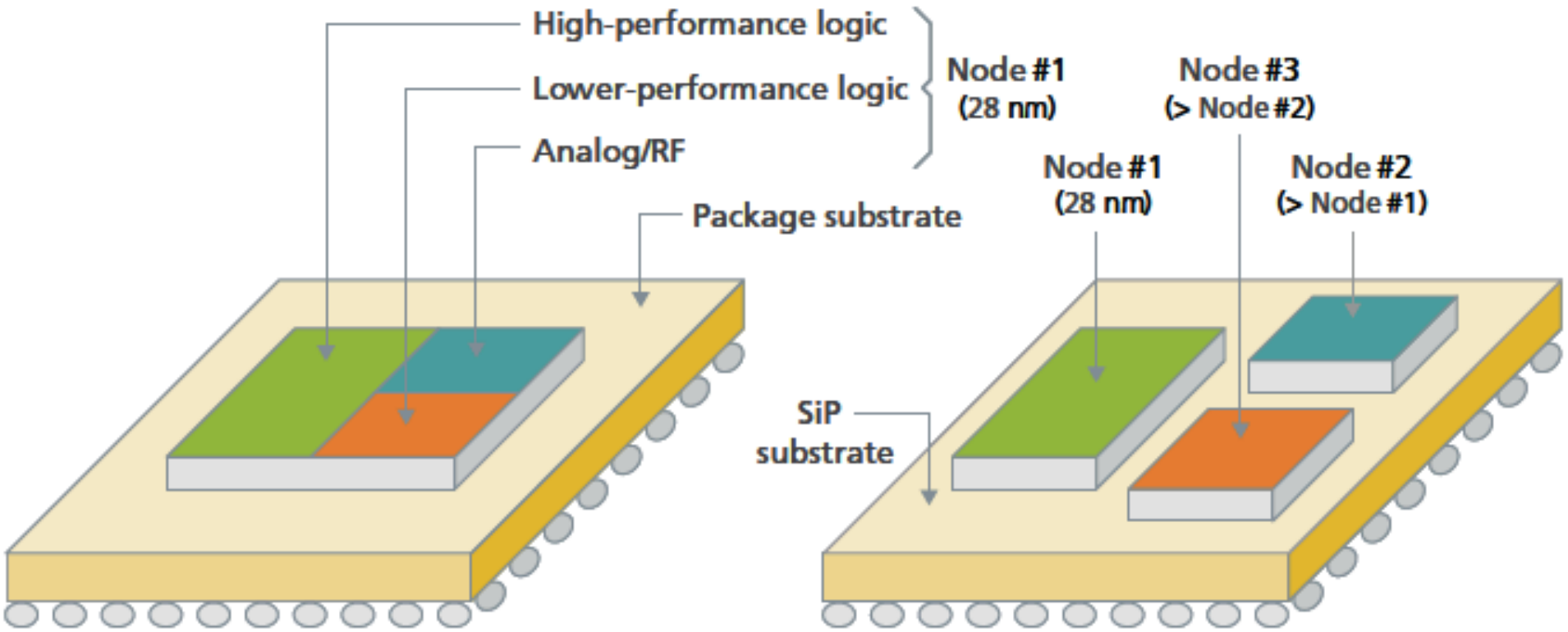
Bump Bond used to flip-chip interconnect two circuit layers



Two-layer stack with insulated vias through thinned bulk Si



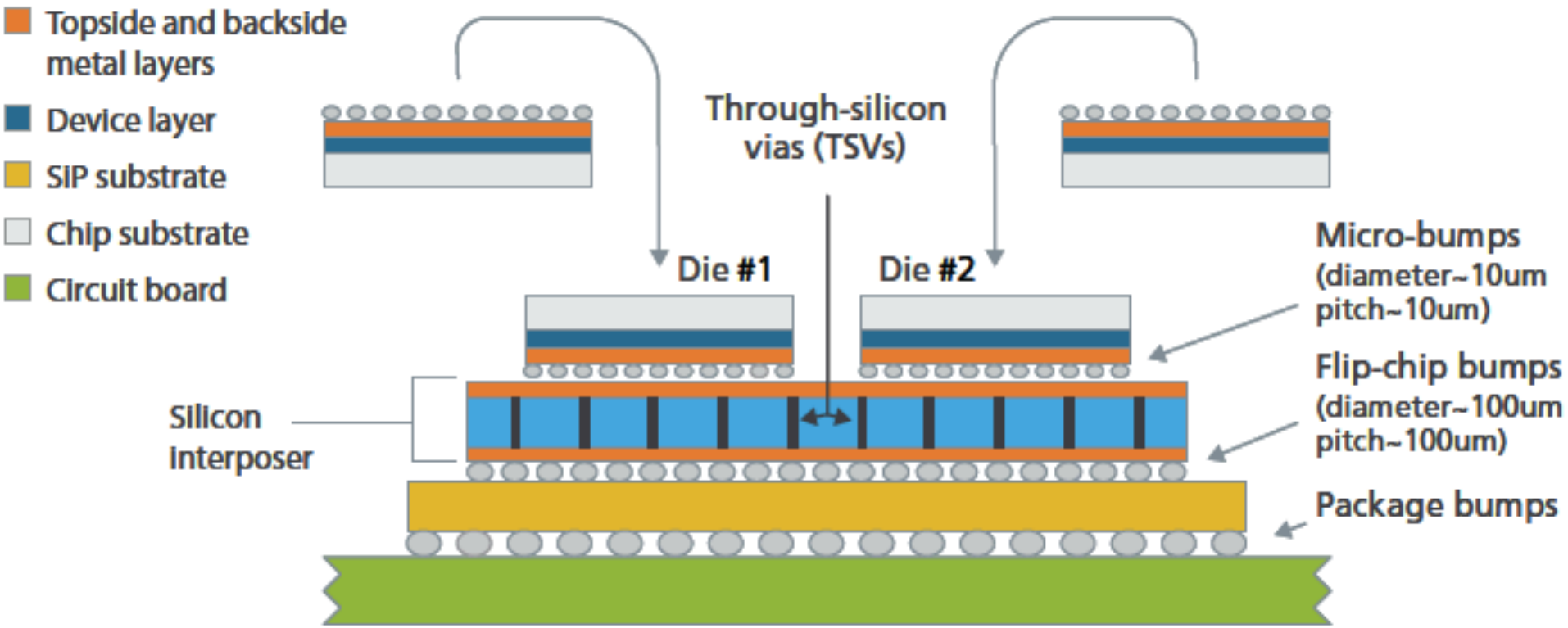
Three-layer circuit using MIT-LL's SOI-based vias



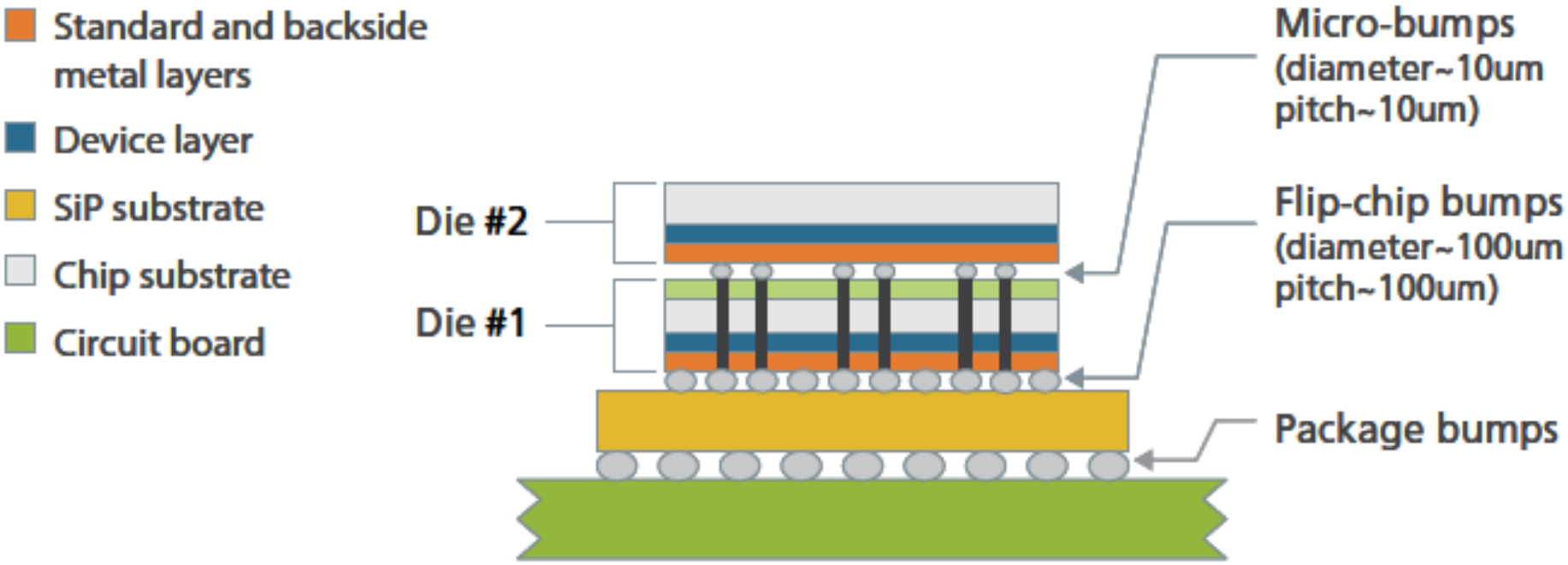
(a) SoC (single-chip package)

(b) SiP (multi-chip package)

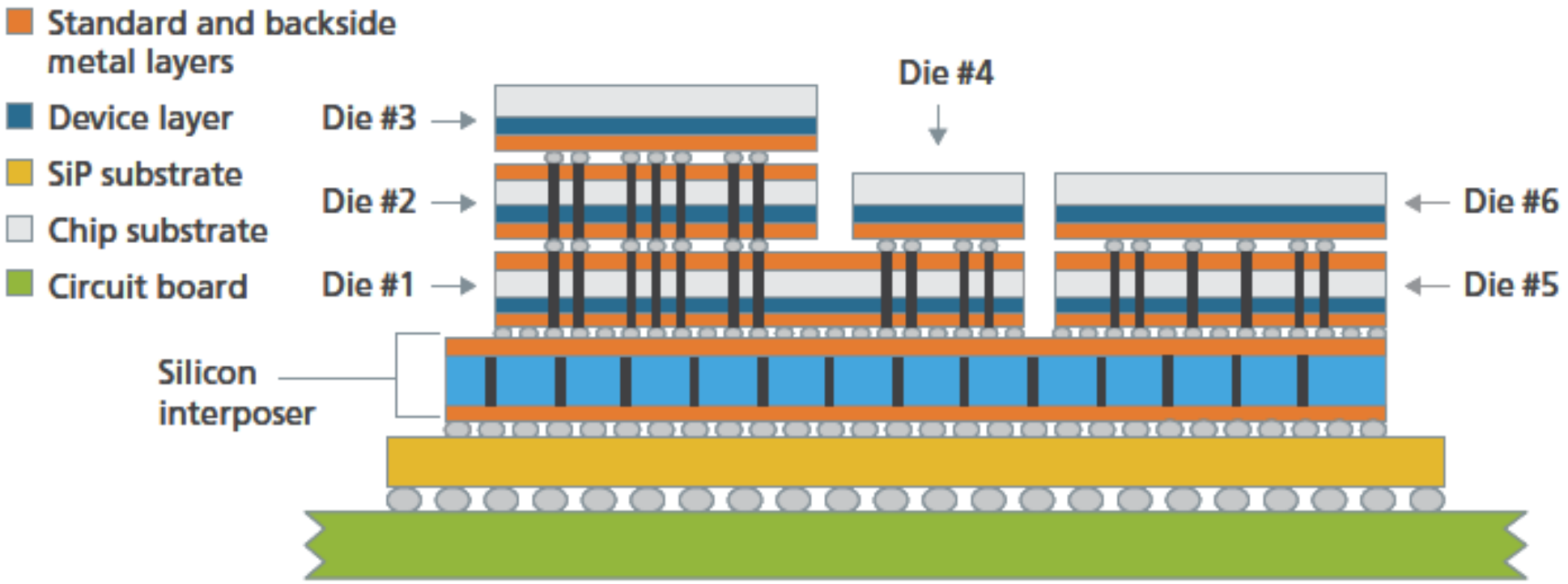
2.5D stacking – adding silicon interposer with TSVs



Simple 3D design with TSVs



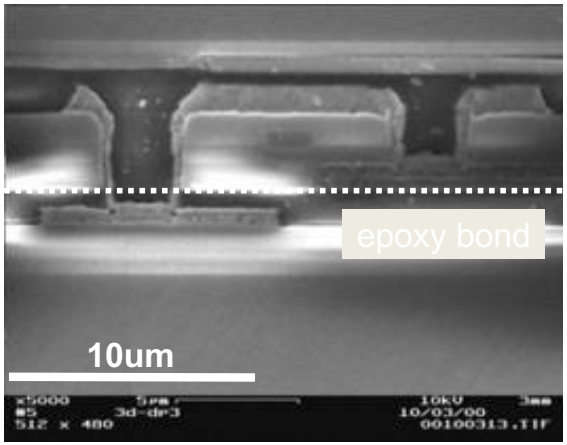
Complex 3D design with multiple dies and TSVs



MIT-LincolnLab 3D Via History

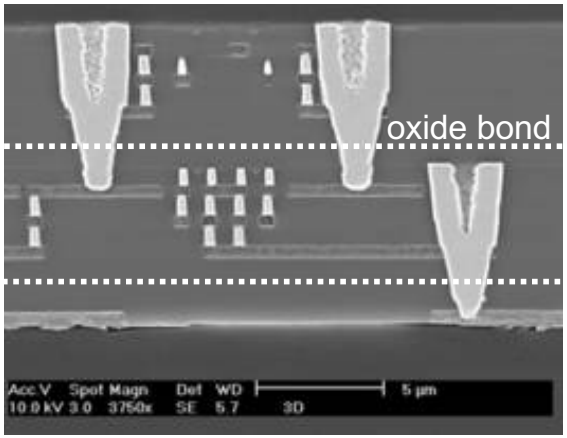
(Photos Shown with Same Scale and Drawn 3D Via Size)

3 μm
Oct 2000



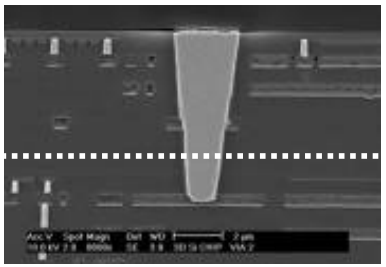
64 x 64, 12-μm active-pixel sensor[1]

2 μm
Dec 2004



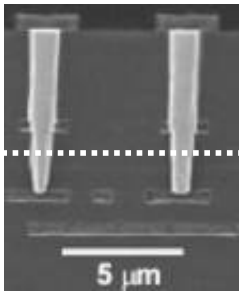
1024×1024, 8-μm pixel visible image sensor[2]

1.75 μm
May 2005



64 x 64, 50-μm pixel LADAR[3]

1.0 μm
Sept 2006



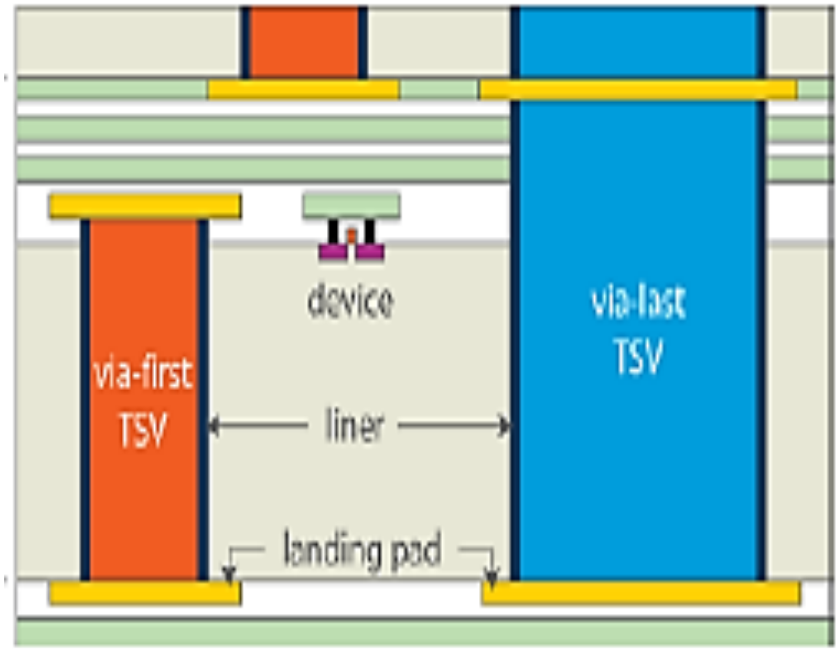
Scaled 3D via

[1] J. Burns, et al., "Three-dimensional integrated circuits for low-power high-bandwidth systems on a chip," in Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig., 2001, pp. 268-269.

[2] V. Suntharalingam, et al., "Megapixel CMOS image sensor fabricated in three-dimensional integrated circuit technology," in Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig., 2005, pp. 356-357.

[3] B. Aull, et al., "Laser radar imager based on three-dimensional integration of Geiger-mode avalanche photodiodes with two SOI timing-circuit layers," in Proc. Papers IEEE Int. Solid-State Circuits Conf. Tech. Dig., 2006, pp. 304-305.

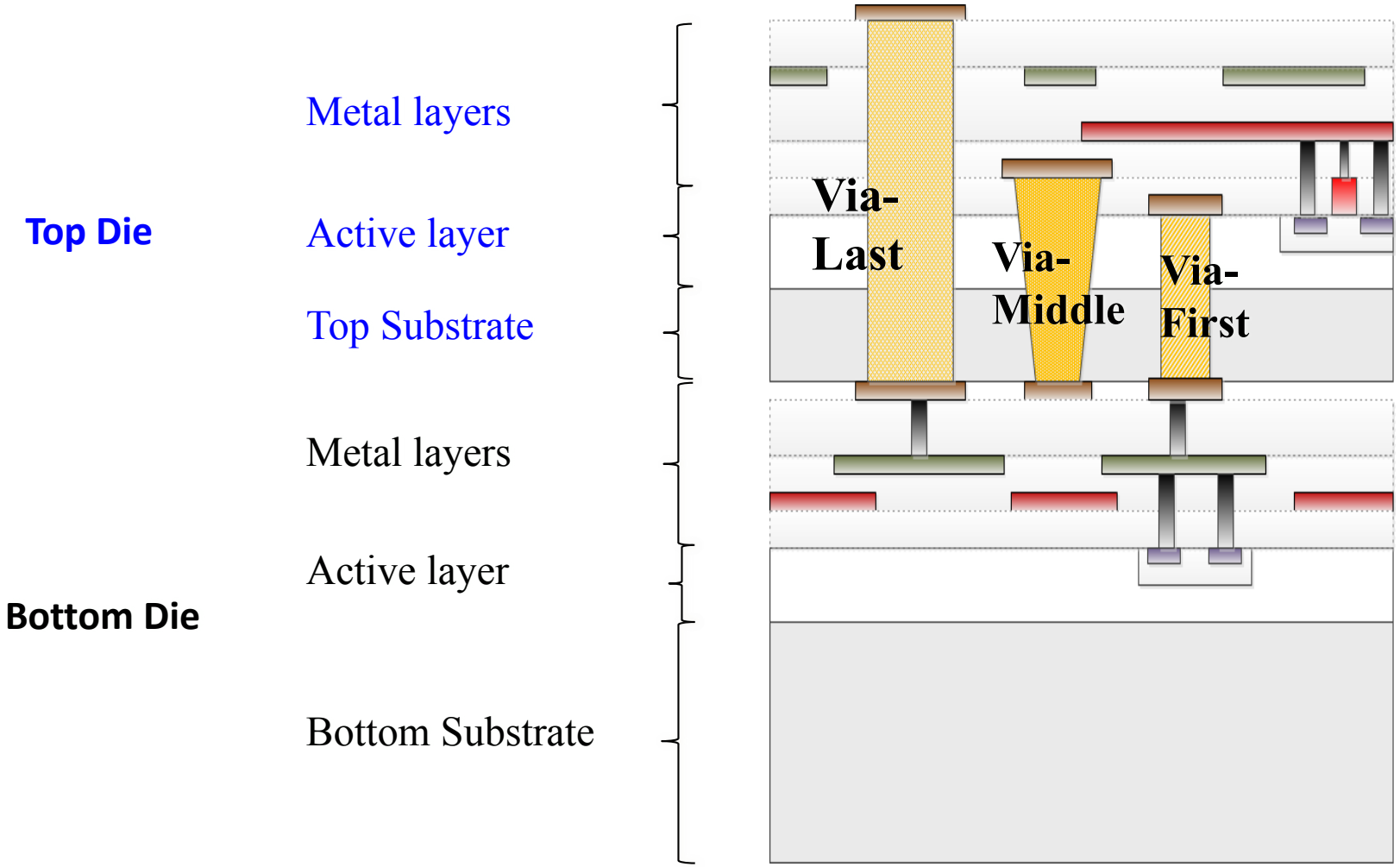
TSV Technology



- ***Via-First (Polysilicon filled)***
- - Process before CMOS front end steps
- - Pitch ~ 10µm
- - Density ~ 10000 TSV/mm^2
- - Limits active area for transistors
- ***Via-Middle (Copper filled)***
- - Process after CMOS front end steps
- - Pitch ~ 40-50µm
- - Density ~ 500 TSV/mm^2
- - Most Preferred (IBM, TI, TSMC, Samsung)
- ***Via-Last (Copper filled)***
- - Process after metallization
- - Pitch ~ 100µm
- - Density ~ 100 TSV/mm^2
- - Reliability issues in interconnects

Source: P. Garrou, 2007

TSV Types


Top Die
Metal layers
Active layer
Top Substrate
Metal layers
Active layer
Bottom Die
Bottom Substrate
Via-
Last
Via-
Middle
Via-
First

Comparison of Cu- & W- TSVs

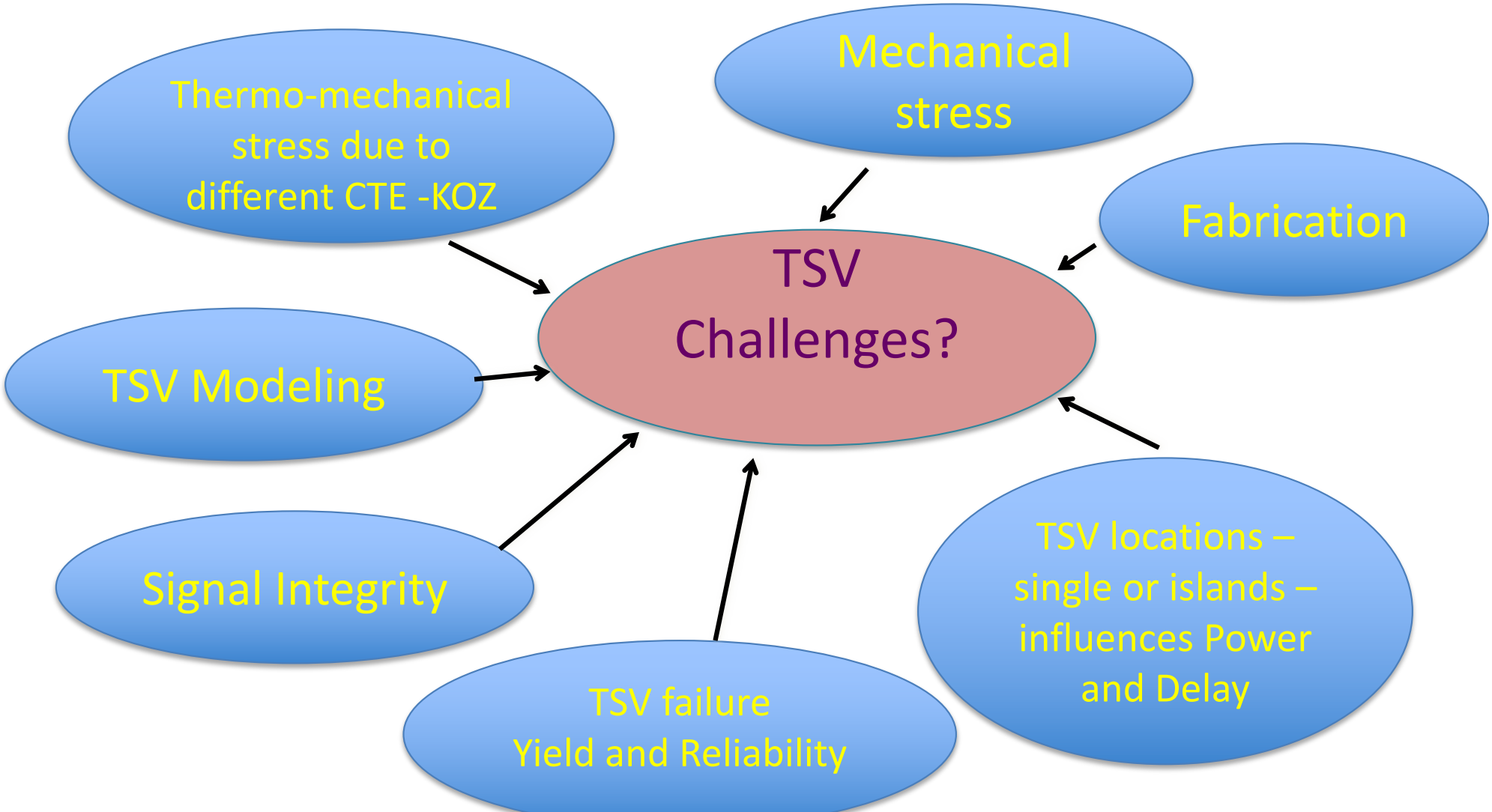
Properties	Tungsten	Copper
Resistivity (μΩ.cm)	12	3
CTE (ppm.K^{-1})	4.6	17
Deposition (^oC)	440-470	25
Maximum Aspect Ratio	30:1	12:1
Intrinsic Stress as deposited (MPa)	1400	20
Specific surface resistance for 100 μm deep TSV (Ω. $μm^2$)	28	3

Source: G. Parès,. IC Design & Technology (ICICDT), 2011 IEEE International Conference

Merging heterogeneous technologies ??

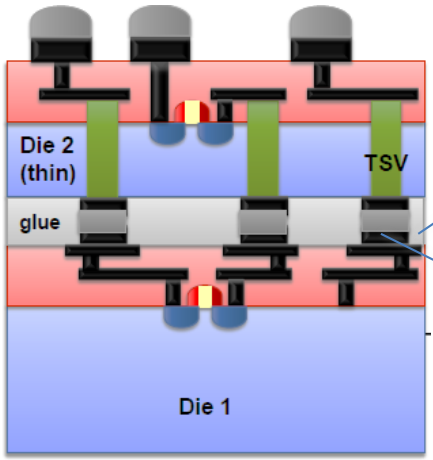
- Different processes in silicon !
- Different materials used
- Different connection techniques
- Different working conditions (temperature, humidity etc.)
- Chemical incompatibility
- Electrical incompatibility
- Operating conditions (voltages, temperature etc.)

TSVs – challenges (all temperature dependent)

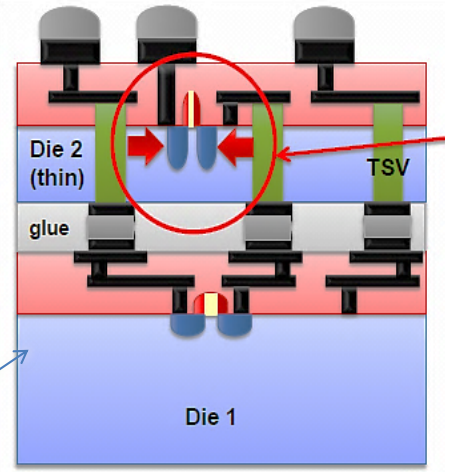


TSV Thermo-mechanical Stress

- Thermal Mismatch
- - Silicon CTE: 3.05 ppm
- - Copper CTE: 17.7 ppm



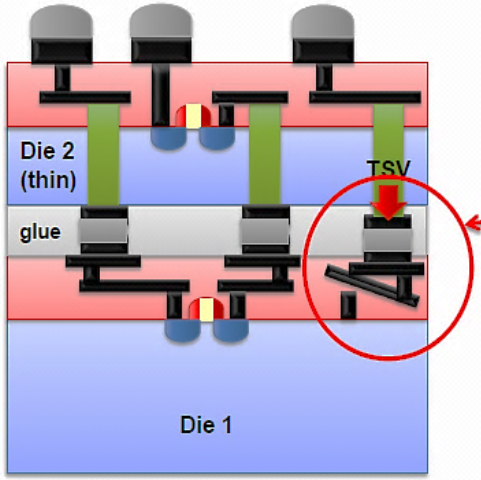
Stress Affects Transistor Performance



Transistor -
Squeezed or Stretched

Material deformation leads to mobility & threshold voltage change

Stress Affects Interconnects Reliability



Interconnects
Squeezed or Stretched

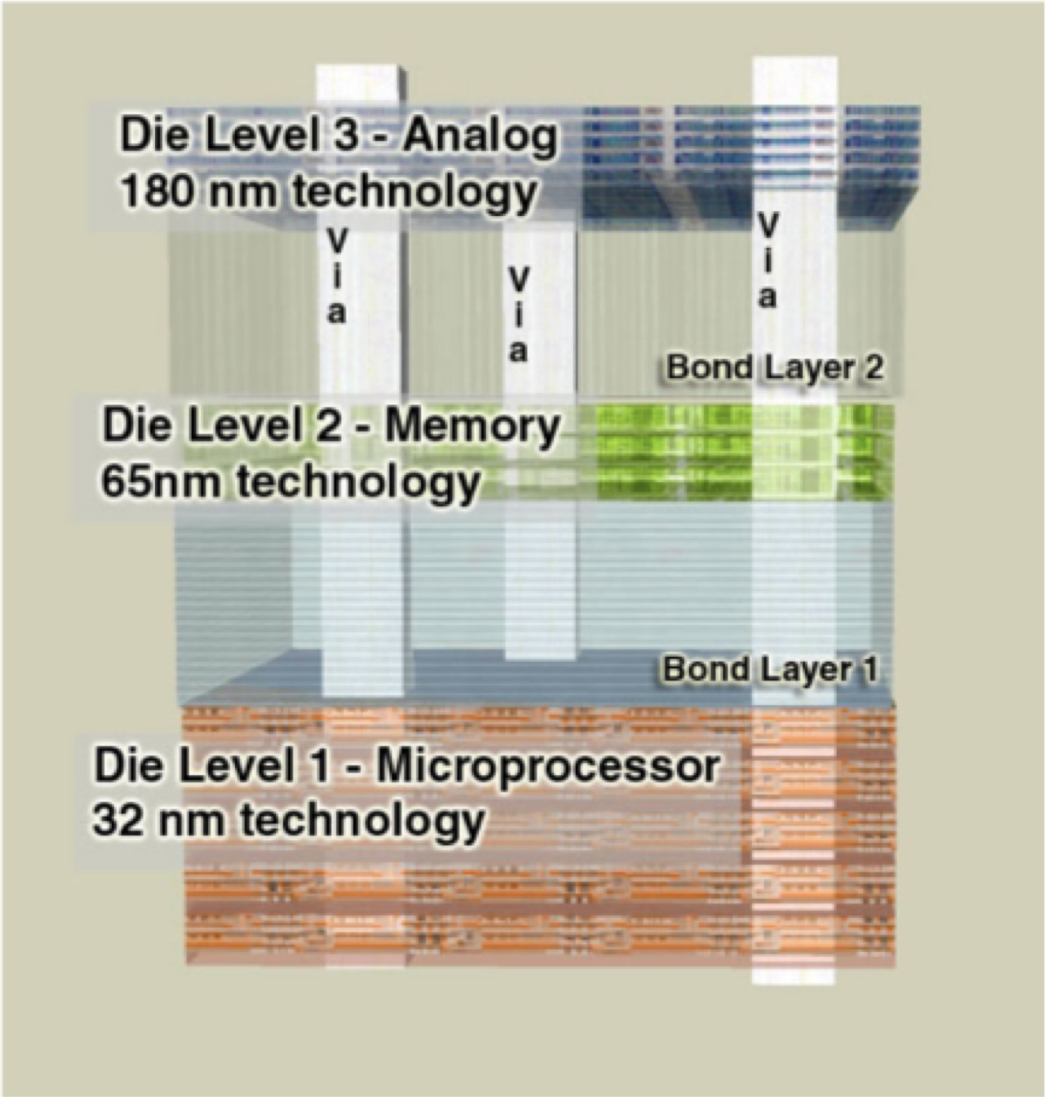
Source: J. Kawa, DATE 2010

What we mean by heterogeneous technologies ??

- Different processes in silicon !
- Different materials used
- Different connection techniques
- Different working conditions (temperature, humidity etc.)
- Chemical incompatibility
- Electrical incompatibility
- Operating conditions (voltages, temperature etc.)

3D ICs with Through Silicon Vias
Merging different silicon technologies

- Used in 2.5 and 3D ICs
- Increased performance due to reduced interconnect length
- Commercial applications: sensors, memory, FPGAs and others continue to emerge



Further developments in 3-D Integration

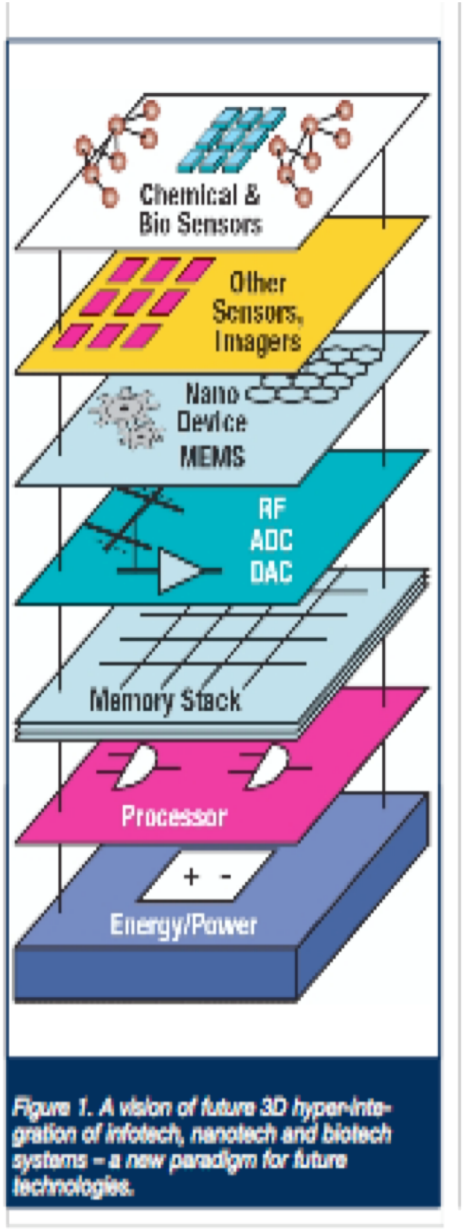


Figure 1. A vision of future 3D hyper-integration of infotech, nanotech and biotech systems – a new paradigm for future technologies.

- Chemical and Bio Sensors
- Other Sensors, Imagers
- Nano Device MEMS
- RF, ADC, DAC
- Memory Stack
- Processor
- Energy/Power

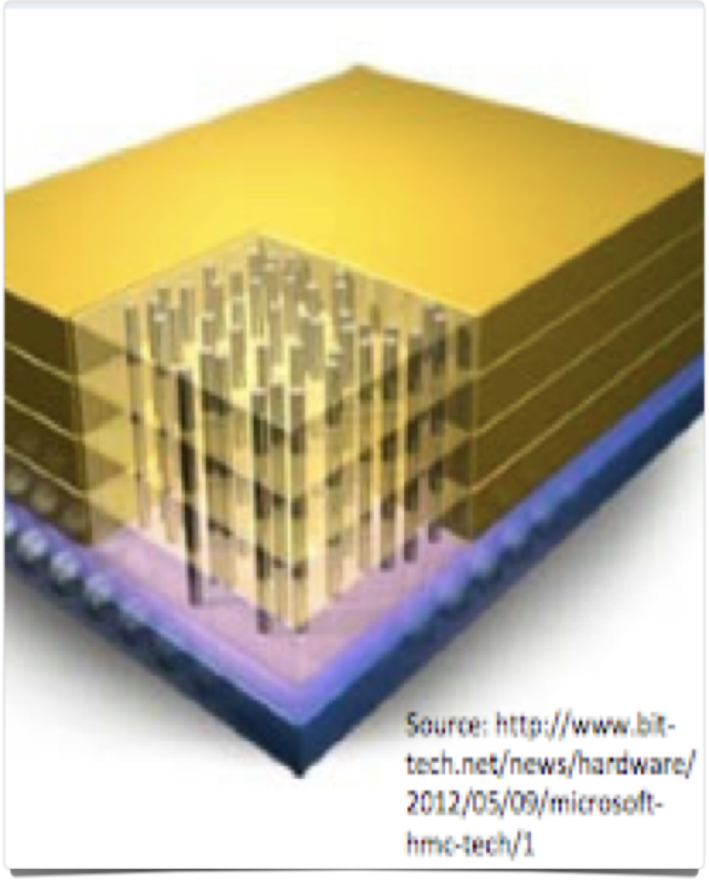
New technologies come to play

What important parts not available in silicon could be introduced in 3D technologies?

1. Nano-layers built for new functionalities
2. Energy harvesting + storage devices
3. Integrated cooling systems
4. Many others eg. Bio, organic, optical etc.

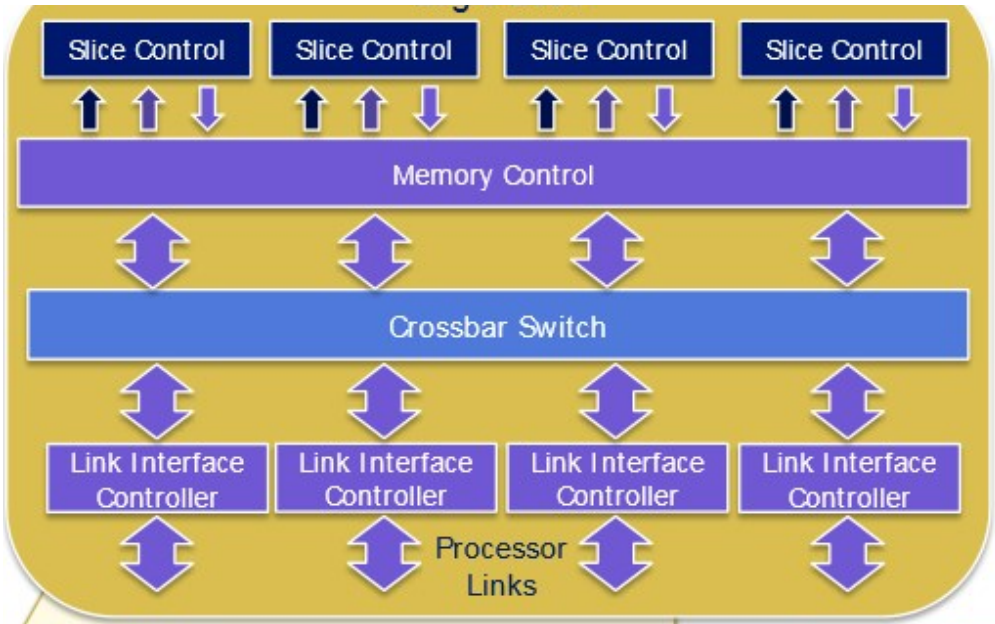
Hybrid Memory Cube

- High speed logic levels
- allows for different flavors of technology (spin-torque, memristor and others)
- a stack of TSV bonded memory die
- Improved memory bandwidth-performance
- decreased energy and latency



http://media2.hpcwire.com/hpcwire/Micron_hmc_layers_w_labels.jpg

Industrial developments - HMC

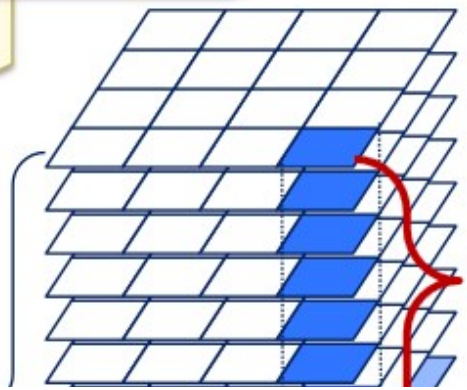


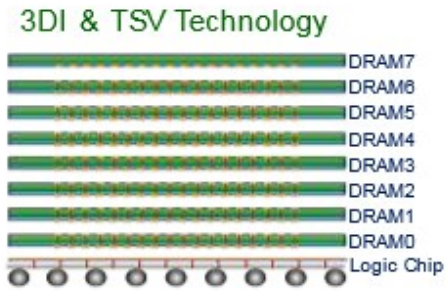
Logic Base

- Wide, high-speed local bus for data movement
- Advanced memory controller functions
- DRAM control at memory rather than distant host controller
- Reduced memory controller complexity and increased efficiency

Add sophisticated switching and optimized memory control…

And now we have a whole new set of capabilities





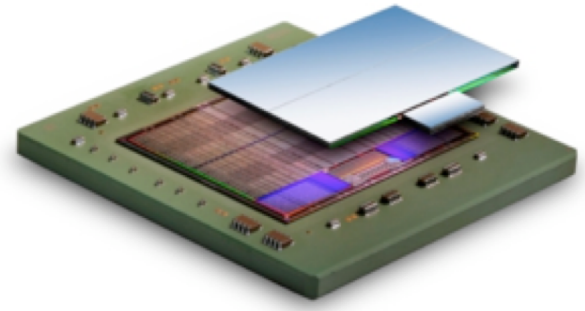
Vertical Slices are managed to maximize overall device availability

- Optimized management of energy and refresh
- Self test, error detection, correction, and

Xilinx's Virtex-7 H580T FPGA

- Equivalent to 20 million ASIC gates,
  - ideal for system integration,
  - ASIC replacement,
  - and ASIC prototyping and emulation.
- capacity is made possible by connecting the FPGAs to each other
  - Xilinx's Stacked Silicon Interconnect technology.
  - "silicon interposer" combined with TSVs.
  - Interposer provides connections between FPGAs and to the chip package

Announcements of the first shipments in May 2012.



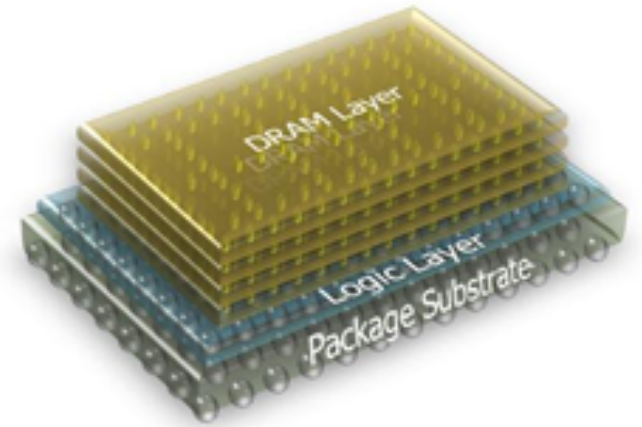
https://www.eetimes.com/ContentEETimes/Images/Design/Max-Stuff/2012-05/Virtex-7-H580T-02a.jpg

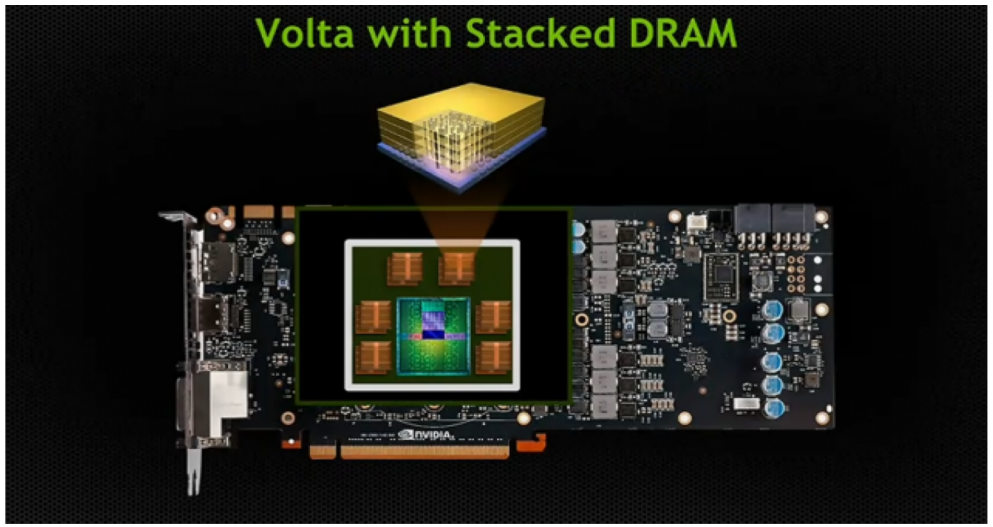
The Virtex-7 H580T
2 FPGA dice and one 8-channel 28Gbps

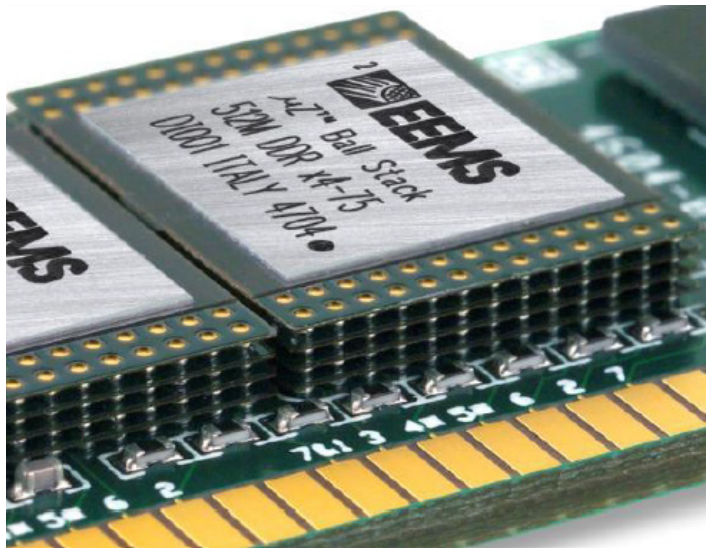
The Virtex-7 2000T -4 FPGA dice

Stratix 10 Family device, 10GX5500/10SX5500	17,000,000,000	2017	Intel (formally Altera)	14 nm	560 mm^2

Industrial developments







61-core Xeon Phi	5,000,000,000	2012	Intel	22 nm	720 mm²
Vega 10	12,500,000,000	2017	AMD	14 nm	484 mm²
GP100 Pascal	15,300,000,000	2016	Nvidia	16 nm	610 mm²
GV100 Volta	21,100,000,000	2017	Nvidia	12 nm	815 mm²
Stratix 10 Family device, 10GX5500/10SX5500	17,000,000,000	2017	Intel (formally Altera)	14 nm	560 mm²
32-core AMD Epyc	19,200,000,000	2017	AMD	14 nm	4× 192 mm²

Heterogeneity

is the key to future developments

New materials apart from silicon!!

Are comming into the picture

(graphene, carbon nanotubes, optical devices, mocelules, proteins, DNA, materials based on different chemicals, and many others)

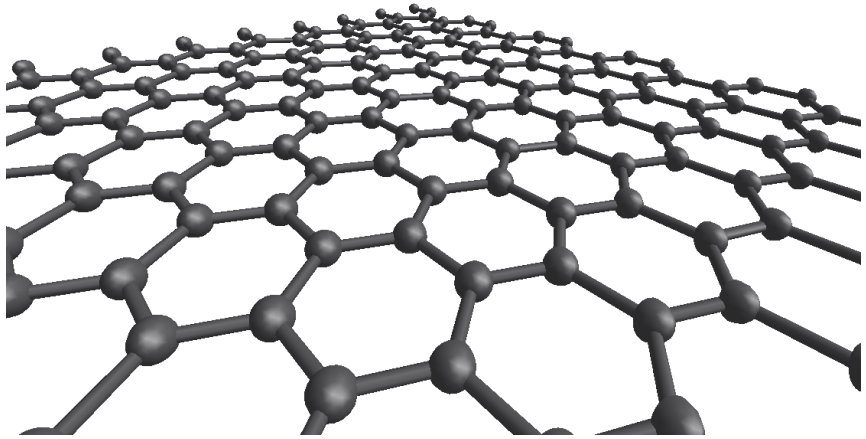
Graphene

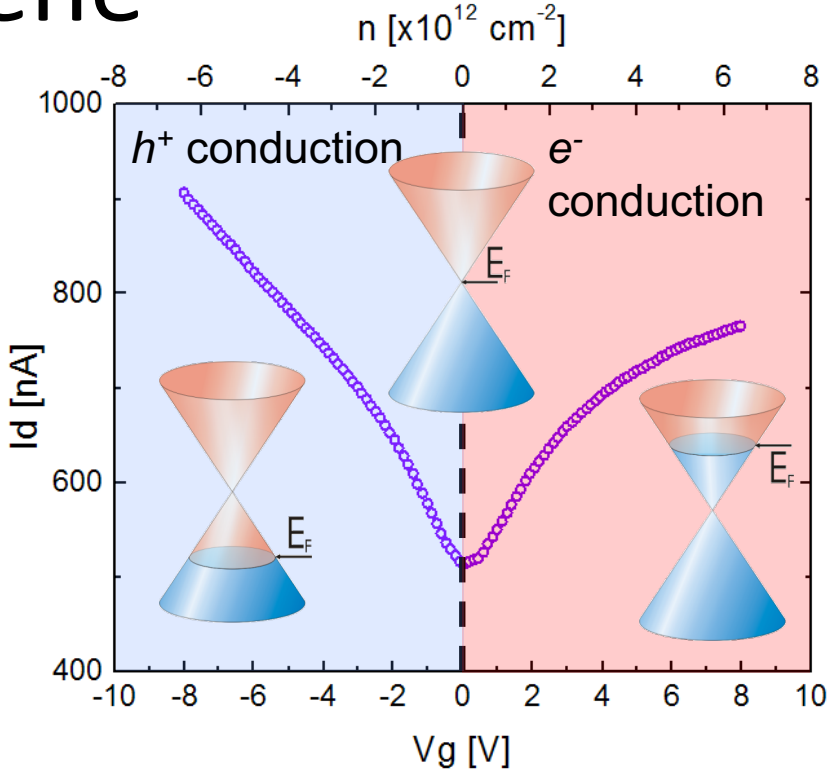
Electric Field Effect in Atomically Thin Carbon Films

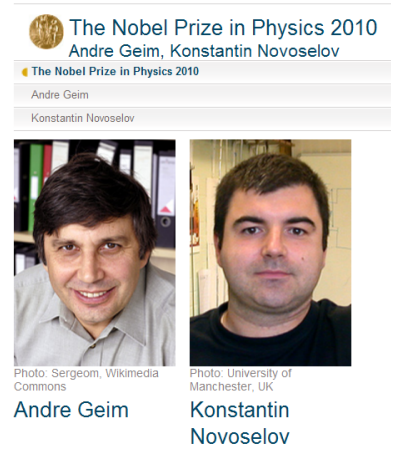
K. S. Novoselov,[1] A. K. Geim,[1]* S. V. Morozov,[2] D. Jiang,[1]
Y. Zhang,[1] S. V. Dubonos,[2] I. V. Grigorieva,[1] A. A. Firsov[2]

We describe monocrystalline graphitic films, which are a few atoms thick but are nonetheless stable under ambient conditions, metallic, and of remarkably high quality. The films are found to be a two-dimensional semimetal with a tiny overlap between valence and conductance bands, and they exhibit a strong ambipolar electric field effect such that electrons and holes in concentrations up to 10^{13} per square centimeter and with room-temperature mobilities of ~10,000 square centimeters per volt-second can be induced by applying gate voltage.

22 OCTOBER 2004 VOL 306 SCIENCE www.sciencemag.org



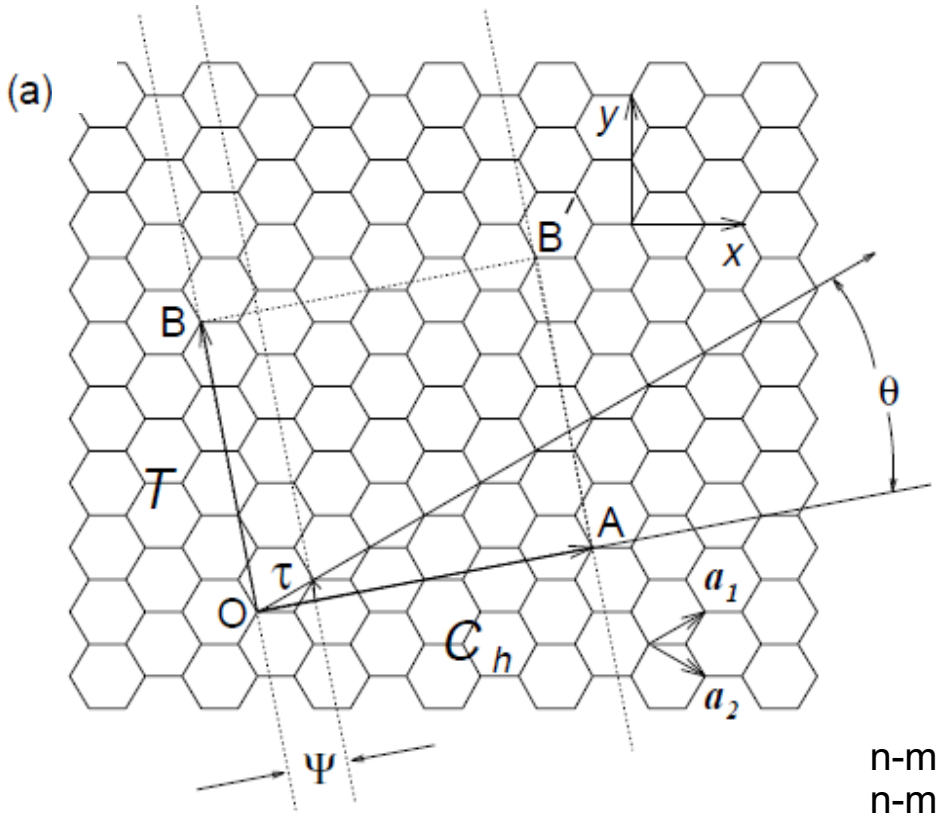


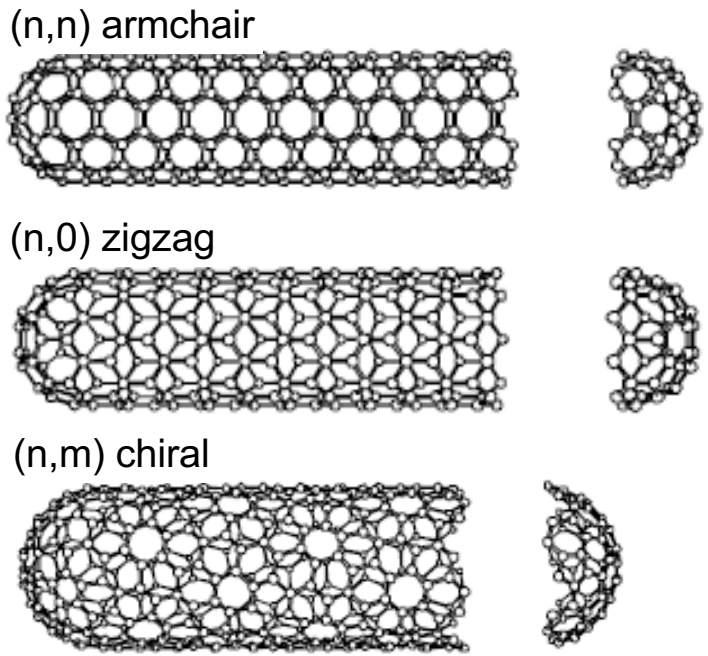


The Nobel Prize in Physics 2010 was awarded jointly to Andre Geim and Konstantin Novoselov *"for groundbreaking experiments regarding the two-dimensional material graphene"*

Carbon nanotubes

SWNTs are obtained by wrapping a graphene sheet along chiral directions





n-m=3k, k integer →metallic SWNTs
n-m=3k±1, k integer →semiconducting SWNTs
(n,n) armchair SWNTs always metallic
(n,0) zigzag SWNTs metallic if n is multiple of 3

Statistically, in a random mixture 1/3 SWNTs are metallic and 2/3 are semiconducting.

Dresselhaus et al., Top. Appl. Phys. **80**, 1 (2001)

CNT Properties

- Electrical conductivity higher than copper, in graphene electrons can move as fast as 2000 times quicker then in silicon!

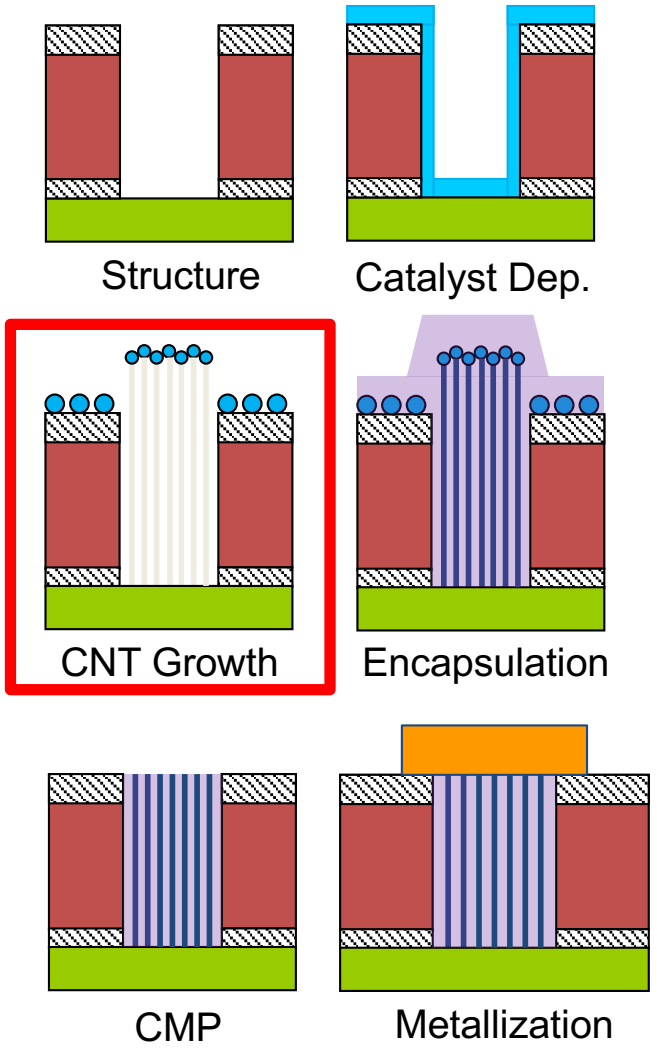
- Can be metallic or semiconducting depending on chirality (m-n)/3 electronic properties can be tailored through application of external magnetic field, application of mechanical deformation…
- CNT exhibits extraordinary mechanical properties: Young's modulus over 1 Tera Pascal, as stiff as diamond, and tensile strength ~ 200 Gpa.
- Very high current carrying capacity (10^7 - 10^9 A/cm^2) (charge transport is ballistic – not diffusive as in normal wire)
- Excellent field emitter; high aspect ratio and small tip radius of curvature are ideal for field emission

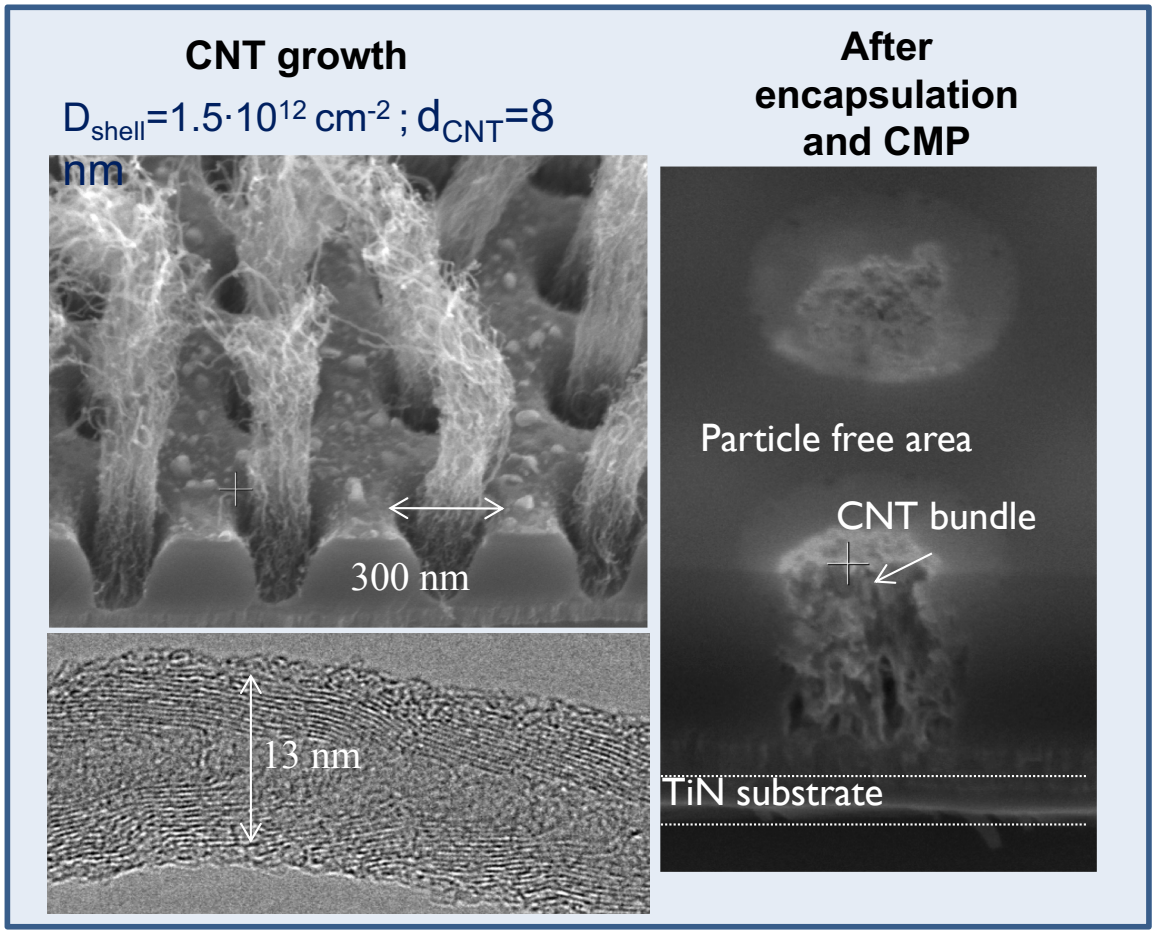
- Other chemical groups can be attached to the tip or sidewall (called 'functionalization')

See textbook on
Carbon Nanotubes: Science and Applications,
M. Meyyappan,
CRC Press, 2004.

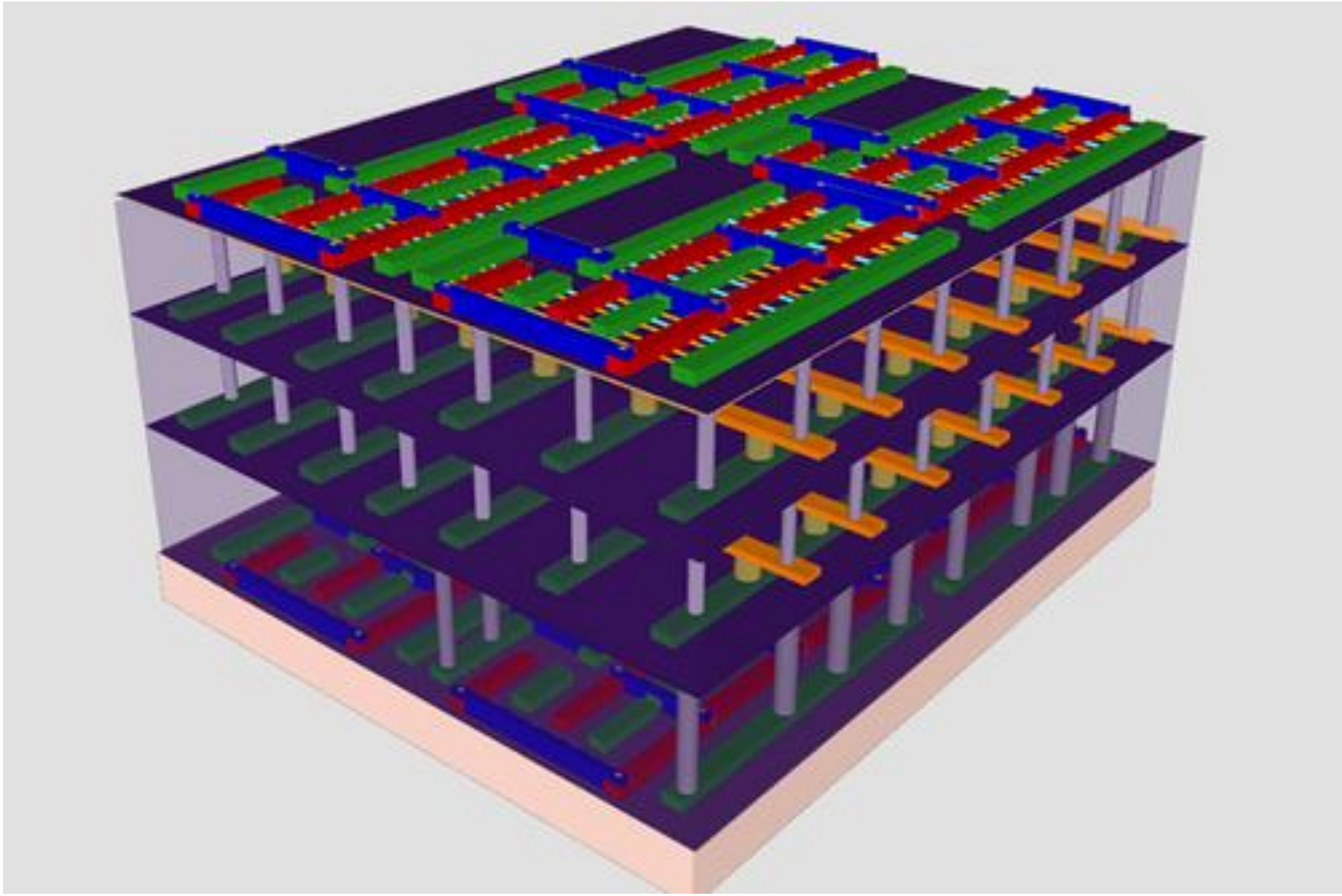
Vertical interconnects with CNTs

Carbon nanotubes can be used in the BEOL for interconnects.





Chiodarelli N. et al., J. Electrochem Soc, 157 (10) (2010)



Source: Subhasish Mitra Stanford University

How about an integrated circuit without external power supply?

What is needed to build a self-powered circuit?

- Energy storage – battery
- Power back-up – capacitor/efficient ways of storing the energy to be used during the periods of inactivity when the battery can not be loaded?
- A way to load the device !

To produce an energy storage device

(same applies also to batteries!)

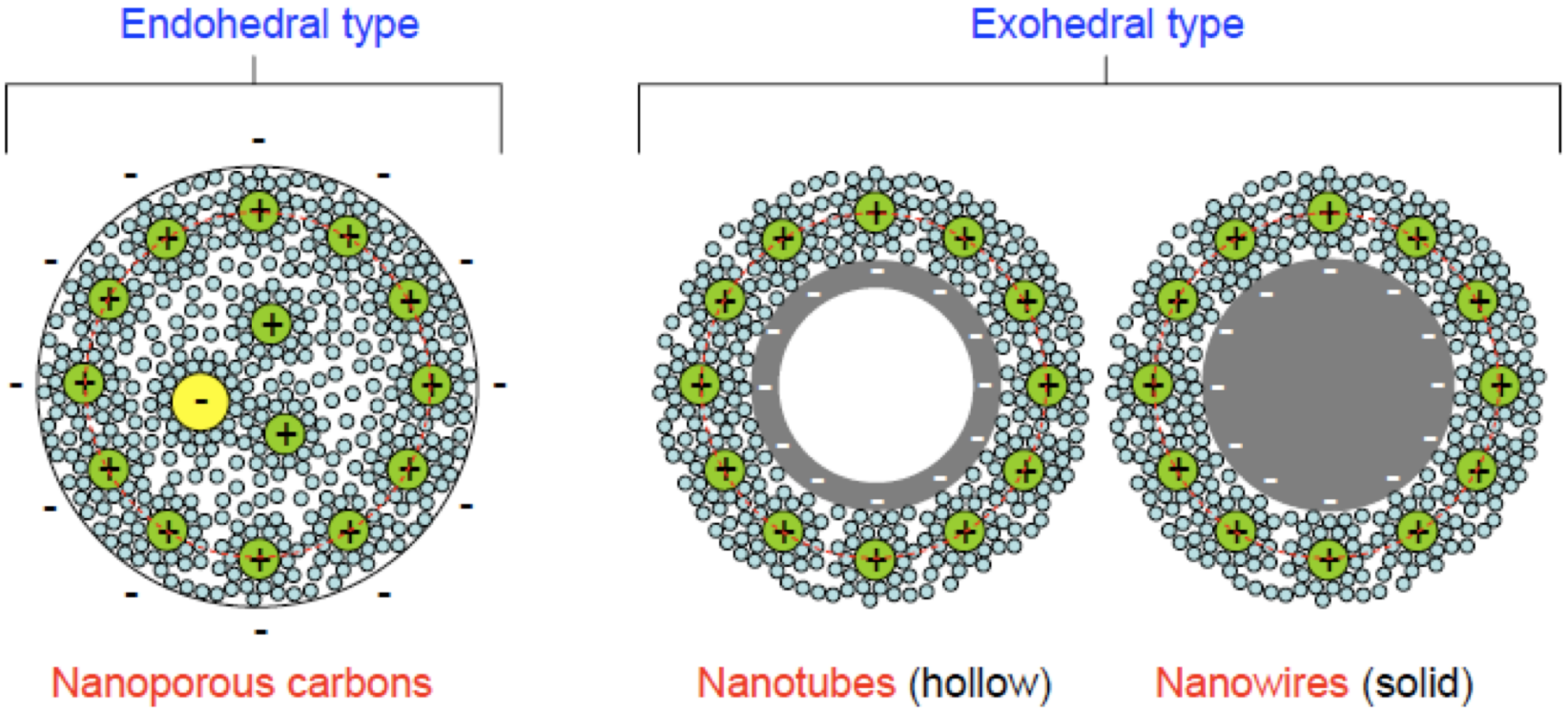
we have to squeeze

very large area electrodes

in an

extremely small volume

How to make a capacitor using one of the new technologies?



With double layer formed in the pores, it should be a double cylinder capacitor, not a parallel plate capacitor.

Huang, J.; Sumpter, B. G.; Meunier, V. ***Angew. Chem. Int. Ed***. 2008, *47*, 520.

nature nanotechnology
LETTERS
CORRECTED ONLINE: 31 MARCH 2009
PUBLISHED ONLINE: 15 MARCH 2009 | DOI: 10.1038/NNANO.2009.37

Nanotubular metal–insulator–metal capacitor arrays for energy storage

Parag Banerjee[1,2], Israel Perez[1,2], Laurent Henn-Lecordier[1,2], Sang Bok Lee[3,4]* and Gary W. Rubloff[1,2,5]*

NATURE NANOTECHNOLOGY DOI: 10.1038/NNANO.2009.37

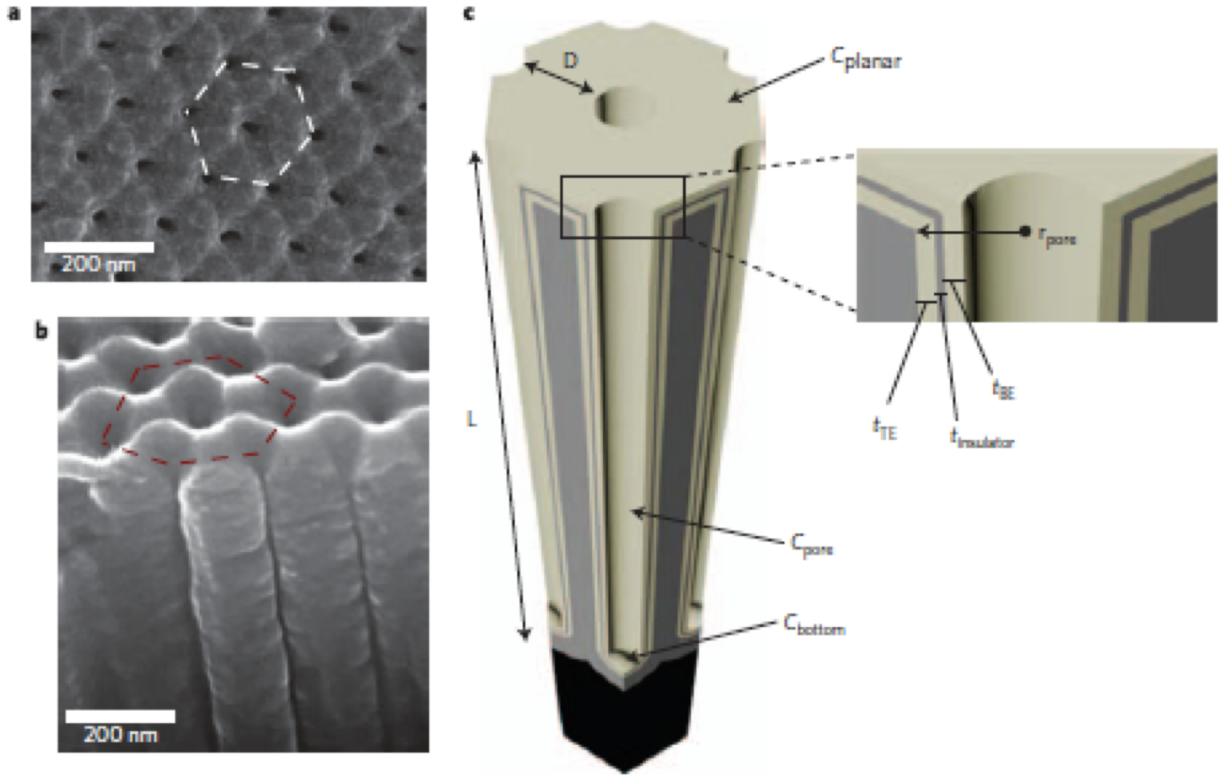


Figure 3 | Relationship between MIM nanotubular structure and the parameters used to calculate total capacitance. **a**, Plan-view SEM of an AAO MIM structure showing the hexagonal unit cell. **b**, Cross-section of the sample in **a**. **c**, Schematic of a unit cell of an AAO MIM capacitor defining the various parameters used to compute total capacitance of the structure. Here, t_{TE} is the thickness of the top electrode (TE), $t_{insulator}$ is the thickness of the insulating film, t_{BE} is the thickness of the bottom electrode (BE), r_{pore} is the radius of the pore, D is the interpore edge-to-edge distance and L is the depth of the pores. The contribution to total capacitance comes from the sum of the top planar part C_{planar}, the cylindrical region of the pore C_{pore}, and the bottom part of the pore C_{bottom}, next to the barrier layer.

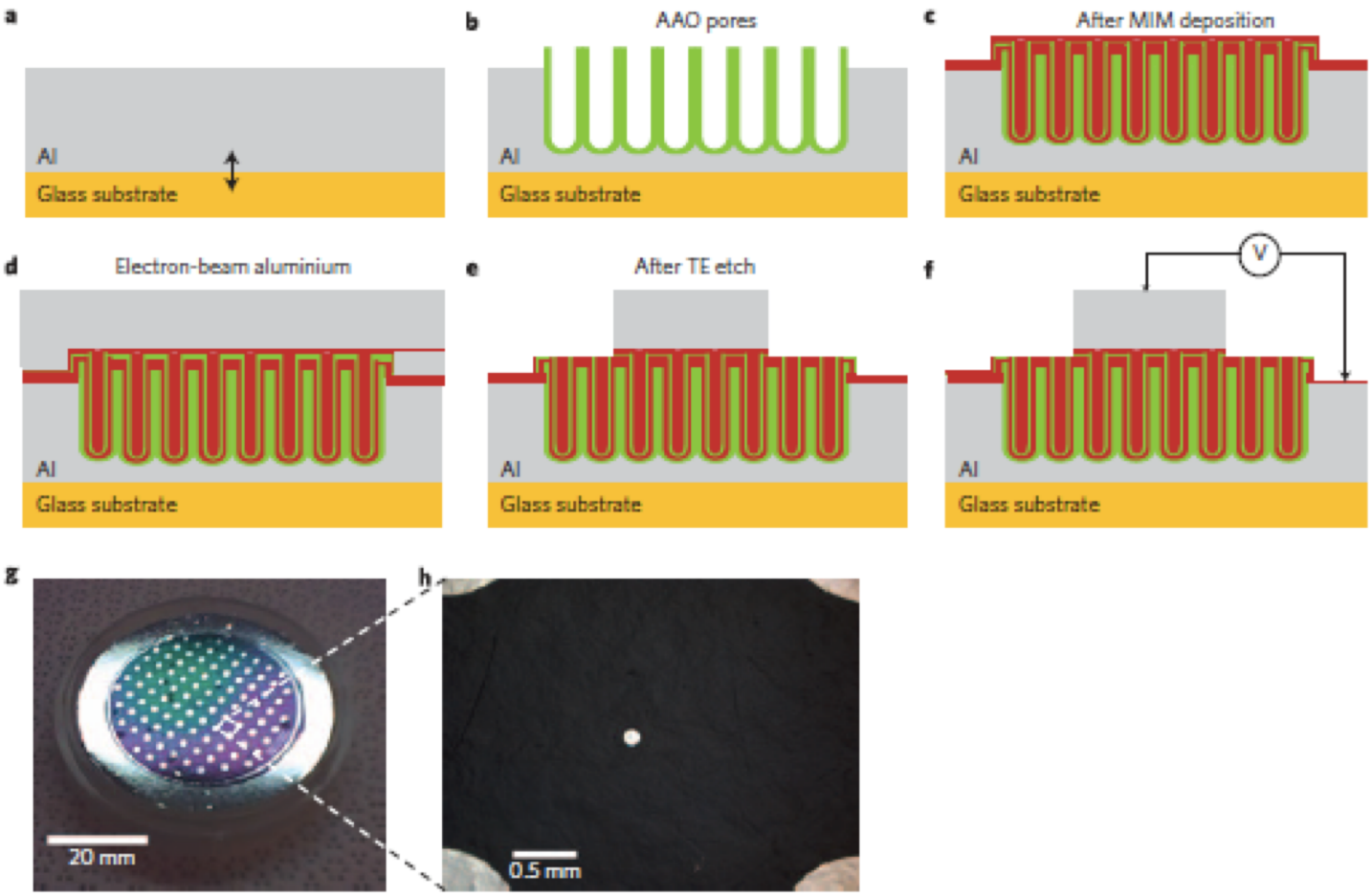
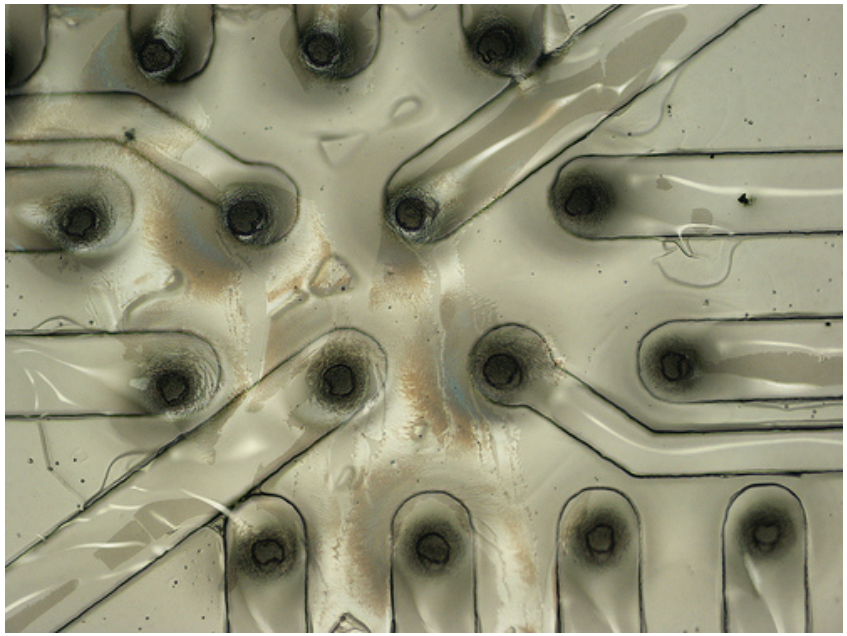


Figure 4 | Process sequence to prepare MIM capacitors. **a**, Al foil is anodically bonded to a glass substrate. **b**, AAO pore formation. **c**, MIM deposition via ALD processes. **d**, Electron-beam Al is deposited on top. **e**, Photolithography, masking and etching of the Al electrode, then the top electrode (TE) TiN, to define the capacitor area. **f**, Electrical testing using the Al foil (which is in contact with the bottom electrode TiN) as a back contact and electron-beam Al as the top contact. **g**, Two-inch wafer with capacitors of different areas defined on the surface. **h**, A blown-up image of an actual 'dot' capacitor tested. Each such dot capacitor is 125 μm wide and contains $\sim 1 \times 10^6$ nanocapacitors.

- Single nano-capacitor of diameter

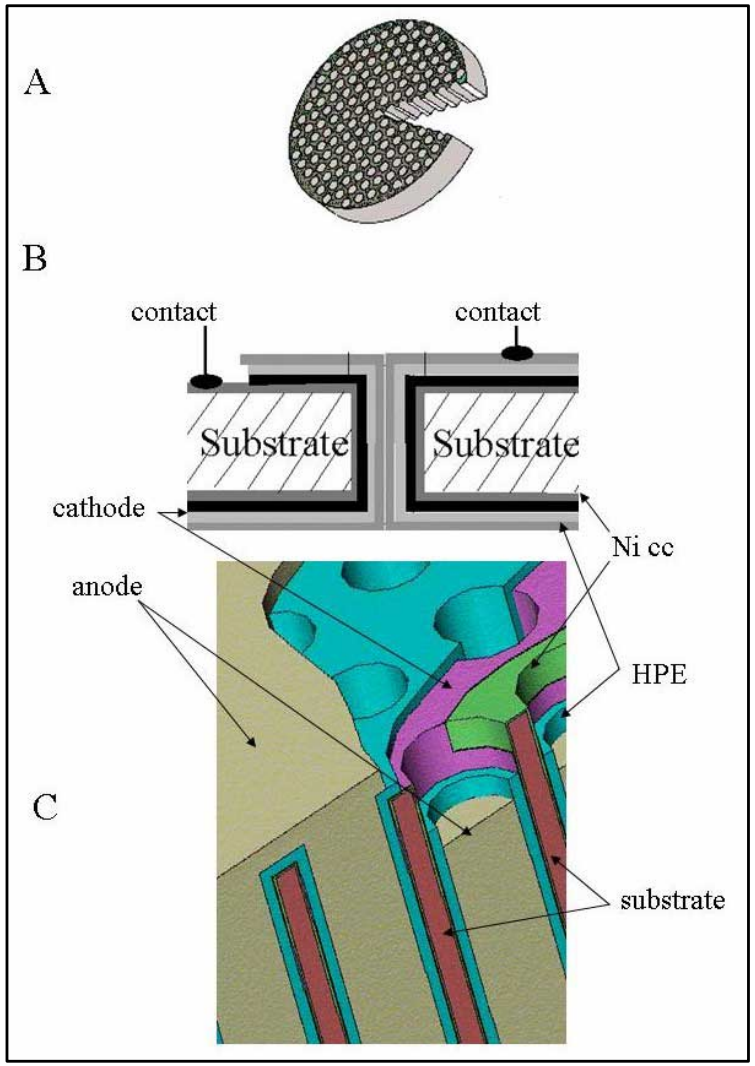
  50 nanometers and depth of

  100 micrometers has, depending on the technology, the capacitance in the range of 20-100 fF (femto = 10^{-15} F)
- How many can we squeeze on 1cm^2 ???
- Easily 10^{12} - 10^{14} !!! So we are almost in the Farad range !!



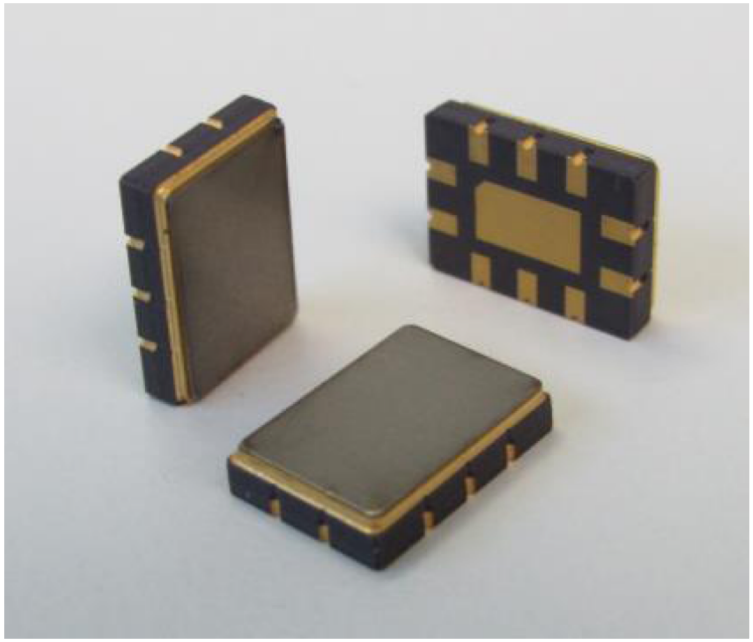
Nano-batteries

- The batteries developed by the team from Tel Aviv University (TAU) work in a different way than conventional batteries.
- Using a silicon or glass substrate, the team from TAU created a matrix of tiny holes each 50 microns in diameter and 500 micron deep. Each of these holes functions as an independent micro battery or microchannel with an output power of around 8-10 microW.
- The power of a $1cm^2$ 3D nanobattery is about 150-200mW.



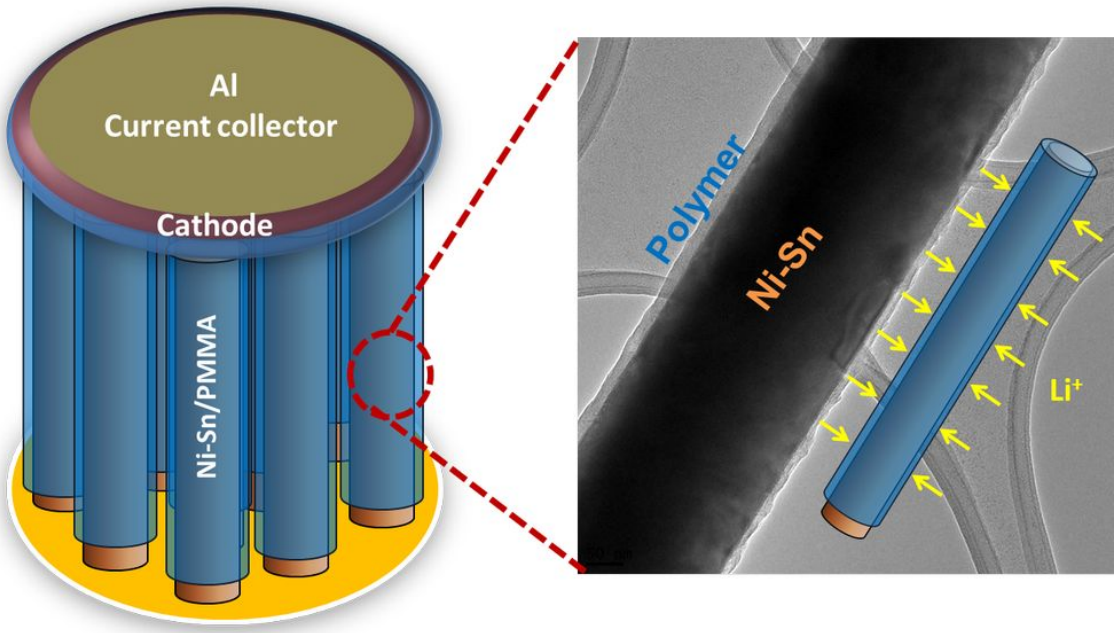
Latest developments

Industrial scale ultra-capacitor chip FastCAP EE



470mF operating at 2.1V

One-centimeter square microbatteries that hold more energy and that charge faster than planar batteries of the same electrode length. the PMMA coating will increase the number of times a battery can be charged by stabilizing conditions between the nanowires and liquid electrolyte, which tend to break down over time.



Nanowires with a PMMA polymer coating, seen in a transmission electron microscope image at right, solve a long-standing problem of forming ultra-thin electrolyte layers around nanostructured electrode materials. Source and images: Rice University

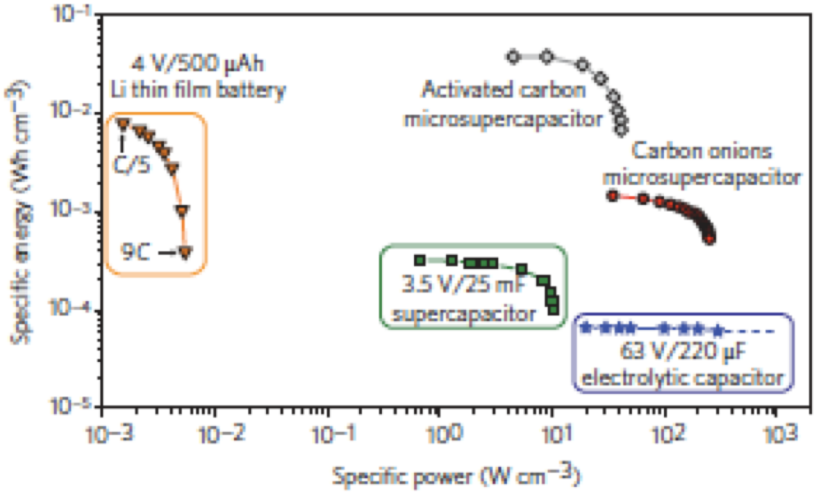
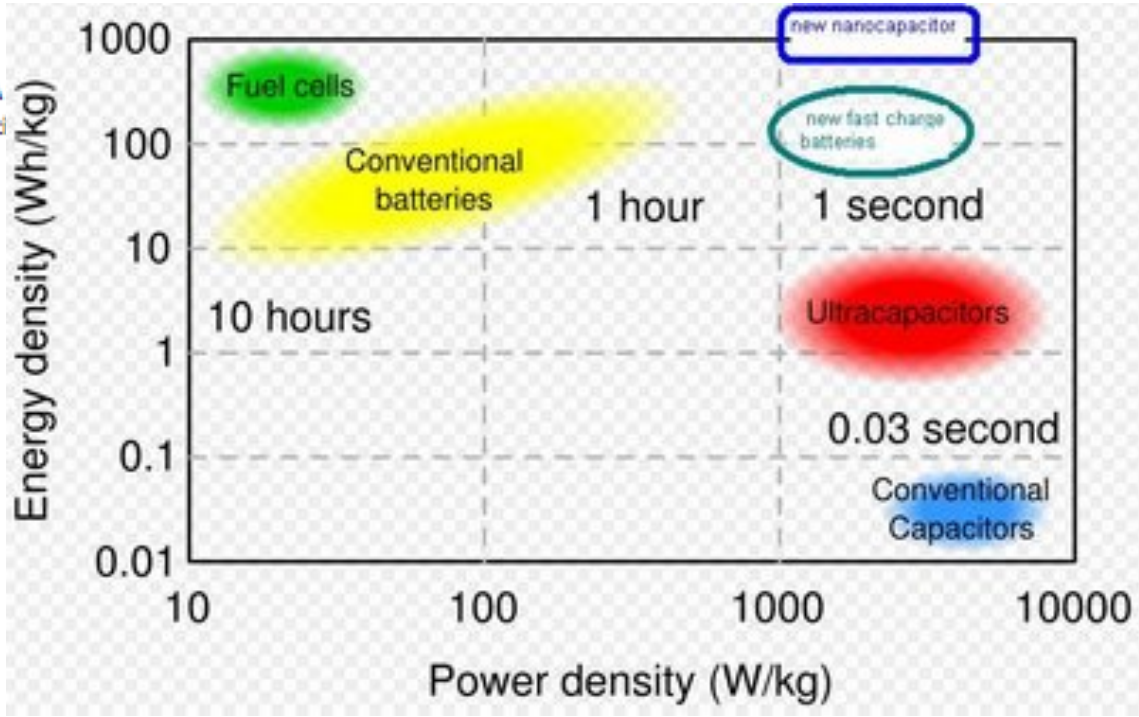


Figure 4 | Comparison, in a Ragone plot, of the specific energy and power density (per cm³ of stack) of typical electrolytic capacitors, supercapacitors and batteries with the microdevices. All the devices (macro and micro) were tested under the same dynamic conditions. A high energy density was obtained with the AC-based microsupercapaci whereas ultrahigh power density was obtained with the OLC-based microsupercapacitor.



Source: MIT Energystore

Main energy sources available for harvesting

- Mechanical energy: from sources such a vibration, mechanical stress and strain – piezoelectric, electrostatic or electromagnetic (CEA/Leti raindrops falling onto piezoelectric structure, HEAD converters for tennis racket or ski)
- Light energy: captured from sunlight or room light via solar panels, photo sensors or photo diodes
- Thermal energy: waste energy from engines, furnaces, heaters and friction sources (Seebeck effect)
- Electromagnetic energy: from inductors, coils and transformers
- Human body: a combination of mechanical and thermal energy naturally generated from bio-organisms or through actions such as walking (human body is emitting ca. 200W into environment!)
- Other energy: from chemical and biological sources

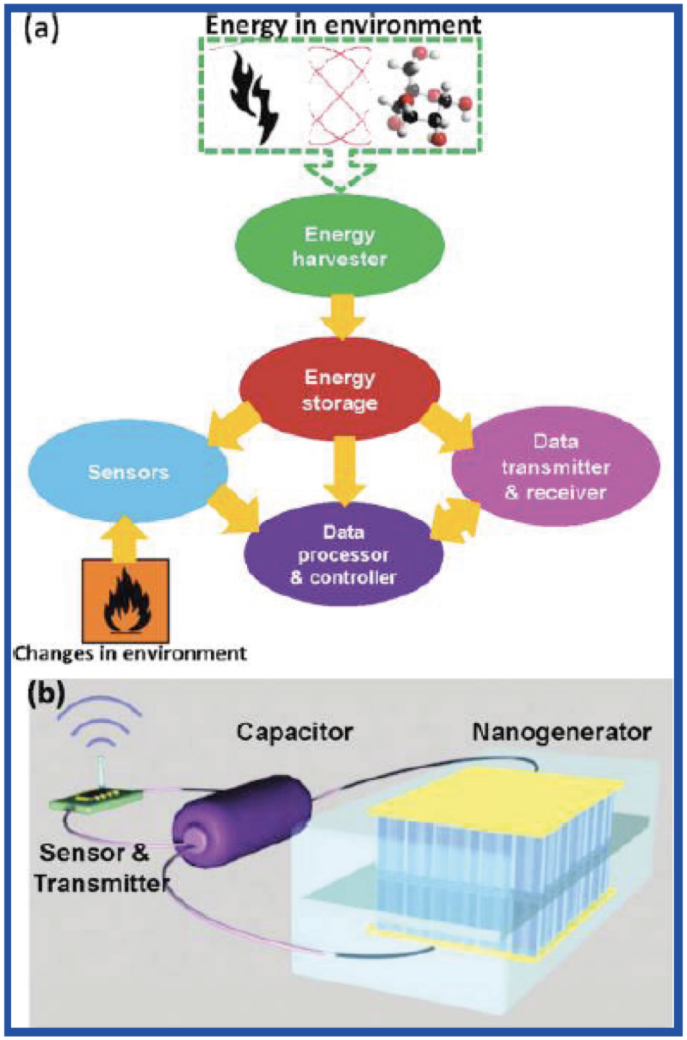


Figure 1. Schematic diagram of the integrated self-powered system. (a) An integrated system can be divided into five modules: energy harvester, energy storage, sensors, data processor and controller, and data transmitter and receiver. (b) The prototype of an integrated self-powered system by using a nanogenerator as the energy harvester.

Self-Powered System with Wireless Data Transmission

Youfan Hu,[+] Yan Zhang,[+] Chen Xu,[+] Long Lin, Robert L. Snyder, and Zhong Lin Wang*

School of Material Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332-0245, United States

Nano Lett. 2011, 11, 2572–2577

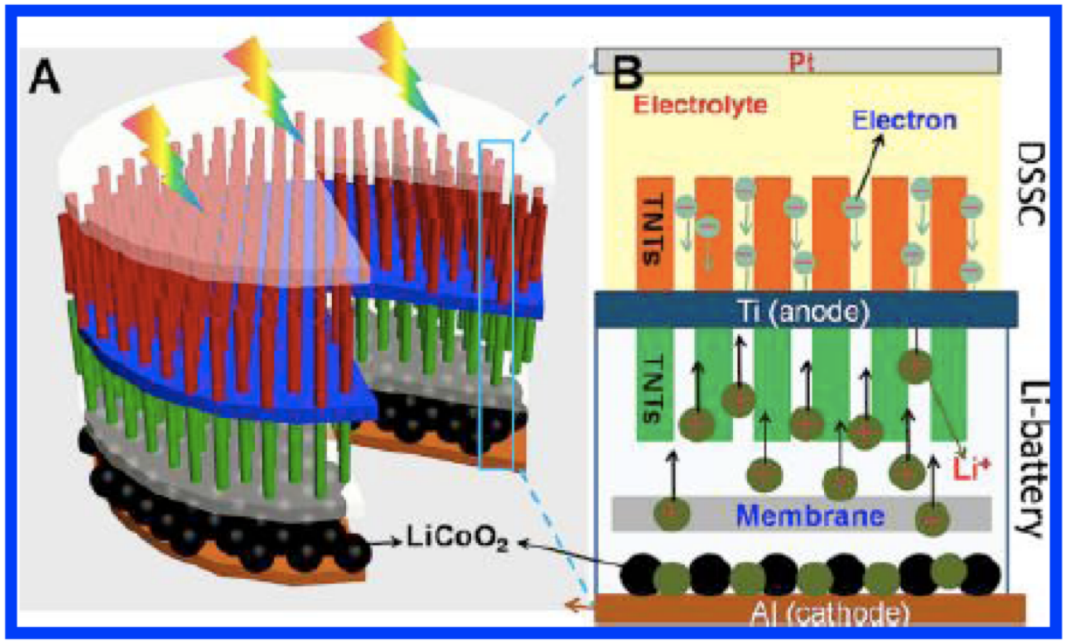


Figure 1. Design and principle of an integrated power pack system based on double-sided TiO_2 nanotube arrays. (A) TiO_2 nanotube arrays grown on the Ti foil substrate by anodization in fluoric ethylene glycol solution. The top segment of the Ti foil is tandem DSSCs which are utilized to harvest sunlight from environment, and the bottom segment is a typical lithium ion battery which is used to store energy converted from DSSCs. (B) Detailed structure and working principle of the integrated power pack system.

NANO LETTERS
Letter
pubs.acs.org/NanoLett

An Integrated Power Pack of Dye-Sensitized Solar Cell and Li Battery Based on Double-Sided TiO_2 Nanotube Arrays

Wenxi Guo,[†,‡,⊥] Xinyu Xue,[†,§,⊥] Sihong Wang,[†] Changjian Lin,[‡] and Zhong Lin Wang*[,†,∥]

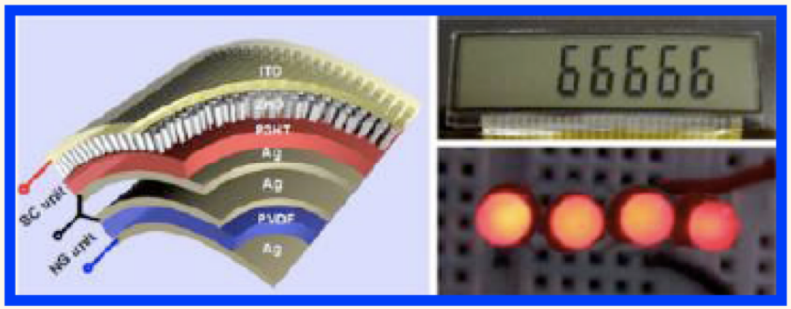
April 2012

Flexible Hybrid Energy Cell for Simultaneously Harvesting Thermal, Mechanical, and Solar Energies

Ya Yang,[†] Hulin Zhang,[†] Guang Zhu,[†] Sangmin Lee,[†] Zong-Hong Lin,[†] and Zhong Lin Wang[†,‡,*]

[†]School of Materials Science and Engineering, Georgia Institute of Technology, Atlanta, Georgia 30332-0245, United States and
[‡]Beijing Institute of Nanoenergy and Nanosystems, Chinese Academy of Sciences, Beijing, China

ABSTRACT We report the first flexible hybrid energy cell that is capable of simultaneously or individually harvesting thermal, mechanical, and solar energies to power some electronic devices. For having both the pyroelectric and piezoelectric properties, a polarized poly(vinylidene fluoride) (PVDF) film-based nanogenerator (NG) was used to harvest thermal and mechanical energies. Using aligned ZnO nanowire arrays grown on the flexible polyester (PET) substrate, a ZnO—poly(3-hexylthiophene) (P3HT) heterojunction solar cell was designed for harvesting solar energy. By integrating the NGs and the solar cells, a hybrid energy cell was fabricated to simultaneously harvest three different types of energies. With the use of a Li-ion battery as the energy storage, the harvested energy can drive four red light-emitting diodes (LEDs).



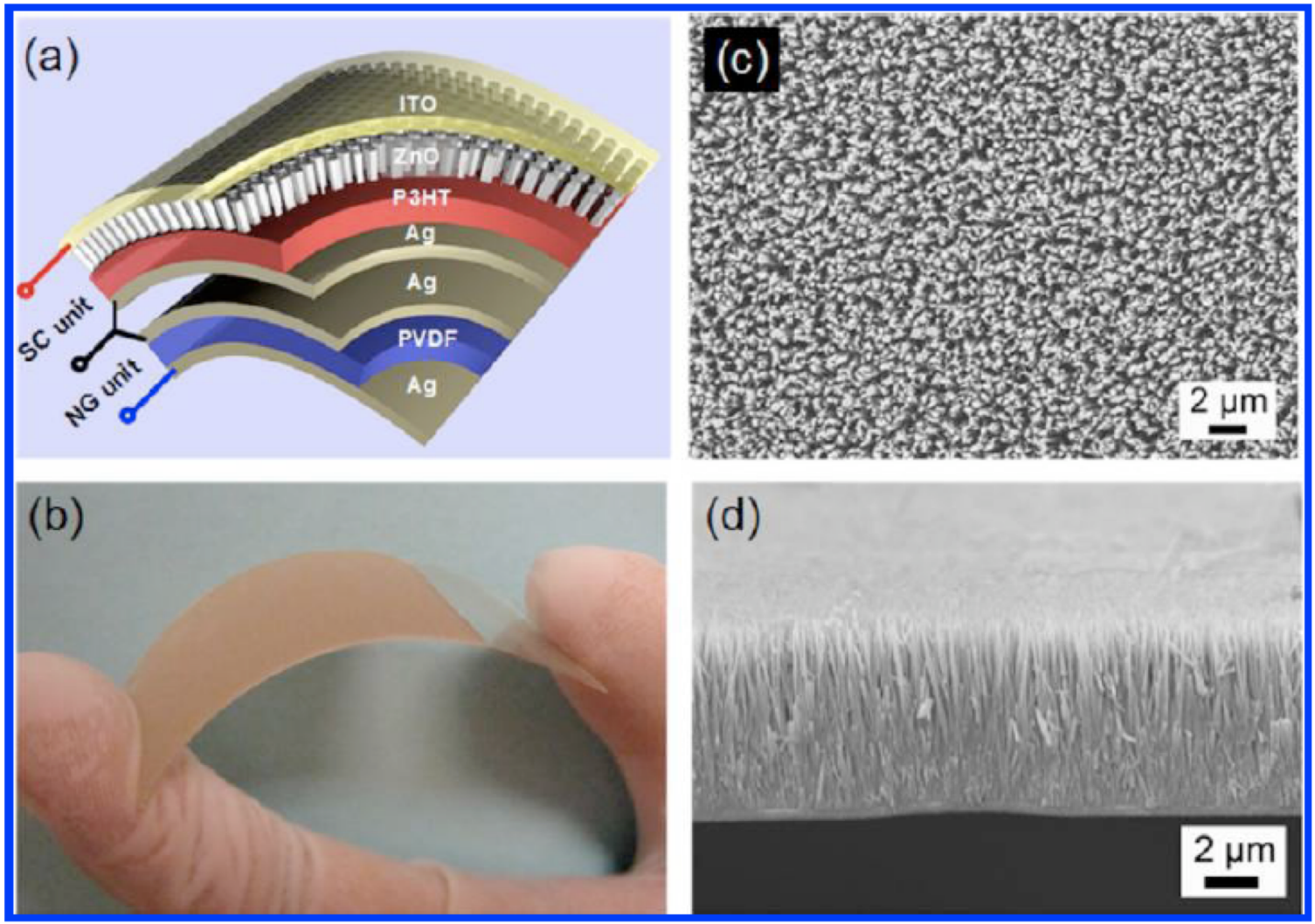


Figure 1. (a) Schematic diagram of the fabricated hybrid energy cell. (b) Photograph of the bent ZnO nanowire array grown on an ITO/PET substrate. (c) SEM image of the ZnO nanowire array. (d) Cross-section SEM image of the ZnO nanowire array.

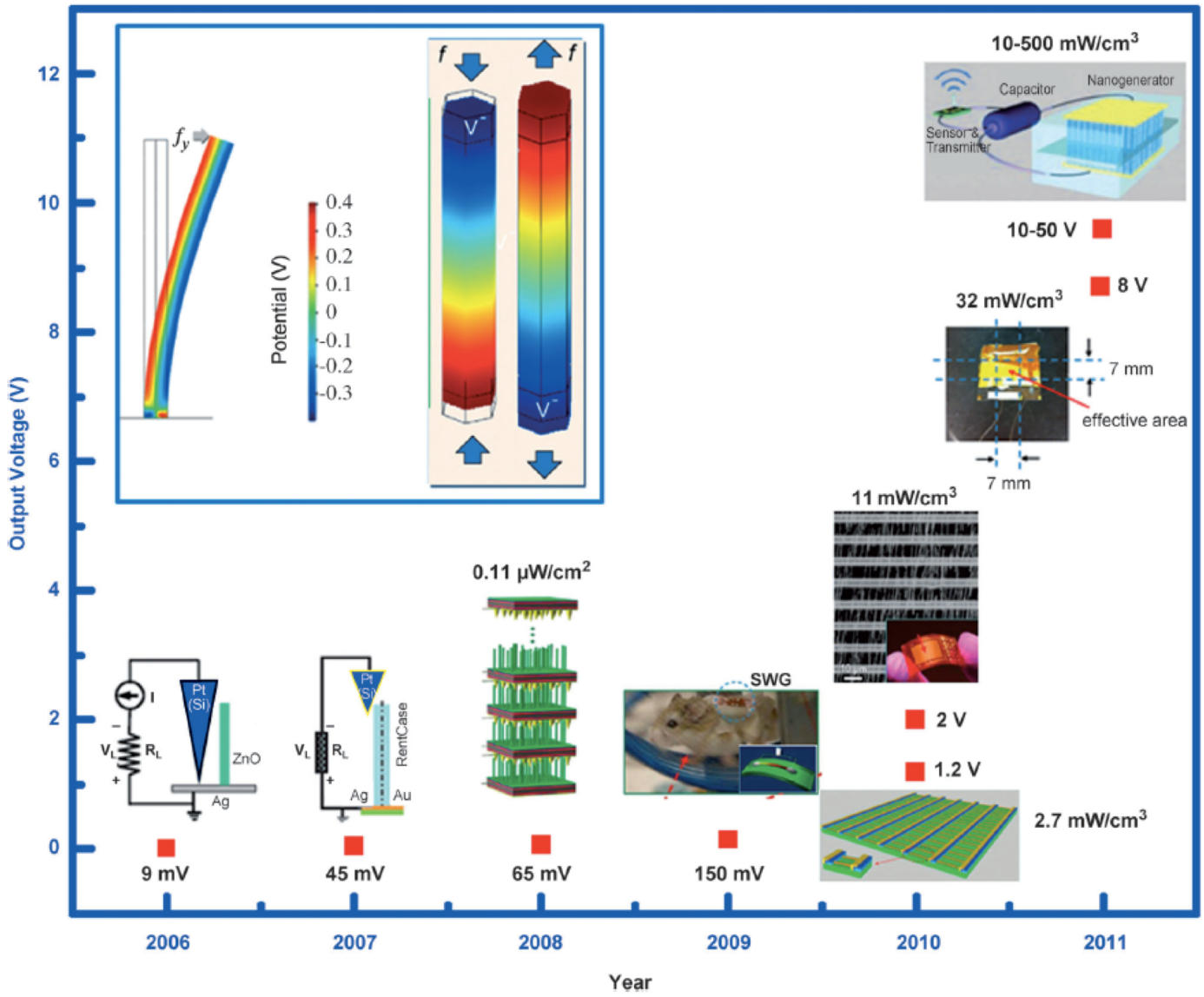
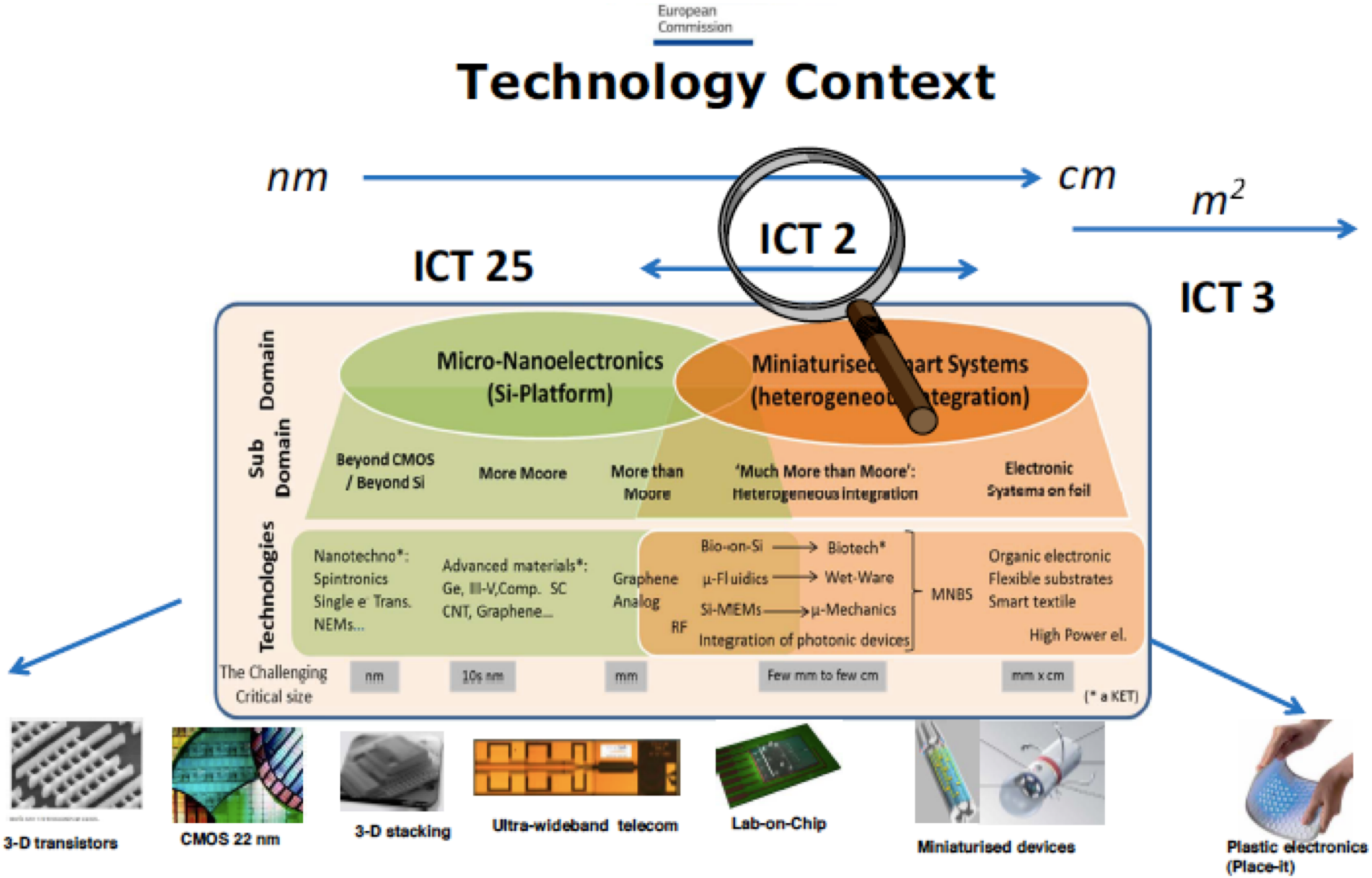


Figure 6. Improvement in the output voltage of nanogenerators based on ZnO nanowires in various configurations. The corresponding output power density is also indicated. The inset shows the simulated piezoelectric-potential distribution in the nanowires of the nanogenerator upon transverse and axial straining (from Ref. [104]). SWG = single wire generator.

Wang and Wu
Angewandte Chemie 2012

Horizon 2020 outlook



CONCLUSIONS

- Merging technologies is a major research problem
- Effort and collaboration of specialists from various domains (electronics, material science, chemistry, physics etc.) is needed
- We need to develop new conceptual design tools that support designers' ways of thinking and working and enhance creativity – no tools for heterogeneous microcircuits so far !
- We need new simulation/ optimization tools - no tools for heterogeneous microcircuits so far !