

Invited Paper

DC operating points of transistor circuits

Ljiljana Trajković^{1 a)}

¹ *Simon Fraser University
Vancouver, British Columbia, Canada*

^{a)} *ljilja@sfu.ca*

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Abstract: Finding a circuit's dc operating points is an essential step in its design and involves solving systems of nonlinear algebraic equations. Of particular research and practical interests are dc analysis and simulation of electronic circuits consisting of bipolar junction and field-effect transistors (BJTs and FETs), which are building blocks of modern electronic circuits. In this paper, we survey main theoretical results related to dc operating points of transistor circuits and discuss numerical methods for their calculation.

Key Words: nonlinear circuits, transistor circuits, dc operating points, circuit simulation, continuation methods, homotopy methods

1. Introduction

A comprehensive theory of dc operating points of transistor circuits has been established over the past three decades [2, 7, 26, 32, 53, 64, 65]. These results provided understanding of the system's qualitative behavior where nonlinearities played essential role in ensuring the circuit's functionality. While circuits such as amplifiers and logic gates have been designed to possess a unique dc operating point, bistable circuits such as flip-flops, static shift registers, static random access memory (RAM) cells, latch circuits, oscillators, and Schmitt triggers need to have multiple isolated dc operating points. Researchers and designers were interested in finding if a given circuit possesses unique or multiple operating points and in establishing the number or upper bound of operating points a circuits may possess. Once these operating points were identified, it was also of interest to establish their stability. Further to qualitative analysis, designers were also interested in finding all dc operating points of a given circuit using circuit simulators.

DC behavior of electronic circuits is described by systems of nonlinear algebraic equations. Their solutions are called the circuit's dc operating points. Bistable circuits that possess two stable isolated equilibrium points are used in a variety of electronic designs. Their operation is intimately related to the circuit's ability to possess multiple dc operating points.

Advances in computer aided design (CAD) tools for circuit simulation have enabled designers to simulate large circuits. The SPICE circuit simulator [35, 59] has become an industry standard and many SPICE-like tools are in use today. Computational difficulties in computing the dc operating points of transistor circuits are exacerbated by the exponential nature of the diode-type nonlinearities that model semiconductor devices. Since traditional methods for solving nonlinear equations describing transistor circuits often exhibited convergence difficulties, application of more sophisticated mathematical techniques and tools such as parameter embedding methods, continuation, and homotopy methods were successfully implemented in a variety of circuit simulators. These methods are a

viable alternative to the existing options in circuit simulators and were used both to resolve convergence difficulties and to find multiple dc operating points. Hence, they proved successful in computing dc operating points of circuits that could not be simulated using more conventional techniques.

2. Transistor DC models and circuit DC equations

A simple model that describes dc (large-signal) behavior [14] of a bipolar junction transistor (BJT) is the Ebers-Moll model [11]. The model has been used in a number of analytical studies. Field-effect transistors (FETs) do not possess such a simple, mathematically tractable, large-signal model. Nonetheless, many of the theoretical results related to BJT circuits have been extended to include circuits with FETs [67].

Two important albeit simple attributes of BJT and FET transistors are their “passivity” [17] and “no-gain” [66] properties. These properties have proved instrumental in establishing theoretical results dealing with dc operating points as well as in designing algorithms for solving equations describing transistor circuits [53]. When considering their dc behavior, transistors are passive devices, which implies that at any dc operating point the net power delivered to the device is nonnegative. They are also no-gain and, hence, are incapable of producing voltage or current gains. Subsequently, passivity is a consequence of the no-gain property.

By using the Ebers-Moll transistor model, the large-signal dc behavior of an arbitrary circuit containing $n/2$ bipolar transistors may be described with an equation of the form

$$QTF(v) + Pv + c = 0. \quad (1)$$

The real $n \times n$ matrices P and Q and the real n -vector c , where

$$Pv + Qi + c = 0, \quad (2)$$

describe the linear multiport that connects the nonlinear transistors. The real matrix T , a block diagonal matrix with 2×2 diagonal blocks of the form

$$T_i = \begin{bmatrix} 1 & -\alpha_{i+1} \\ -\alpha_i & 1 \end{bmatrix}, \quad (3)$$

and

$$F(v) \equiv (f_1(v_1), \dots, f_n(v_n))^T \quad (4)$$

capture the presence of the nonlinear elements. The controlled-source current-gains α_k , $k = 1, 2$, lie within the open interval $(0, 1)$. The functions $f_k: R^1 \rightarrow R^1$ are continuous and strictly monotone increasing. Typically,

$$i = f_k(v) \equiv m_k(e^{n_k v} - 1), \quad (5)$$

where the real numbers m_k , n_k are positive when modeling a *pn*p transistor and negative for an *np*n transistor. They satisfy the *reciprocity* condition:

$$m_i \alpha_i = m_{i+1} \alpha_{i+1}, \text{ for } i \text{ odd}. \quad (6)$$

The nonlinear elements are described via the equation

$$i = TF(v). \quad (7)$$

Hence,

$$AF(v) + Bv + c = 0, \quad (8)$$

where $A = QT$ and $B = P$. This equation represents a general description of an arbitrary nonlinear transistor circuit. Its solutions are the circuit’s dc operating points.

The determinant $\det(AD + B)$ is the Jacobian of the mapping $AF(v) + Bv + c$ evaluated at the point v , where

$$D = \text{diag}(d_1, d_2, \dots, d_n), \quad (9)$$

with

$$d_i = \frac{df_i(v_i)}{dv_i} > 0, \text{ for } i = 1, 2, \dots, n. \quad (10)$$

The sign of this Jacobian varies with v and it is an important indicator of a circuit's ability to possess multiple dc operating points. If a transistor circuit possesses multiple operating points, then there exists some v at which $\det(AD + B) = 0$ [64, 65]. While the presence of feedback structure is essential if a circuit is to possess multiple operating points, circuit parameters also affect the circuit's dc behavior. The number of dc operating points a circuit may possess depends on current gains of bipolar transistors, circuit resistances, and values of independent voltage and current sources [48, 49, 53]. They affect voltages and currents established across transistor pn junctions and, hence, biasing of transistors that is essential when designing electronic circuits.

Stability of dc operating points has been addressed in observation that there are dc operating points of transistor circuits that are unstable in the sense that, if the circuit is biased at such an operating point and if the circuit is augmented with *any* configuration of positive-valued shunt capacitors and/or series inductors, the equilibrium point of the resulting dynamic circuit will always be unstable [19, 21–23]. Almost half of transistor dc operating points are unstable [20].

2.1 Number of DC operating points

It is well known that nonlinear circuits consisting of an arbitrary number of linear resistors and diodes possess at most one dc operating point. Several fundamental results relate the topology of a transistor circuit to the number of possible dc operating points. Many transistor circuits are known to possess a unique dc operating point due to their topology alone [36, 47]. Any circuit containing only a single transistor and all multi-transistor circuits whose topology consists of a generalized common-base structure belong to this class. The so-called “separable circuits” possess unique operating points if each of their constituent one-ports has a unique operating point when its port is either open-circuited or short-circuited. In general, any circuit that does not possess a *feedback structure* possesses a unique dc operating [37]. A feedback structure is identified by setting all independent source values to zero, by open-circuiting and/or short-circuiting resistors, and by replacing all but two of the transistors by a pair of open and/or short circuits. The extension of the topological criteria to more general three-terminal devices (including FETs) [67], circuits employing Ebers-Moll-modeled transistors having variable current-gains [18], and metal-oxide-semiconductor field-effect transistor (MOSFET) circuits [15] have been also established.

A circuit that contains more than two transistors may possess numerous operating points. Several methods have been proposed to obtain upper bounds on the number of dc operating points of transistor circuits. For example, it has been proven [29] that a transistor circuit consisting of an arbitrary number of linear positive resistors, q exponential diodes, and p Ebers-Moll-modeled bipolar transistors has at most

$$(d + 1)^d 2^{d(d-1)/2} \quad (11)$$

isolated dc operating points, where $d = q + 2p$. If, instead of bipolar transistors, the circuit employs Shichman-Hodges modeled FETs, it may have at most

$$2^p 3^{2p} (4p + q + 1)^q 2^{q(q-1)/2} \quad (12)$$

isolated dc operating points. Bounds were also obtained for the number of dc operating points in circuits using other transistor models. However, finding tighter bounds is still an open research problem [13, 31, 38, 39].

3. Calculating DC operating points

DC operating points are usually calculated by using the Newton-Raphson method or its variants such as damped Newton methods [3, 41]. These methods are robust and have quadratic convergence when a starting point sufficiently close to a solution is supplied. The Newton-Raphson algorithms sometimes fail because it is difficult to provide a starting point sufficiently close to an often unknown solution.

Experienced designers of analog circuits employ various ad hoc techniques to solve convergence difficulties when simulating electronic circuits. They are known as *source-stepping*, *temperature-sweeping*, and *G_{min}-stepping* techniques. The *source-stepping* relies on linearly increasing source voltages and then calculating a series of operating points until the response to the desired voltage is found. In *temperature-sweeping*, the temperature is increased over a range of values and a series of dc operating points is calculated until the dc operating point is found at the desired temperature. *G_{min}-stepping* involves placing small conductances between every circuit node and the ground, finding the operating point of the circuit, and then using it to set initial node voltages for the next step when the auxiliary conductances are decreased until a default minimum value is reached. In the latter case, the initial value of the conductances is chosen large enough to enhance the convergence since they contribute to the diagonal elements of the circuit's Jacobian matrix and may force it to become row or column sum dominant. All these techniques rely on the Newton-Raphson method or its variants for solving nonlinear circuit equations. They implicitly exploit the idea of embedding or continuation where a parameter is varied over a range of values until the desired operating point is found. The approach often works because each subsequent dc operating point is found by using the previous result as the starting point.

3.1 Parameter embedding and continuation methods

Parameter embedding methods, also known as continuation methods [8, 9] are robust and accurate numerical techniques employed to solve nonlinear algebraic equations [1, 62, 63]. They are used to find multiple solutions of equations that possess multiple solutions [46]. Probability-one homotopy algorithms are a class of embedding algorithms that promise global convergence [5, 61]. Various homotopy algorithms have been introduced for finding multiple solutions of nonlinear circuit equations [4, 40] and for finding dc operating points of transistor circuits [16, 24, 28, 43, 56, 58, 68]. Homotopy algorithms were implemented in a number of developed stand-alone circuit simulators [69, 70], simulators developed based on SPICE [55, 58], and proprietary industrial tools designed for simulation of analog circuits such as ADVICE at AT&T [12, 34, 51, 52] and TITAN at Siemens [33]. They have been successful in finding solutions to highly nonlinear circuits that could not be simulated using conventional numerical methods. The main drawback of homotopy methods is their implementation complexity [50, 54] and computational intensity. However, they offer a very attractive alternative for solving difficult nonlinear problems where initial solutions are difficult to estimate or where multiple solutions are desired.

3.2 Homotopy methods: Background

Homotopy methods are used to solve systems of nonlinear algebraic equations and may be applied to a large variety of problems. We are most interested in solving the zero finding problem

$$\mathcal{F}(\mathbf{x}) = \mathbf{0}, \quad (13)$$

where $\mathbf{x} \in \mathcal{R}^n$, $\mathcal{F} : \mathcal{R}^n \rightarrow \mathcal{R}^n$. Note that the fixed point problem $\mathcal{F}(\mathbf{x}) = \mathbf{x}$ may be easily reformulated as a zero finding problem

$$\mathcal{F}(\mathbf{x}) - \mathbf{x} = \mathbf{0}. \quad (14)$$

A homotopy function $\mathcal{H}(\mathbf{x}, \lambda)$ is created by embedding a parameter λ into $\mathcal{F}(\mathbf{x})$ to obtain an equation of higher dimension

$$\mathcal{H}(\mathbf{x}, \lambda) = \mathbf{0}, \quad (15)$$

where $\lambda \in \mathcal{R}$, $\mathcal{H} : \mathcal{R}^n \times \mathcal{R} \rightarrow \mathcal{R}^n$. For $\lambda = 0$,

$$\mathcal{H}(\mathbf{x}, 0) = \mathbf{0} \quad (16)$$

is an easy equation to solve. For $\lambda = 1$,

$$\mathcal{H}(\mathbf{x}, 1) = \mathbf{0} \quad (17)$$

is the original problem (13). The parameter λ is called the continuation or homotopy parameter.

An example of a homotopy function is

$$\mathcal{H}(\mathbf{x}, \lambda) = (1 - \lambda)\mathcal{G}(\mathbf{x}) + \lambda\mathcal{F}(\mathbf{x}). \quad (18)$$

Hence,

$$\mathcal{H}(\mathbf{x}, 0) := \mathcal{G}(\mathbf{x}) = \mathbf{0} \quad (19)$$

has an easy solution while

$$\mathcal{H}(\mathbf{x}, 1) := \mathcal{F}(\mathbf{x}) = \mathbf{0} \quad (20)$$

is the original problem. By following solutions of

$$\mathcal{H}(\mathbf{x}, \lambda) = \mathbf{0} \quad (21)$$

as λ varies from 0 to 1, the solution to $\mathcal{F}(\mathbf{x}) = \mathbf{0}$ is reached.

The solutions (21) trace a path known as the zero curve. Various numerical situations may occur depending on the behavior of this curve. One problem occurs if the curve folds back. At the turning point, the values of λ decrease as the path progresses. Increasing λ from 0 to 1 results in “losing” the curve. The difficulty is resolved by making λ a function of a new parameter, the arc length s . This method is known as the *arc length* continuation [61, 63].

3.3 Homotopy functions

Various homotopies may be constructed from the circuit’s nodal or modified nodal formulations.

The *fixed-point* homotopy is based on the equation

$$\mathcal{H}(\mathbf{x}, \lambda) = (1 - \lambda)\mathbf{G}(\mathbf{x} - \mathbf{a}) + \lambda\mathcal{F}(\mathbf{x}), \quad (22)$$

where, in addition to the parameter λ , a random vector \mathbf{a} and a new parameter (a diagonal matrix) $\mathbf{G} \in R^n \times R^n$ are embedded. With probability one, a random choice of \mathbf{a} gives a bifurcation-free homotopy path [63].

The *variable-stimulus* homotopy is based on the equation

$$\mathcal{H}(\mathbf{x}, \lambda) = (1 - \lambda)\mathbf{G}(\mathbf{x} - \mathbf{a}) + \mathcal{F}(\mathbf{x}, \lambda), \quad (23)$$

where the node voltages of the nonlinear elements are multiplied by λ . The starting point of the homotopy is the solution to a linear circuit. The homotopy is a generalization of the *source-stepping* approach.

The fastest converging homotopy for bipolar circuits is the *variable-gain* homotopy:

$$\mathcal{H}(\mathbf{x}, \lambda) = (1 - \lambda)\mathbf{G}(\mathbf{x} - \mathbf{a}) + \mathcal{F}(\mathbf{x}, \lambda\alpha), \quad (24)$$

where α is a vector consisting of transistor forward and reverse current gains. The starting point $\lambda = 0$ corresponds to the dc operating point of a circuit consisting of resistors and diodes only and, hence, possesses a unique dc operating point. A combination of variable-stimulus and variable-gain homotopies called the *hybrid* homotopy may also be used as a solver. The variable-stimulus homotopy is first used to solve the initial nonlinear circuit and the variable-gain homotopy is then applied to find the dc operating points of the original circuit.

3.4 Numerical solver

There are several approaches for implementing homotopy methods [63]. One set of algorithms is based on the ordinary differential equations. The solution of the equation

$$\mathcal{H}(\mathbf{x}(s), \lambda(s)) = \mathbf{0}, \quad (25)$$

where s is the *arc length* parameter, is a trajectory

$$\mathbf{y}(s) = \begin{pmatrix} \lambda(s) \\ \mathbf{x}(s) \end{pmatrix}. \quad (26)$$

This trajectory is found by solving the differential equation

$$\frac{d}{ds} \mathcal{H}(\mathbf{x}(s), \lambda(s)) = \mathbf{0}, \quad (27)$$

with conditions

$$\lambda(0) = 0, \quad \mathbf{x}(0) = \mathbf{a}, \quad \text{and} \quad \left\| \frac{d\lambda}{ds}, \frac{d\mathbf{x}}{ds} \right\|_2 = 1. \quad (28)$$

Differential equation (27) may be written as

$$\mathbf{P}(\mathbf{y})\dot{\mathbf{y}} := \begin{bmatrix} \frac{\partial \mathcal{H}}{\partial \lambda} & \frac{\partial \mathcal{H}}{\partial \mathbf{x}} \end{bmatrix} \begin{bmatrix} \frac{d\lambda}{ds} & \frac{d\mathbf{x}}{ds} \end{bmatrix}. \quad (29)$$

We wish to solve

$$\mathbf{P}(\mathbf{y})\dot{\mathbf{y}} = \mathbf{0} \quad (30)$$

for $\dot{\mathbf{y}}$. The solution is unique if the extended Jacobian matrix (27) is of full rank. Conditions (28) define the starting value of λ , the starting point for \mathbf{x} , and ensure that the sign and the magnitude of $\dot{\mathbf{y}}$ are fixed in the implementation. The solution $\dot{\mathbf{y}}$ is found by solving linear differential equation (29) using standard linear solvers via the QR factorization algorithm [30].

Once the derivatives are determined, the variable-step predictor-corrector method is used to find $\mathbf{y}(s)$ from its derivative that were found in the previous step. The method proved superior to the Runge-Kutta methods.

Finally, the “end game” is used to determine the step size so that the solution to $\mathbf{y}(s)$ for $\lambda = 1$ may be reached. A cubic spline interpolation of $\lambda(s)$ and a solution to $\lambda(s) = 1$ (the smallest root that is greater than the current value of s) are used to predict the next step size. Once λ is within the preselected tolerance, the value of \mathbf{x} is assumed to be the sought solution.

3.5 Implementations in analog circuit simulators

Homotopy methods have been used [34, 54] to simulate various circuits that could not be simulated using conventional methods available in circuit simulators. In several implementations, the software package HOMPACT [61] was interfaced to SPICE-like simulators such as the ADVICE (AT&T) [34], TITAN (Siemens) [54], and SPICE 3F5 (UC Berkeley) [55] simulator engines. When existing methods for finding dc operating points fail, the dc operating points of a transistor circuit are obtained using HOMPACT. DC operating points of various circuits that could not be simulated using conventional methods available in simulators were successfully found using homotopies. These circuits are often highly sensitive to the choice of parameters and the biasing voltages. Even simple software implementations of homotopy algorithms using the widely available MATLAB software package [25] proved powerful enough to solve benchmark nonlinear circuits that possess multiple operating points.

4. Examples

Implementations of homotopy algorithms need not necessarily rely on large numerical solvers or proprietary circuit simulation tools. Furthermore, simple homotopy functions proved adequate for solving some difficult benchmark circuits. MATLAB implementation was successfully used [10] to find three dc operating points of the Schmitt Trigger circuit and nine dc operating points of a benchmark four-transistor circuit. The accuracy of the results was verified by comparison with the PSPICE [42] solutions and results of other homotopy implementations.

4.1 Schmitt trigger circuit

We illustrate the application of homotopy methods by solving nonlinear equation that describe the Schmitt trigger circuit shown in Fig. 1. The circuit possesses three dc operating points. All three solutions to the circuit’s modified nodal equations were successfully found by using the fixed-point homotopy (22).

The set of nonlinear equations based on the modified nodal formulation [27] describes the circuit:

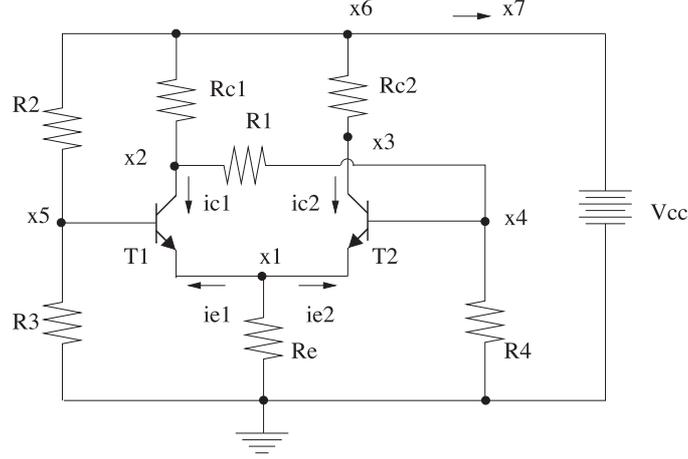


Fig. 1. Schmitt trigger circuit whose equations were solved by using homotopy method. Circuits parameters are: $V_{cc} = 10$ V, $R_1 = 10$ k Ω , $R_2 = 5$ k Ω , $R_3 = 1.25$ k Ω , $R_4 = 1$ M Ω , $R_{c1} = 1.5$ k Ω , $R_{c2} = 1$ k Ω , and $R_e = 100$ Ω . The two bipolar transistors are identical with parameters: $m_e\alpha_f = m_c\alpha_r = -1.0 \times 10^{-16}$ A, $\alpha_f = 0.99$, $\alpha_r = 0.5$, and $n = -38.78$ 1/V.

$$\begin{aligned}
 \frac{x_1}{R_e} + i_{e1} + i_{e2} &= 0 \\
 \frac{x_2 - x_4}{R_1} + \frac{x_2 - x_6}{R_{c1}} + i_{c1} &= 0 \\
 \frac{x_3 - x_6}{R_{c2}} + i_{c2} &= 0 \\
 \frac{x_4 - x_2}{R_1} + \frac{x_4}{R_4} - i_{e2} - i_{c2} &= 0 \\
 \frac{x_5 - x_6}{R_2} + \frac{x_5}{R_3} - i_{c1} - i_{e1} &= 0 \\
 \frac{x_6 - x_2}{R_{c1}} + \frac{x_6 - x_3}{R_{c2}} + \frac{x_6 - x_5}{R_2} + x_7 &= 0 \\
 x_6 - V_{cc} &= 0.
 \end{aligned} \tag{31}$$

Bipolar-junction transistors are modeled using the Ebers-Moll transistor model [11]

$$\begin{pmatrix} i_e \\ i_c \end{pmatrix} = \begin{pmatrix} 1 & -\alpha_r \\ -\alpha_f & 1 \end{pmatrix} \begin{pmatrix} f_e(v_e) \\ f_c(v_c) \end{pmatrix}, \tag{32}$$

where

$$f_e(x) = m_e(e^{nx} - 1) \quad \text{and} \quad f_c(x) = m_c(e^{nx} - 1) \tag{33}$$

and the *reciprocity* condition holds:

$$m_e\alpha_f = m_c\alpha_r. \tag{34}$$

For transistor T_1

$$\begin{aligned}
 v_1 &= x_1 - x_5 \\
 v_2 &= x_2 - x_5
 \end{aligned} \tag{35}$$

while for transistor T_2

$$\begin{aligned}
 v_3 &= x_1 - x_4 \\
 v_4 &= x_3 - x_4.
 \end{aligned} \tag{36}$$

For the two *npn* transistors that were used in the example $m_e < 0$, $m_c < 0$, and $n < 0$.

By using the fixed-point homotopy (22) we have successfully found all three solutions to (31). The elements of the diagonal matrix \mathbf{G} were set to 10^{-3} and the starting vector \mathbf{a} was chosen by a random number generator. The solution paths for voltages x_1 through x_4 and the current x_7 as functions of the homotopy parameter λ are shown in Fig. 2. These paths were obtained by solving circuit's modified nodal equations with a simple homotopy embedding (22). The three solutions are found when the paths intersect the vertical line corresponding to the value $\lambda = 1$. The solutions for the circuit's node voltages and the current flowing through the independent voltage source are listed in Table I.

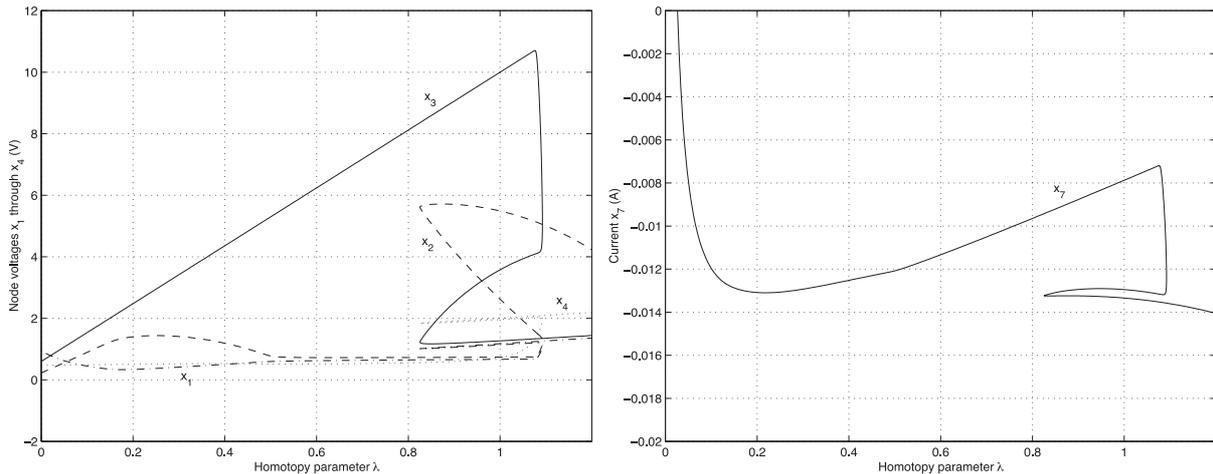


Fig. 2. Homotopy paths for the four node voltages x_1 through x_4 (left) and the current x_7 (right) of the Schmitt trigger circuit. The plots show solutions of the homotopy equations vs. the value of the the homotopy parameter λ .

Table I. Three solutions were found by solving the circuit's modified nodal equations using the fixed-point homotopy. Variables x_1 through x_6 are node voltages in (V) and variable x_7 is the current in (mA) flowing through the independent voltage source V_{cc} .

Three DC Operating Points of the Schmitt Trigger Circuit				
Variable	Sol. 1	Sol. 2	Sol. 3	
x_1	0.6682	1.1388	1.1763	
x_2	0.7398	2.6204	5.4897	
x_3	10.0000	3.5785	1.2689	
x_4	0.7325	1.9587	2.0055	
x_5	1.4905	1.9515	1.9734	
x_6	10.0000	10.0000	10.0000	
x_7	-7.9	-13.0	-13.3	

4.2 Four-transistor circuit

Nine dc operating points of the four-transistor benchmark circuit [6, 57] shown in Fig. 3 were found by using the MATLAB implementation of the homotopy algorithm. A simple homotopy function

$$\mathcal{H}(\mathbf{x}, \lambda) = (1 - \lambda)\mathbf{G}(\mathbf{x} - \mathbf{a}) + \lambda\mathcal{F}(\mathbf{x}) \quad (37)$$

was used, where \mathbf{G} is a diagonal scaling matrix and \mathbf{a} is a starting vector.

MATLAB was used to generate plots of the homotopy paths for the unknown node voltages and for the currents flowing through each independent voltage source. They are shown in Fig. 4 (left) and Fig. 5 (left). By zooming in on the path for an individual node voltage and current, it may be seen

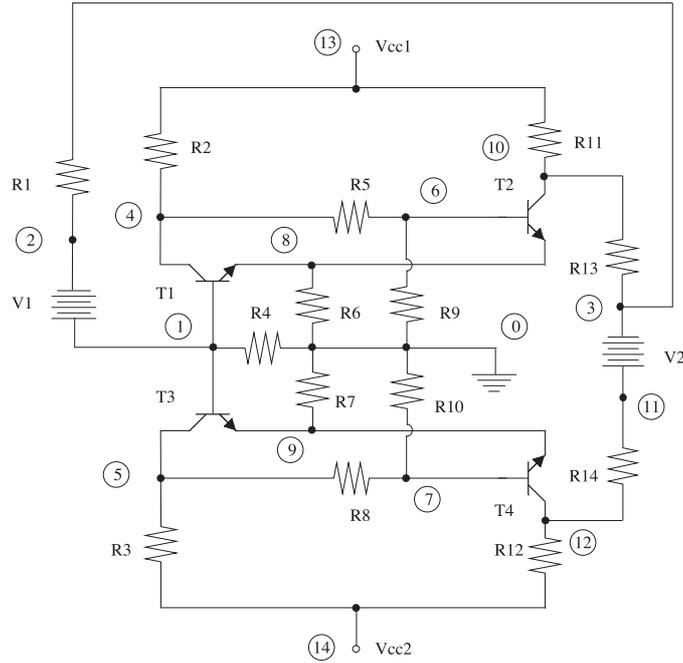


Fig. 3. Four-transistor benchmark circuit that possesses nine dc operating points. Circuit parameters: $R1 = 10\text{k}\Omega$, $R2 = R3 = 4\text{k}\Omega$, $R4 = 5\text{k}\Omega$, $R5 = R8 = 30\text{k}\Omega$, $R6 = R7 = 0.5\text{k}\Omega$, $R9 = R10 = 10.1\text{k}\Omega$, $R11 = R12 = 4\text{k}\Omega$, $R13 = R14 = 30\text{k}\Omega$, $V1 = 10\text{V}$, $V2 = 2\text{V}$, and $VCC = 12\text{V}$. The four bipolar transistors are identical with parameters: $m_e\alpha_f = m_c\alpha_r = -1.0 \times 10^{-9}$ A, $\alpha_f = 0.9901$, $\alpha_r = 0.5$, and $n = -38.7766$ 1/V.

that each path crosses the vertical line $\lambda = 1$ nine times. These paths are shown in Fig. 4 (right) and Fig. 5 (right).

The MATLAB results listed in Table II are comparable with solutions from other homotopy implementations [70]. Even though Newton-Raphson method solvers implemented in simulators such as SPICE 3 [45], SPICE 3F5 [44], and PSPICE [42] will calculate only one dc operating point, it is possible to provide PSPICE with an initial guess that is close to a desired solution by using the .NODESET option. In this manner, by using the MATLAB results as a starting point, all nine dc operating points listed in Table III were found.

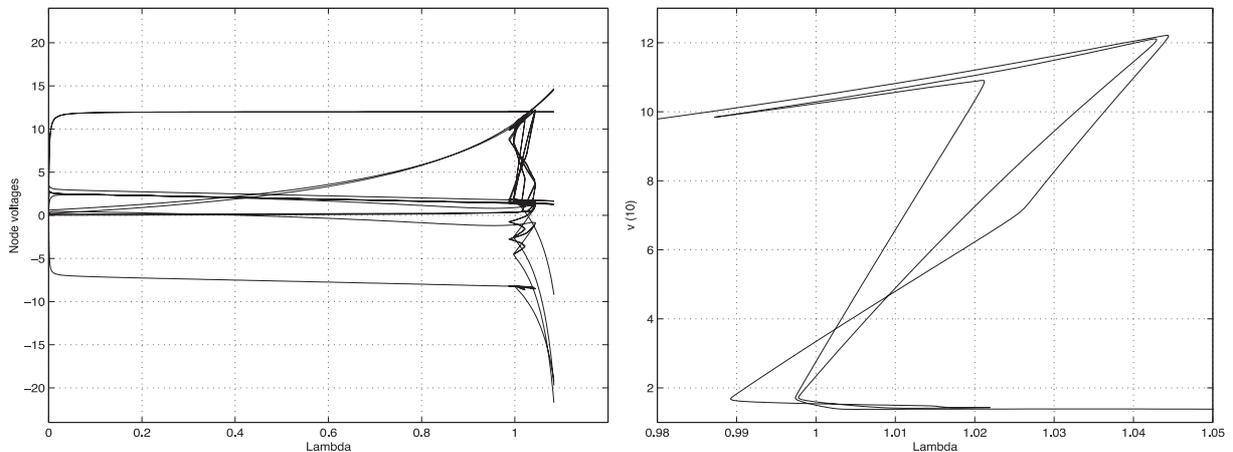


Fig. 4. Homotopy paths for the fourteen node voltages of the four-transistor benchmark circuit (left). Closer view of the homotopy path for the voltage at node 10 (right).

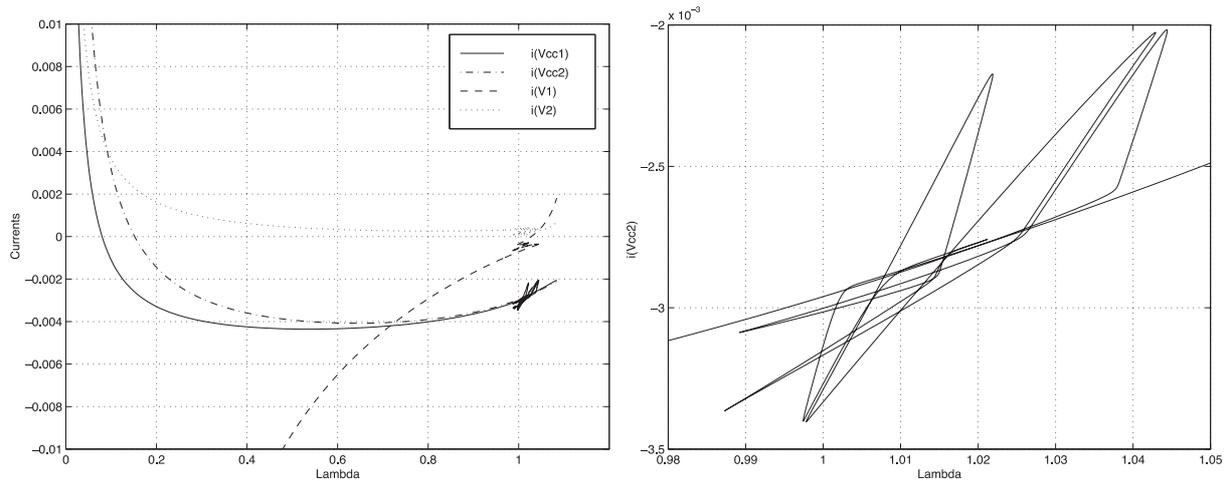


Fig. 5. Homotopy paths for the four currents flowing through the four independent voltage sources of the four-transistor benchmark circuit (left). Closer view of the homotopy path for the current flowing through the independent voltage source connected to node number 14 (right).

Table II. Nine solutions were found by solving the circuit’s modified nodal equations using the fixed-point homotopy. Values of node voltages are given in (V) while values of currents flowing through the independent voltage sources are given in (mA).

Nine DC Operating Points of the Four-Transistor Circuit									
Variable	Sol. 1	Sol. 2	Sol. 3	Sol. 4	Sol. 5	Sol. 6	Sol. 7	Sol. 8	Sol. 9
V(1)	1.7718	1.7823	1.7688	1.8195	1.8456	1.7823	1.7670	1.8108	1.7278
V(2)	-8.2282	-8.2177	-8.2312	-8.1805	-8.1544	-8.2177	-8.2330	-8.1892	-8.2722
V(3)	-1.1066	-2.5571	-2.9350	-4.4107	-4.3092	-2.5571	-2.9839	-4.4439	-4.7633
V(4)	1.4645	7.7505	9.6275	9.0400	8.0928	1.4715	1.4615	7.9047	9.7504
V(5)	1.4645	1.4715	1.4626	7.9514	8.0928	7.7505	9.8520	9.3418	9.9609
V(6)	0.3689	1.8035	1.8216	1.8606	1.8726	0.3706	0.3681	1.8346	1.7832
V(7)	0.3689	0.3706	0.3684	1.8441	1.8726	1.8035	1.8260	1.8576	1.7897
V(8)	1.3881	1.4298	1.4409	1.4810	1.4961	1.3982	1.3835	1.4596	1.4028
V(9)	1.3881	1.3982	1.3852	1.4687	1.4961	1.4298	1.4446	1.4772	1.4086
V(10)	10.4580	3.3448	1.5405	1.5943	2.3408	10.2874	10.2372	2.7637	1.4980
V(11)	0.8934	-0.5571	-0.9350	-2.4107	-2.3092	-0.5571	-0.9839	-2.4439	-2.7633
V(12)	10.6933	10.5227	10.4782	2.8939	2.5761	3.5800	1.5422	1.5843	1.5024
V(13)	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000
V(14)	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000
i(Vcc1)	-3.0	-3.2	-3.2	-3.3	-3.4	-3.1	-3.1	-3.3	-3.2
i(Vcc2)	-3.0	-3.0	-3.0	-3.3	-3.3	-3.2	-3.2	-3.3	-3.1
i(V1)	-0.7	-0.6	-0.5	-0.4	-0.4	-0.6	-0.5	-0.4	-0.4
i(V2)	0.3	0.4	0.4	0.2	0.2	0.1	0.1	0.1	0.1

5. Concluding remarks

In this paper, we have rather briefly surveyed fundamental theoretical results emanating from the theory of nonlinear transistor circuits. These results were used to derive nonlinear algebraic equations whose solutions are a circuit’s dc operating points. We have also described numerical methods for calculating dc operating points of transistor circuits and resolving dc converge difficulties when simulating circuits with multiple dc operating points.

Table III. Nine solutions each found by using PSPICE. Values of node voltages are given in (V) while values of currents flowing through the independent voltage sources are given in (mA).

Nine DC Operating Points of the Four-Transistor Circuit									
Variable	Sol. 1	Sol. 2	Sol. 3	Sol. 4	Sol. 5	Sol. 6	Sol. 7	Sol. 8	Sol. 9
V(1)	1.7729	1.7832	1.7698	1.8198	1.8461	1.7832	1.7680	1.8112	1.7278
V(2)	-8.2271	-8.2168	-8.2302	-8.1802	-8.1539	-8.2168	-8.2320	-8.1888	-8.2722
V(3)	-1.1060	-2.5574	-2.9343	-4.4098	-4.3081	-2.5574	-2.9832	-4.4430	-4.7634
V(4)	1.4647	7.7551	9.6267	9.0448	8.0947	1.4715	1.4616	7.9060	9.7566
V(5)	1.4647	1.4715	1.4627	7.9528	8.0947	7.7551	9.8511	9.3464	9.9668
V(6)	0.3689	1.8046	1.8227	1.8611	1.8732	0.3706	0.3681	1.8350	1.7836
V(7)	0.3689	0.3706	0.3684	1.8445	1.8732	1.8046	1.8271	1.8582	1.7901
V(8)	1.3880	1.4297	1.4409	1.4804	1.4955	1.3980	1.3834	1.4589	1.4021
V(9)	1.3880	1.3980	1.3851	1.4680	1.4955	1.4297	1.4446	1.4767	1.4079
V(10)	10.4580	3.3405	1.5409	1.5940	2.3431	10.2870	10.2370	2.7673	1.4974
V(11)	0.8940	-0.5574	-0.9343	-2.4098	-2.3081	-0.5574	-0.9832	-2.4430	-2.7634
V(12)	10.6930	10.5230	10.4780	2.8975	2.5784	3.5758	1.5425	1.5840	1.5019
V(13)	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000
V(14)	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000	12.000
i(Vcc1)	-3.02	-3.23	-3.21	-3.34	-3.39	-3.06	-3.08	-3.33	-3.19
i(Vcc2)	-2.96	-3.00	-3.02	-3.29	-3.33	-3.17	-3.15	-3.27	-3.13
i(V1)	-0.712	-0.566	-0.530	-0.377	-0.385	-0.566	-0.525	-0.375	-0.351
i(V2)	0.327	0.369	0.380	0.177	0.163	0.138	0.0842	0.134	0.142

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